



Multichannel High-Resolution Data Acquisition

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The first application we'll examine today is a multichannel, general purpose data acquisition system.



Overview

- Tradeoffs
- Signal Conditioning
- Filtering
- Multiplexing
- Interfacing to Processors
- Layout
- Demonstrations

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This section will discuss design tradeoffs and techniques for analog-to-digital data acquisition systems. We'll cover the signal conditioning and filtering requirements, as well as multiplexing. We'll see how these interact to set the overall system throughput. Along the way, we'll also be looking at the error sources of our system, to predict just how accurate our measurements will be. Tips for maximizing the effectiveness of our converter as well as general layout guidelines will be discussed.

We will discuss several common design tradeoffs for these kinds of systems, and offer advice on making the right choice in your own designs. Demonstrations with real hardware will allow us to compare different designs, and, in some cases, show designs that don't work, so that you'll know what not to do.



System Requirements

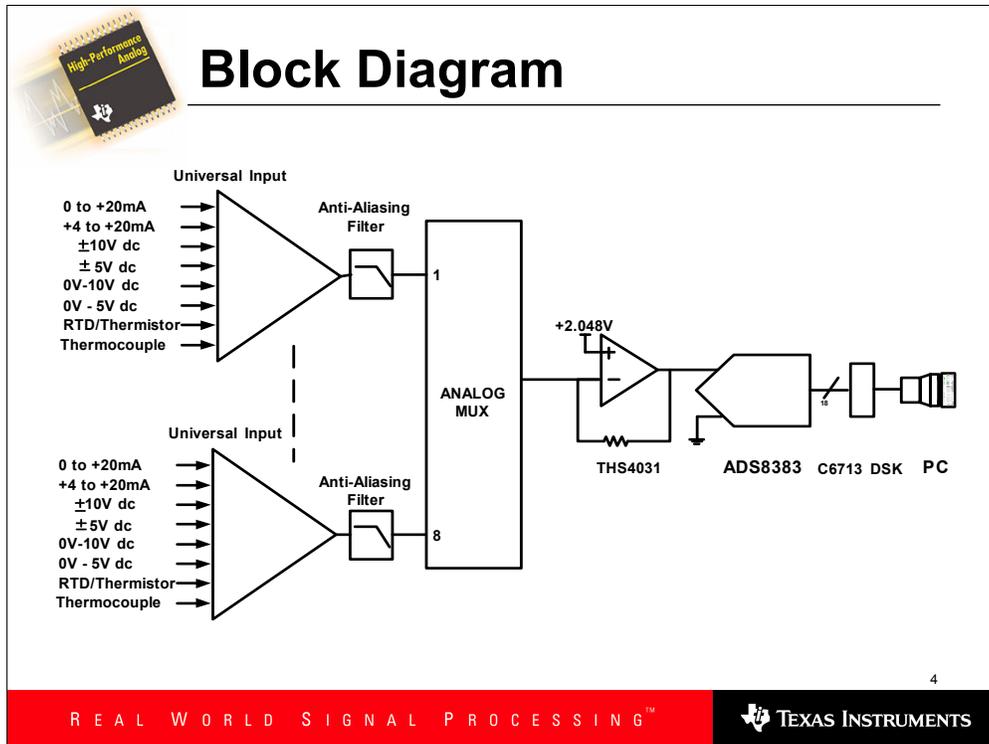
- 8 input channels
- “Universal Input”
- Fastest throughput possible with
- Highest resolution possible
- Low cost – of course!

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Our design begins where you might: with a vague and difficult system specification. All we know is that we need eight channels of input, which should be a “universal input”: any signal you might want to hook up to this should be able to be handled. We want the fastest throughput and highest resolution possible, and of course we want to do all this at the lowest possible cost. How should we approach this?



A quick block diagram helps to frame the system design. Each of the eight input channels must be configurable to handle any type of input – we’ve jotted down a few on this diagram. Each channel then must have an antialiasing filter, and then go into the multiplexer. The multiplexed signal will then be routed to the A/D converter through some type of buffer. We’ll route the resulting digital data to a DSP for evaluation purposes. In the actual design, a DSP might be used to do digital filtering or some other processing, or we may actually interface to some sort of microcontroller.

Because the system is general purpose, we really don’t know what kinds of signals or applications the measurement system may be required to handle. If the system were to be used in a high speed control loop, the time from measuring a channel to getting a precision digital representation of the signal should be minimized. Why are we concerned with this? It helps us to choose the converter type to use. For example, in multichannel imaging systems, the data is really point-by-point, and each channel needs to be independent.

A delta-sigma converter would probably not be the best choice for this type of system, as those converters assume the signal into them is continuous, and each output value is related to the previous conversion. Delta-sigma converters usually have some **latency** associated with them – the time it takes for the output to change to an accurate representation of the input after a change in input channel. We wish to minimize latency, and so choose instead a successive-approximation type converter, which can give an accurate reading based upon only one sample of a signal.



“Universal Input”

- 0-20mA
- 0-5V
- 0-10V
- $\pm 5V$
- $\pm 10V$
- Thermistor input
- RTD input
- Thermocouple input
- Output: 0 to 4.096V to match ADC

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What about that “universal input”? What exactly does that mean?

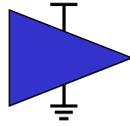
We’ve decided that for our data acquisition system, it means that any of the signals listed above may be an input. A current, a voltage, a thermistor or thermocouple, all should be able to be handled by the input signal conditioning.

The reason we wanted to know now which converter we might use is because that helps decide the signal conditioning needed: in this case, the ADS8383 can handle signals only from 0 to 4.096V, so our input circuitry should make sure that it provides that range of output from whatever input range is selected.

Let’s now consider the design of our signal conditioning.

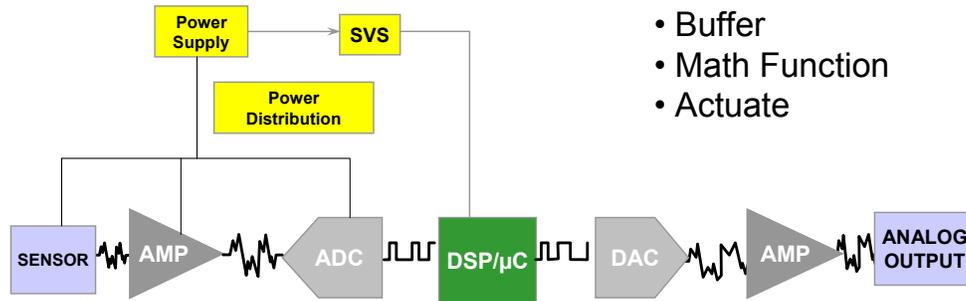


Amplifiers



Op Amps

- Amplify
- Filter
- Buffer
- Math Function
- Actuate



Op Amps Perform the Analog Signal Conditioning

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Amplifiers are used in most data acquisition systems found in the industrial world today. They are commonly found at the beginning and end of the signal chain.

They are used as an interface between the sensors that measure or monitor physical parameters. They are also sometimes used to take that measured parameter, once it has been digitized and analyzed, and force an analog response.

For example, one might be monitoring flow rate in a system. If the rate is determined to be high, a valve could be caused to move to slow down the rate.



(Q) Why is Analog so Important?

- (A) Because the world is Analog and we frequently desire to "connect" to it.
 - Signal Chains (Industrial or Otherwise) for the most part monitor a specific physical parameter (temperature, pressure, etc) and then...
 - ... control this monitored parameter either directly or through the control of another physical parameter.



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Consider the case of an oven. We desire to control the temperature of the food.

1. The temperature of the oven is measured through a thermocouple, which produces a small signal that is proportional to the temperature.
2. The electricity that is sent to the heater in the oven is turned on or off depending on the actual versus the desired temperature.



The Need for Signal Conditioning

- **(Q) Why do we need amplifiers in the first place?**
- **(A) Because most Industrial Analog Signals do not work well directly with SAR based ADC's such as:**
 - Very tiny signals from RTD's or Bridges,
 - Signals that have high common mode voltages,
 - Very wide dynamic range signals,
 - Or signals that need to be converted into an input the ADC can recognize, i.e. light or charge.
- **The goal is to take all of these “hostile” signals and convert them into a voltage which equals the input voltage range of the converter.**

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In the real world the need for amplifiers is driven by the fact that the world is analog and in general unfriendly to many data converter designs.

Throughout this section it will be assumed that you have some type of analog signal that needs to be conditioned for the input of our data converter which has a 0 to 4.096 volt full scale input range.

Some signals, such as those from an RTD, bridge, or human body are so tiny, μV 's to mV 's, that they need to be amplified heavily. In many cases these signals are differential in nature.

Another real world situation is that the signal to be analyzed is in the presence of external noise or interference. The signal might be “riding” on top of a common mode voltages that the data converter can not accommodate.

Finally, the signal might not be a voltage at all. It may be light / photons, current or even charge. Fortunately, there are amplifier devices that are designed specifically for dealing with all of these scenarios.



Selecting the Correct Type of Amplifier

- **What type of amplifier is required ?**
 - **Operational Amplifiers**
 - Ideal for tiny single ended signals.
 - Also used where common mode voltages are NOT an issue.
 - **Differential Amplifiers**
 - Best for low (< 100) gain differential signals.
 - Found where high levels of common mode voltage are present.
 - Current (shunt) measurement.
 - **Instrumentation Amplifiers**
 - Where high gain, high common mode rejection, and high input impedance are required.
 - **Analog Circuit Function**
 - Wide dynamic range (> 60dB) signals.

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The first step in the design cycle when choosing an amplifier for a data acquisition system is to determine what type of amplifier is needed.

If the signal is single ended in nature, i.e. it is referred to a common voltage like ground, then a simple operational amplifier may be best.

Not that operational amplifiers, being differential in nature, are not suited for differential signals, but there is a different class of amplifiers that are designed for these types of signals. These are called differential or instrumentation amplifiers. Rejection is what these types of amplifiers are all about. Among other considerations these devices are designed specifically to REJECT common mode signals, such as noise.

A differential amplifier (diff-amp) is a fixed gain device with relatively low input impedance. In general, diff-amps are not designed to be connected directly to a sensor. They are used most commonly to translate a differential voltage into a single ended one.

Instrumentation amplifiers (INA's) are designed to connect directly to a sensor and amplify the resulting voltage by a large (1000V/V+) factor. An INA brings together the best qualities of operational and differential amplifiers.

Finally, analog circuit function amplifiers are useful for either non-electrical or very wide dynamic range signals.



Op-Amp Technologies

- **The process used to build an Op-Amp has a significant impact on performance**
- **Four types are used**
 - Bipolar
 - JFET
 - CMOS
 - Difet
- **These technologies are sometimes combined**
 - BiFET or Bipolar and JFET combination
- **Process description is usually associated with input stage of the Op-Amp**

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The op-amps used primarily in industrial data acquisition systems are fabricated on either Bipolar, JFET, CMOS, or *Difet* semiconductor processes.

Each of these processes have unique electrical properties that in turn impacts the overall performance of the system. Hence the type of application and nature of the signal to be conditioned directs the choice of process and amplifier.

The pros and cons of each process will be covered next.



Bipolar Operational Amplifiers

- **Bipolar Op-Amps are characterized by**
 - Low input impedance, I_{bias} of 1 to 100 nA,
 - Low offset voltage, V_{os} as low as 10 μ V,
 - Temperature Stability, Drift as low as 0.1 μ V / $^{\circ}$ C,
 - Low Voltage Noise, Low as 1 nV/ \sqrt Hz.
- **Small signal, low impedance high gain applications**
 - Weigh Scales, Geophysical Analysis, High Precision Temperature Measurement.
- **Example device OPA277**
 - 2.5nA, 10 μ V, 0.1 μ V / $^{\circ}$ C, 3 nV/ \sqrt Hz



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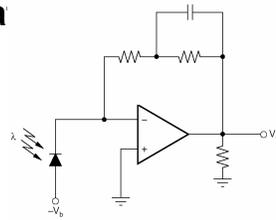
When the utmost in DC precision is required in a system, usually a bipolar based operational amplifier is best. These devices offer the highest level of common mode rejection (CMRR), open loop gain (A_{OL}), offset voltage (V_{OS}), and associated drift ($\Delta V_{OS}/T$). In addition, the voltage noise of a bipolar amplifier is very low. This is important because this noise source will be amplified by the closed loop gain of the amplifier, which is set very high for small signal sources like RTD's and bridges.

On the down side, the current noise of a bipolar op-amp is very high and the input impedance is low, as compared to other amplifiers. These two characteristics make bipolar amplifiers poor choices for high impedance signal sources, such as those found in many medical applications.



JFET Operational Amplifiers

- **JFET Op-Amps are characterized as having**
 - Moderately High Input Impedance, I_{bias} of 10 to 100pA,
 - Moderate Offset Voltage, V_{OS} of 0.1 to 5 mV,
 - Large bias current changes with temp., I_{bias} doubles every 10 °C,
 - Lowest I_{bias} noise, As low as 4 fA/ \sqrt{Hz} .
- **High source impedance, moderate gain applications**
 - Blood Analysis, CT Scanner, and Audio applications
- **Example device OPA130**
 - 20 pA, 1mV, 5 pA, 4 fA/ \sqrt{Hz}



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JFET input amplifiers are an excellent choice for high impedance signal sources. This type of amplifier is an ideal choice for transimpedance applications. Low current noise and distortion also make it a good choice for audio and other high frequency applications.

DC performance, voltage noise, and a change in input impedance with temperature limit the choice of applications that the JFET amplifier is suitable for. In general the JFET op-amp is the best choice when AC performance is paramount.



***Difet* Operational Amplifiers**

- **Difet Operational Amplifiers are characterized by**
 - Ultimate in low current and voltage noise, $4 \text{ nV}/\sqrt{\text{Hz}}$; $2 \text{ fA}/\sqrt{\text{Hz}}$,
 - Highest Input Impedance, I_{bias} as low as 3 fA ,
 - Best DC Specifications, Process allows designs that have best CMRR and AOL,
 - Highest cost, Each active device is individually isolated in glass tub, i.e. large die size.
- **High Speed / Resolution Data Acquisition**
 - Base Station Quantization, High End Medical, ATE
- **Example device OPA627**
 - $4.5 \text{ nV}/\sqrt{\text{Hz}}$, $1.6 \text{ fA}/\sqrt{\text{Hz}}$, 1 pA , 106 dB , 120 dB

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Difet, or dielectrically isolated FET op-amps offer the best of both bipolar and JFET devices. At the same time it is possible to garner both DC precision and JFET AC performance. In fact with this type of fabrication technology it is sometimes possible to exceed the performance of any other process technology.

In a conventional integrated circuit process the individual components, transistors etc., are kept electrically isolated from each other by reverse biasing the substrate based diode common in this process. In a *Difet* design the isolation process is accomplished by placing the individual components in glass or dielectric tubs. While this technique results in superior performance it also dramatically increases both the fabrication process and resulting die size. The cost of a *Difet* device is always higher than an equivalent Bipolar, JFET, or CMOS device.

This added cost and higher performance in general makes the *Difet* device suitable for only very high performance data acquisition systems.



CMOS Operational Amplifiers

- **CMOS devices are characterized as having**
 - Large Input Voltage Range, Input can often exceed both supplies,
 - Excellent Output Drive Capability, Output swings to within 1mV,
 - Excellent V_{OS} , 125 μ V
 - Very Low Power Requirements, $I_q < 1 \mu$ A,
 - High Input Impedance, I_{bias} of 10 pA,
 - Low Cost, Built using small geometry “Digital” processes,
 - Wide variety of bandwidth and accuracy offerings.
 - Wide temperature range, -65 to +150 ° C
- **Battery powered, low to moderate performance systems**
 - Glucometer, CDAC ADC driver, CO and Smoke detectors
- **Example device OPA336**
 - ± 300 mV, 3mV, 125 μ V, 125 μ V, 1pA, 100kHz

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When the CMOS process was first used to build amplifier products the resulting devices were generally of very low performance. They were slow, noisy, and had poor DC performance. A lot has changed since then and you can now obtain CMOS amplifiers with levels of DC precision approaching Bipolar products and AC performance that in some cases exceeds JFET ones.

As is widely known, CMOS devices are known for rail-to-rail operation, small size, low power, and cost. TI has CMOS amplifiers that can accept input signals in excess of both supply rails, whose output stages can swing to within 1mV of each supply rail, and that have bandwidths of almost 500MHz. In terms of DC performance there are devices with offset ratings of less than 100 μ V and A_{OL} and CMRR specifications in excess of 100dB. Also, these devices are very quiet with voltage noise floors of less than 5 nV/ \sqrt Hz.

The CMOS process used at TI is very amenable to optimization. There are devices that are optimized for the following characteristics

- Speed / Power or MHz per μ A. OPA348 has 1MHz BW while using only 45mA of I_Q .
- Output drive – a very important parameter for driving CDAC based converters. OPA353 can drive a 10K Ω load to ± 1 mV of each supply rail.
- Over temperature performance. -65 to 150 °C operation makes these devices very suitable for automotive and industrial applications.
- Building blocks for other amplifier applications. TI builds a wide variety of other amplifier devices using the CMOS op-amp as the central element.



CMOS Auto Zero Amplifier

OPA335

- **Most precise CMOS architecture**
- **Bipolar Precision + CMOS Advantages**
 - Rail-to-Rail output
 - Low Power
- **Achieves chopper type precision and drift without the chopper drawbacks**
 - V_{OS} and Drift – $5 \mu\text{V} / 0.05 \mu\text{V}/^\circ\text{C}$
 - Noise – $1.4 \mu\text{V pp}$
 - Bandwidth – 2MHz
- **Uses an auto-zero topology in series with a time continuous operational amplifier**

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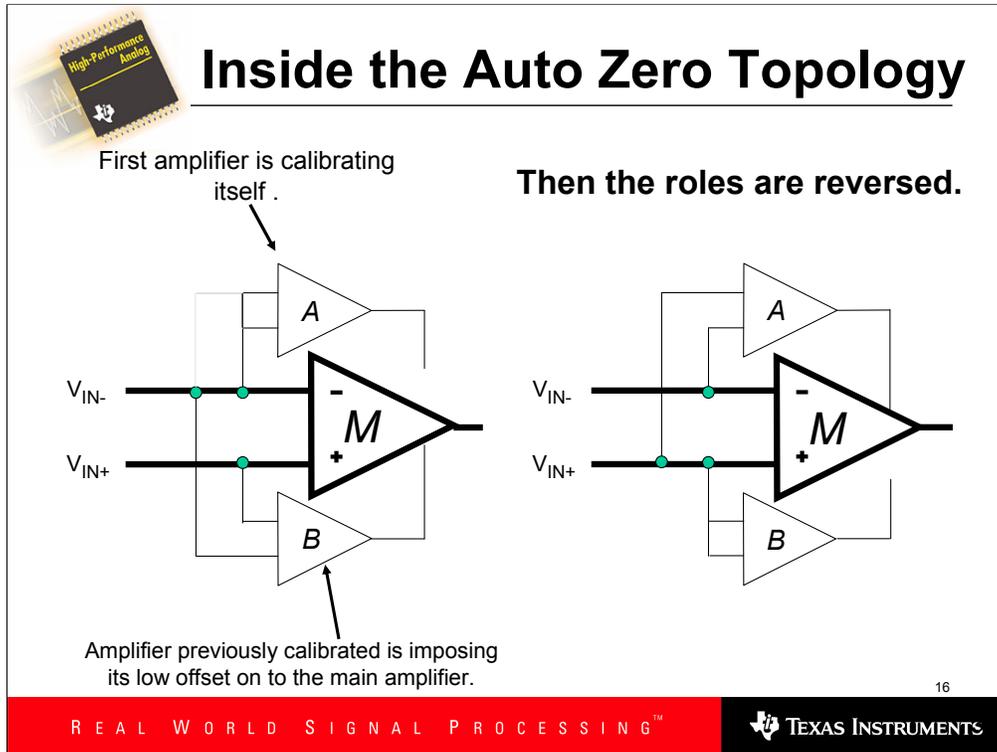
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The latest “version” of amplifier to take advantage of the CMOS process is the auto zero op-amp. This new topology is sometimes compared with the “chopper stabilized” type of amplifier. The reason for this is that both approaches offer the best performance in terms of offset voltage and drift. However, the auto-zero amplifier does not suffer from the pitfalls of the chopper type. The chopper amp is known for high levels of noise and low bandwidth.

The auto-zero amplifier uses a time continuous amplifier in the signal chain that is constantly corrected for its offset voltage. This approach yields a precise, fast, low noise op-amp.

The auto zero amplifier, being a CMOS device, is ideal for single supply data acquisition systems. Due to its high levels of precision and excellent drive capability it is ideal for driving high resolution (16+ bits) data converters. A typical application would be a commercial weigh scale.



The diagram above illustrates the action of the auto zero amplifier. At first calibrating amplifier B is imposing its previously calibrated output of the main amplifier M. During this cycle amplifier A is sampling the offset voltage present on the inverting input.

During the next cycle the main amplifier is calibrated by amplifier A to eliminate that offset voltage. So the main amplifier is continuously calibrated for input offset voltage. Because this action occurs over temperature as well, offset voltage drift is also eliminated.

Auto Zero Op-Amp Application

Concept:

- Wideband CMOS OPamp
- High Precision Integrator

Results:

- **1MHz** TZA Bandwidth
- 0-5V Output Range
- 16 μ Vrms Integrated Noise
- **10 μ V** DC Offset
- Long-term Stability
- \approx 5nA to 1.2mA (**107 dB!**)
- Both parts in SOT23

diode's parasitic capacitance

Eliminates Offset

Noise Filter

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The auto zero amplifier, OPA335, can also be used to calibrate other linear systems. In particular the above concept can be used on any inverting input amplifier system that employs negative feedback. An example of such a system is the classic transimpedance amplifier (TZA). In this case it is assumed that the input is a photodiode.

One of the limitations of the conventional TZA is that the offset voltage of the op-amp limits the dynamic range (i.e. size of the feedback resistor) available. This limitation tends to restrict its use to input current ranges of less than 60dB. In many TZA applications the input range is far higher, up to 160 dB.

In the example shown the OPA335 auto zero amplifier continuously compensates for the offset voltage of the TZA amplifier, the OPA353. The resulting circuit results in a TZA application that offers large dynamic range, low noise, and excellent DC precision.

With the addition of a negative supply and pull down resistors the output of the OPA335 and OPA353 can go from 0 to +4.999 volts, which is within 1mV of the full scale range of many data converters. This is another unique feature of the CMOS op-amp offering from TI. The outputs can actually be pulled down below the negative rail without damaging the device.



Recommended Op-Amps

Device	Offset Voltage (μV)	Input Bias Current (pA)	GBW Product (MHz)	Voltage Noise ($\text{nV}/\sqrt{\text{Hz}}$)	Current Noise ($\text{fA}/\sqrt{\text{Hz}}$)
OPA131	± 750	± 50	4	15	3
OPA227	± 75	± 10	8	3	400
OPA277	± 20	± 50	1	8	200
OPA344	± 500	± 50	2	30	0.5
OPA335	± 5	± 50	2	50	20
OPA627	± 100	± 50	16	4.5	2.5

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Instrumentation Devices

- **Many types of Instrumentation Devices**
 - Difference Amplifiers
 - Current Shunt Amplifiers
 - Instrumentation Amplifiers
 - Programmable Gain Amplifiers
 - 4-20 mA Transmitters
- **All of these devices share similar characteristics**
 - Combination of precision op-amp and trimmed resistors
 - Accept a differential voltage
 - Are easily programmed for a fixed gain
 - Used for a variety of input signal conditions

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Instrumentation devices are designed to interface with specific types of sensors used to monitor physical parameters in the real world. There are devices designed to measure current, temperature, pressure and reject very high levels of common mode voltage.



Difference Amplifiers (Diff Amps)

- A Diff-Amp is an Op-Amp + 4 or 5 Resistors.
- Characterized by
 - Low Input Impedance , $10\text{K}\Omega \sim 1\text{M}\Omega$
 - Moderate CMRR, $70 \sim 80 \text{ dB}$
 - Bandwidth, $100\text{KHz} \sim 5\text{MHz}$
- Function is to accept differential input voltage and output a single ended voltage.
- Diff Amps are designed for specific functions.
 - Unity gain devices $V_{\text{IN}} = V_{\text{OUT}}$
 - Devices with gain $V_{\text{IN}} < V_{\text{OUT}}$
 - Devices with attenuation $V_{\text{IN}} > V_{\text{OUT}}$
 - Devices which support large common mode voltages:

$$V_{\text{IN}} + \text{⚡} = V_{\text{OUT}}$$

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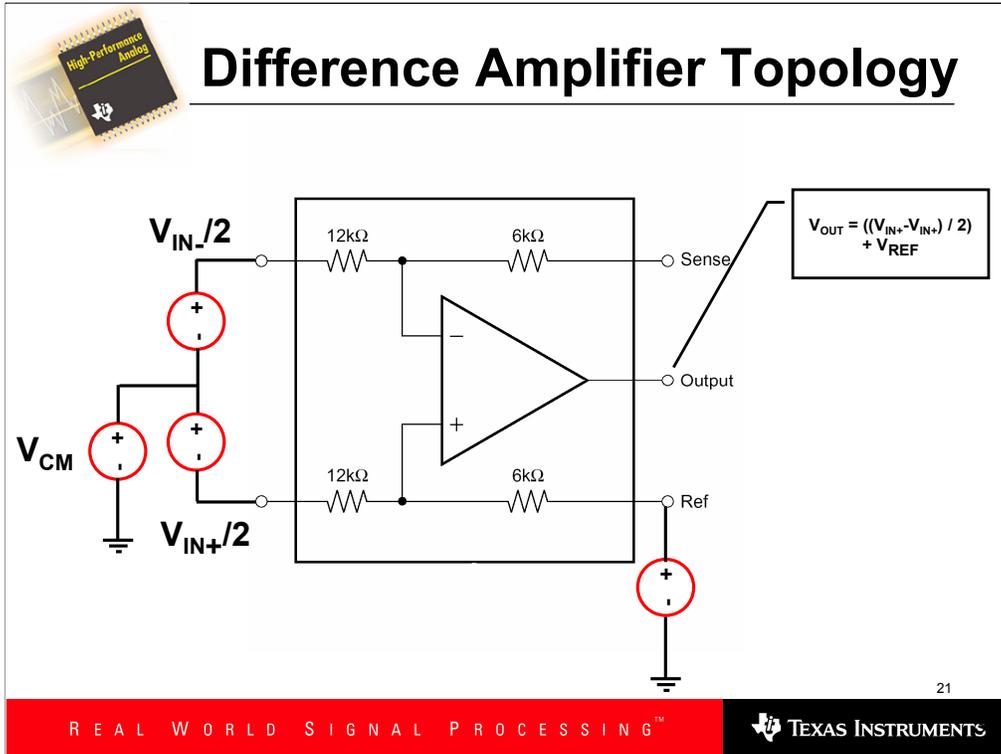
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Difference amplifiers, as the name implies, measure the magnitude of a differential voltage and deliver an output that is proportional to it. This output is referenced to a reference voltage, V_{REF} .

The diff-amp can buffer, amplify or attenuate the input signal. A conventional diff-amp uses four precision resistors and one op-amp.

With the addition of other resistors the diff-amp can be used to hold off or interface with very high levels of common mode voltage. In fact there are devices available that allow systems that are powered from conventional analog power supplies (± 15 volts) to monitor signals that are in the presence of up to ± 200 Volts!



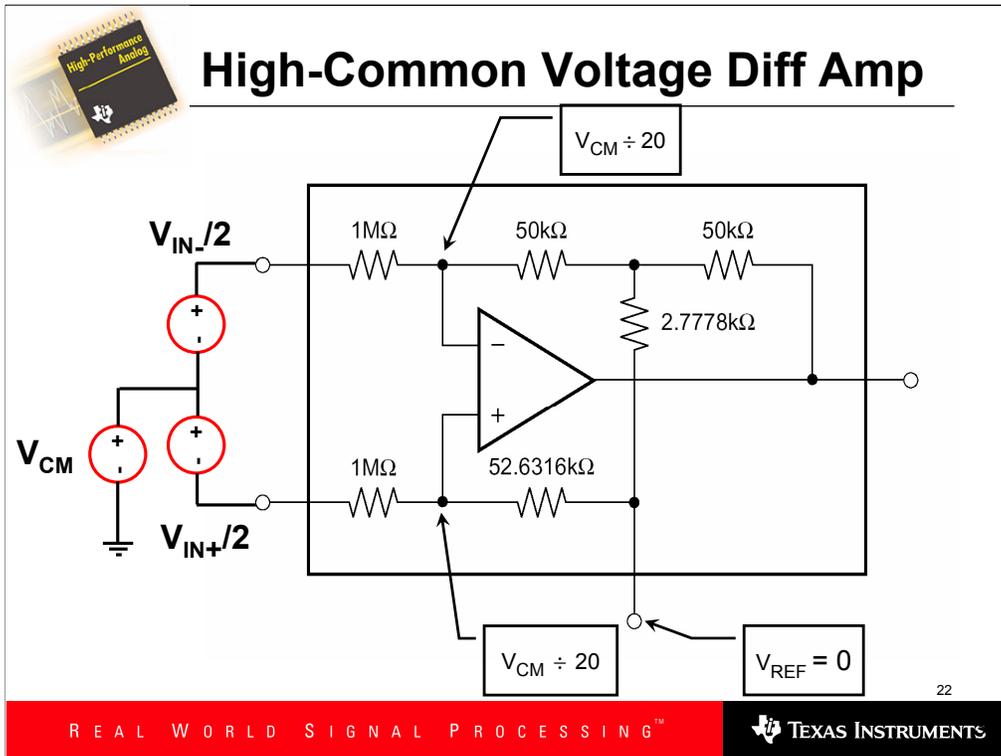
The figure above shows the topology of the conventional diff-amp. In the example the input resistors (12kΩ) are twice the value of the feedback resistors (6kΩ). This results in a design that actually attenuates the input voltage.

Why is this useful for a data acquisition system?

Suppose for example we have a data converter that is run from a single +5 volt supply whose full scale input voltage is somewhere between 0 and +5 volts. If an input voltage of -5V to +5V is to be monitored then a way is needed to accurately translate this input signal to the data converter. Using a diff-amp, like the one shown above, would divide down the 10 volt input span to 5 volts (+2.5 to -2.5). We then apply +2.5 volts to the V_{REF} pin and the input signal is now 0 to +5. In the process we have not lost any accuracy and have preserved the differential nature of the signal, thus improving noise immunity.

A final word about the nature of resistors used in instrumentation products is in order. The absolute value of these resistors is on the order of 30%. Also the match between the pairs of input or output resistors is not in general precise. Instrumentation devices achieve their high levels of performance due to the precise ratio between a feedback and corresponding input resistor. They are laser trimmed to ratios of 0.001% or better.

It is for this reason and the low, sub 1MΩ value of these resistors, that differential amplifiers are suitable for signal sources with low impedance.



Another type of differential amplifier is a device that is designed to interface with high levels of common mode voltage. Like the conventional diff-amp we have a differential input stage whose value is compared by an op-amp and then made relative to a reference pin.

This device has an additional set of resistors that divide down the common mode voltage, in this example by 20. This type of amplifier will work with common mode voltages of up to ± 200 volts continuously, ± 500 volts for up to 10 seconds. This makes it very useful for a wide variety of industrial and telecommunications applications.

An obvious question at this point is why bother with an integrated difference amplifier in the first place? Would it not be less expensive to use a combination of a discrete op-amp and resistors?

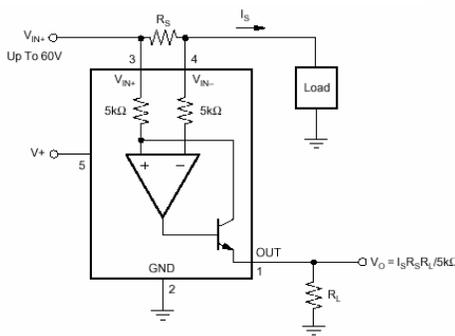
The answer is yes it would be less expensive but performance would suffer. In general, if the desire is to achieve CMRR performance of better than 60 dB and linearity of better than 12 bits, a purpose-built diff-amp is needed.



Current Shunt Monitors

INA138

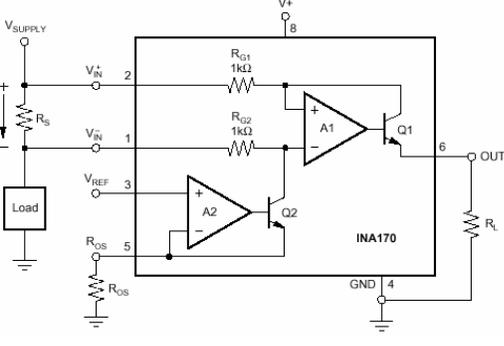
High-Side, *uni-polar*



$V_O = I_S R_S R_L / 5k\Omega$

INA170

High-Side, *bi-directional*



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 TEXAS INSTRUMENTS

The last type of diff-amp to be discussed is the current shunt amplifier. These devices are designed to monitor currents of up to 25 amps and can monitor supply voltages of up to 60 volts while drawing only 25μA and running on supplies as low as 2.7 volts.

There are two types of current shunt amplifiers currently available. The first uses a single op-amp and is suitable for measuring currents flowing into a load. This device is programmed by a single resistor such that the output is proportional to the current flowing into the load.

The second type is useful when it is necessary to monitor currents flowing either into or out of the load. This device has a second element in the transfer function, namely the output voltage that is desired when the load is drawing no current. This is also set with an external resistor.



Instrumentation Amplifiers

- **Instrumentation Amplifiers (INA's) feature**
 - Differential Inputs
 - Gain setting via a standard resistor
 - Superior noise immunity, better CMRR vs frequency than standard op-amp designs

- **There are specific INA devices for**
 - Single Supply Applications
 - Low Noise Applications
 - High Impedance Sources
 - Programmable Gain

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The last type of instrumentation devices to be discussed are the true instrumentation amplifiers, INAs. Like diff-amps these devices have a differential input. Unlike diff-amps they have high input impedance inputs and feature adjustable gain. The gain is set with an external resistor.

There are also devices, programmable gain amplifiers or PGAs, that have gain setting resistors built in. The gain can be set “digitally” via internal switches.

“Two” Op-Amp INA

$$Gain = \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{2 \cdot R_1}{R_G}\right)$$

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Like the op-amps that are used to construct them, there are a number of configurations and performance options available for INAs.

The most basic INA uses two op-amps and four resistors in its construction. This topology, as one might imagine, is the smallest, lowest power, and lowest cost choice available. The trade off for the 2 versus 3 op-amp design is lower cost and power versus minimum required gain and lower AC CMRR.

There are two big limitations with this type of design. First there is a minimum gain that can be had from this design. The second and more important limitation is that the CMRR ratio changes dramatically with frequency as compared with other types of INAs. This response is caused by the asymmetrical path from input to output with regard to the inputs.

As can be seen from the diagram, the negative input goes through both op-amps whereas the positive signal path only goes through one. This results in different phase response between the positive and negative inputs and results in lower CMRR as frequency increases.

This type of instrumentation amplifier is usually used in lower performance systems. Most of the new product development for this type of device is being done on the CMOS process.

“Three” Op-Amp INA

$$Gain = 1 + \left(\frac{2R_1}{R_G} \right)$$

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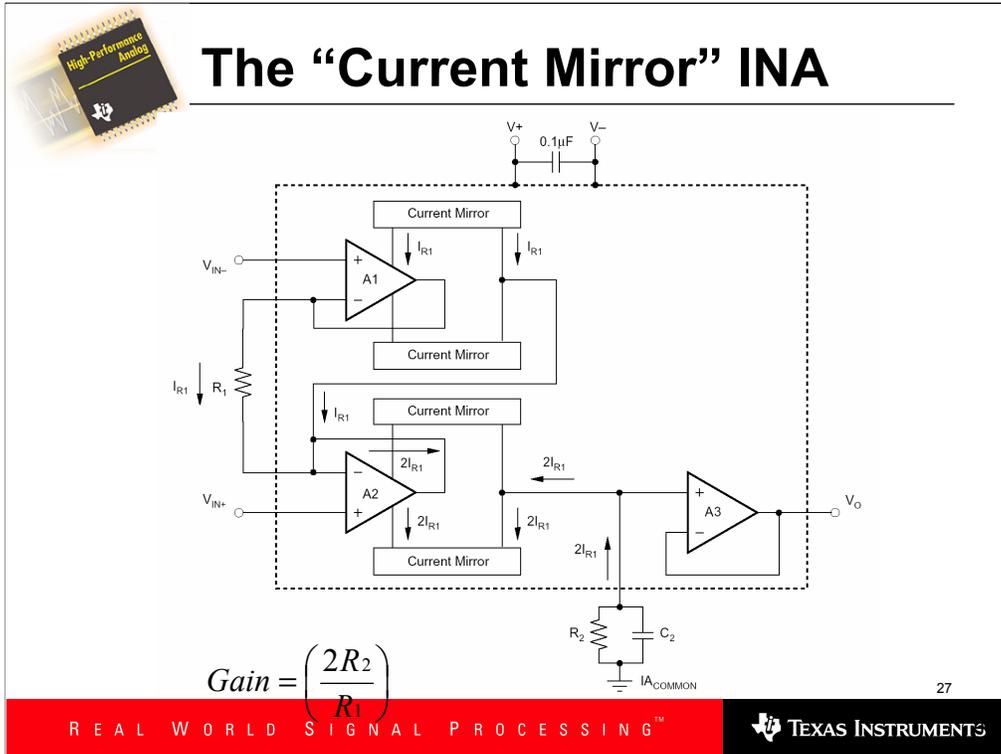
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The three op-amp INA has the highest levels of overall performance available today. Voltage gains of 1 to 10,000 V/V are achievable. It does not suffer from the CMRR vs. frequency limitations of the two op-amp approach. In fact, the three op-amp INA rejects 60Hz common mode noise 10 to 20 times better than does the two op-amp version.

Finally, since this device is intended for high end signal acquisition it is common for additional features to be included in its design, such as over voltage protection.

The three op-amp INA is currently offered on the Bipolar, JFET, and *Difet* semiconductor processes. Hence there exist a wide choice in terms of DC and AC performance parameters.



The current mirror INA, the INA326, is the latest innovation in instrumentation amplifier design. While all previous INA topologies were based on voltage gain and feedback, this device uses the current that is generated as a result of the input differential voltage divided across the gain setting resistor R_1 as the main feedback signal.

The principal of operation is fairly straightforward. First of all, the front end of the amplifier is internally powered by a pair of charge pumps. This allows input voltages to actually exceed the rails by 20mV. The input voltage impressed across R_1 generates current I_{R1} .

I_{R1} is mirrored and ultimately multiplied by a factor of two. The resulting current is drawn across R_2 resulting in the gain equation shown above.

Another feature of this type of INA design is the ability to easily implement low-pass filtering. A capacitor can be placed in parallel with R_2 , causing the gain of the INA to decrease with frequency. This is particularly useful when anti-aliasing or noise reduction is desirable in the application.

Like the CMOS op-amps that the INA326 is based on, rail-to-rail performance is excellent. This makes it an excellent choice for driving single supply CDAC data converters. Also since the input is very high impedance almost any signal source can be interfaced to it.



Instrumentation Devices

Device	CMRR (dB)	Bandwidth (MHz)	Non-Linearity (%)	Offset Voltage (μV)	Gain Range (V/V)
INA128	120 (G = 100)	0.2 (G = 100)	0.002	50	1-10,000
INA148	70	0.1	0.001	5,000	1
INA154	80	3.1	0.001	750	1
INA169	100	4.4	0.1	1,000	200$\mu\text{A/V}$
INA170	100	0.4	0.1	1,000	200$\mu\text{A/V}$
INA326	100 (G = 100)	1 (kHz) (G = 100)	0.5	0.125	0.1-10,000 ²⁸

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Current to Voltage Conversion Solutions

- Transimpedance (TZA)
 - Op-Amp + Resistor
- Integrator
 - Op-Amp + Switch + Cap
- Logarithmic Amplifiers
 - Op-Amps + VBE of a BJT
- Direct Digital Conversion
 - Charge input Data Converter

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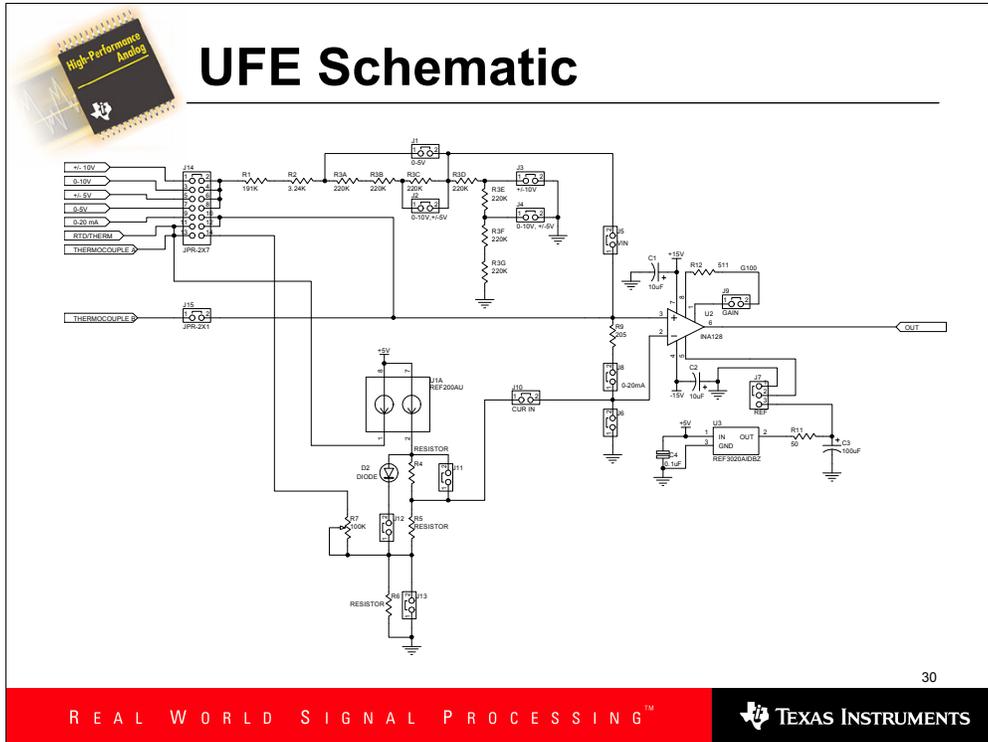
TEXAS INSTRUMENTS

If the parameter of interest is light, or one of its derivatives, charge or current, then a different approach is required.

TI offers 4 basic approaches to aid in converting light intensity into a voltage suitable for digitization.

- (1) Simple transimpedance: An op-amp with a resistor in the feedback loop.

$$V_{OUT} = I_{IN} * R_{FB}$$
- (2) Integrator: Integrates an input current across a precision capacitor. V_{OUT} = Integral of Input Current vs time divided by the integration capacitance
- (3) Log amplifiers: A special class of amplifiers whose output is the Logarithm of the input current divided by a reference current. Very accurate and temperature stable. With these devices it is possible to accurately scale 6 ~ 7 decades of input signal to a 0 to 5 volt signal, as may be needed by a data acquisition system.
- (4) There are also data converters available that use charge or current as the input parameter. The current state of art for these is a 20 bit delta sigma converter – the DDC112. These devices do have a rather limited input current (charge) input which relegates their use to electronic imaging,



We've opted to use an instrumentation amplifier for the active signal conditioning, because of the small differential signals that we may encounter in the presence of significant common mode voltages, particularly with the current and thermal input sensors. Moreover, the high input impedance helps us to design simple divider-type circuits to handle the higher single-ended voltage ranges.

The schematic for one channel of our complete "Universal Front End" is shown here. Because this is a difficult slide to view at once, we'll look at it in terms of each input range and the equivalent circuits.



UFE – Jumper Setup

JUMPER	0-5V	0-10V	+/-5V	+/-10V	0-20mA	RTD/Therm	Thermocouple
J1	On	Off	Off	Off	Off	X	X
J2	Off	On	On	Off	Off	X	X
J3	Off	Off	Off	On	Off	X	X
J4	Off	On	On	Off	Off	X	X
J5	On	On	On	On	Off	Off	Off
J6	On	On	On	On	On	Off	Off
J7	1-2	1-2	2-3	2-3	1-2	2-3	2-3
J8	Off	Off	Off	Off	On	Off	Off
J9	Off	Off	Off	Off	Off	Off	1-2
J10	Off	Off	Off	Off	Off	On	On
J11	X	X	X	X	X	On	Off
J12	X	X	X	X	X	Off	On
J13	X	X	X	X	X	On	Off
X= Do Not	Care						

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Demonstration

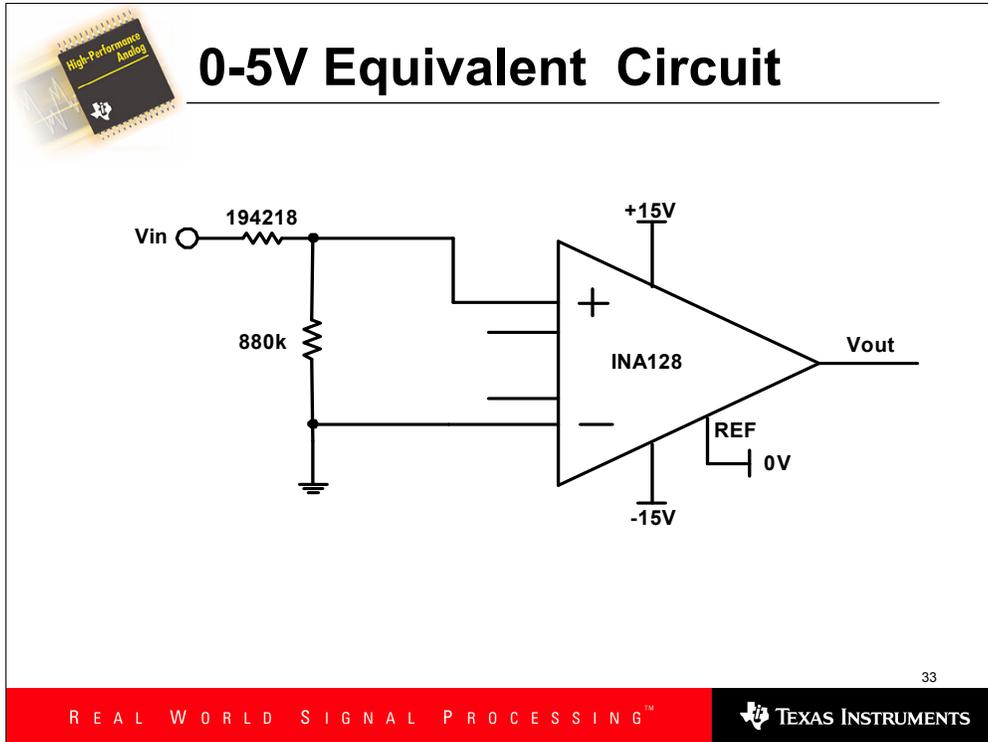
Universal Front End

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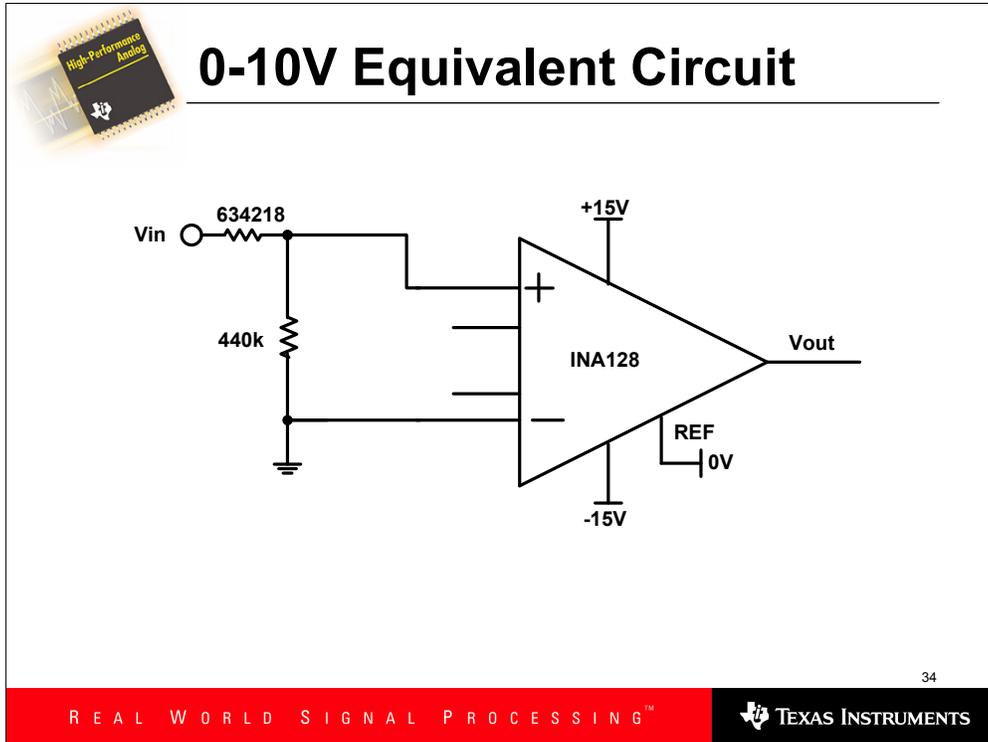
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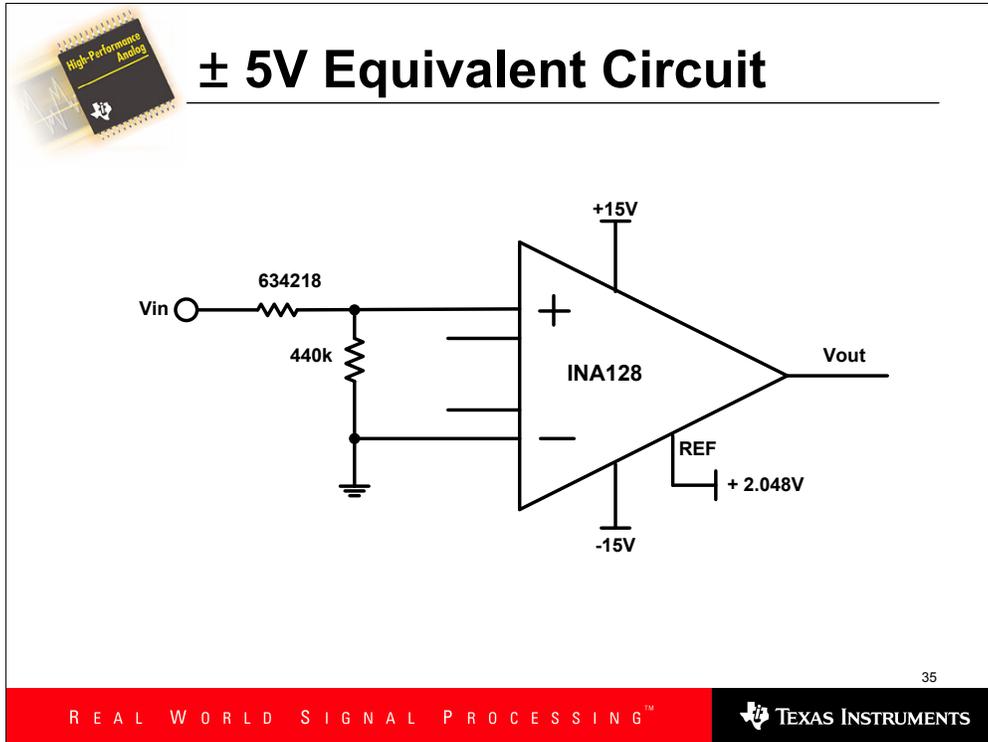
[A live demonstration illustrating the operation of the universal front end will be performed during this slide]



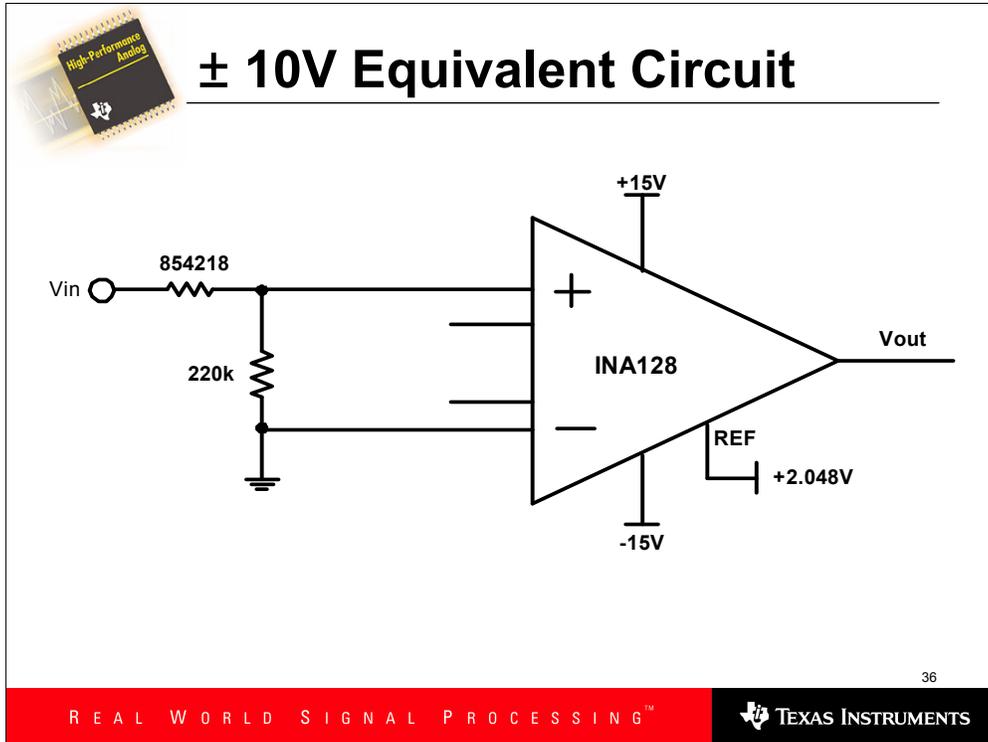
The 0-5V input is simply a small voltage divider into a gain of 1 amplifier. We need only to reduce the 0 to 5V single-ended input down to 0 to 4.096V. The values chosen for the resistive divider on this and the other voltage inputs provides an input impedance of just over 1M Ω .



Similarly, the 0 to 10V range is simply a voltage divider as well. Again, we use a gain of 1 for the instrumentation amplifier.

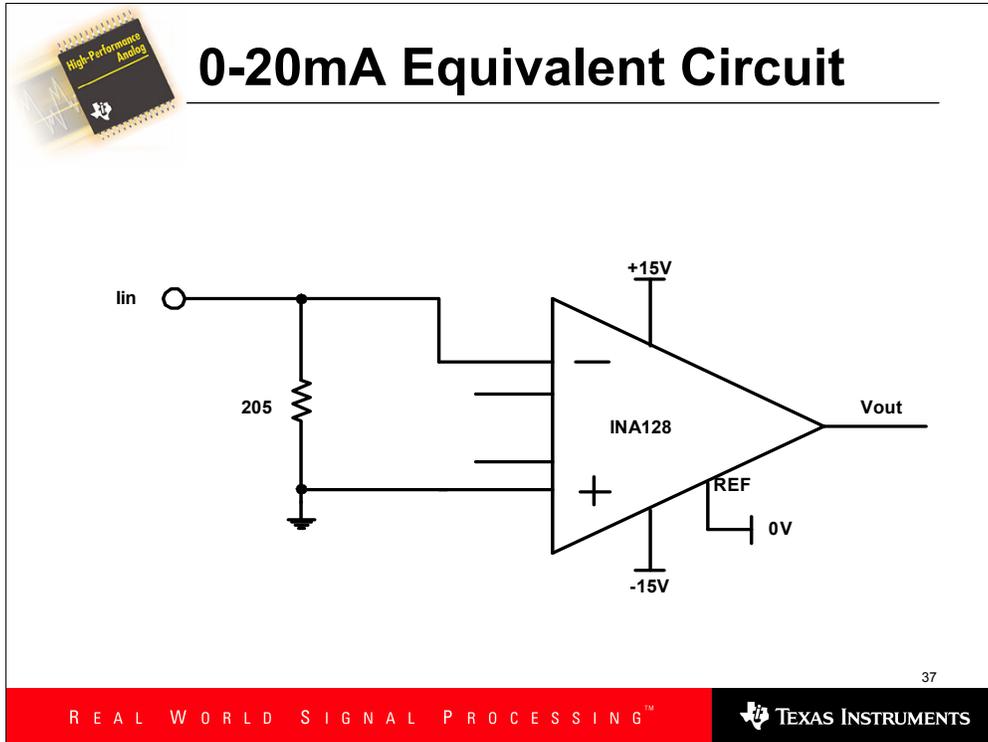


The +/-5V input range is essentially the same as the 0 to 10V range: each has a span of 10V. So the same voltage divider ratio is used to reduce this range to 0 to 4.096V. The trick here is to use the instrumentation amplifier's reference pin to offset the output of the instrumentation amplifier by 2.048V, so that when 0V goes into the input, the output is at half of its range.



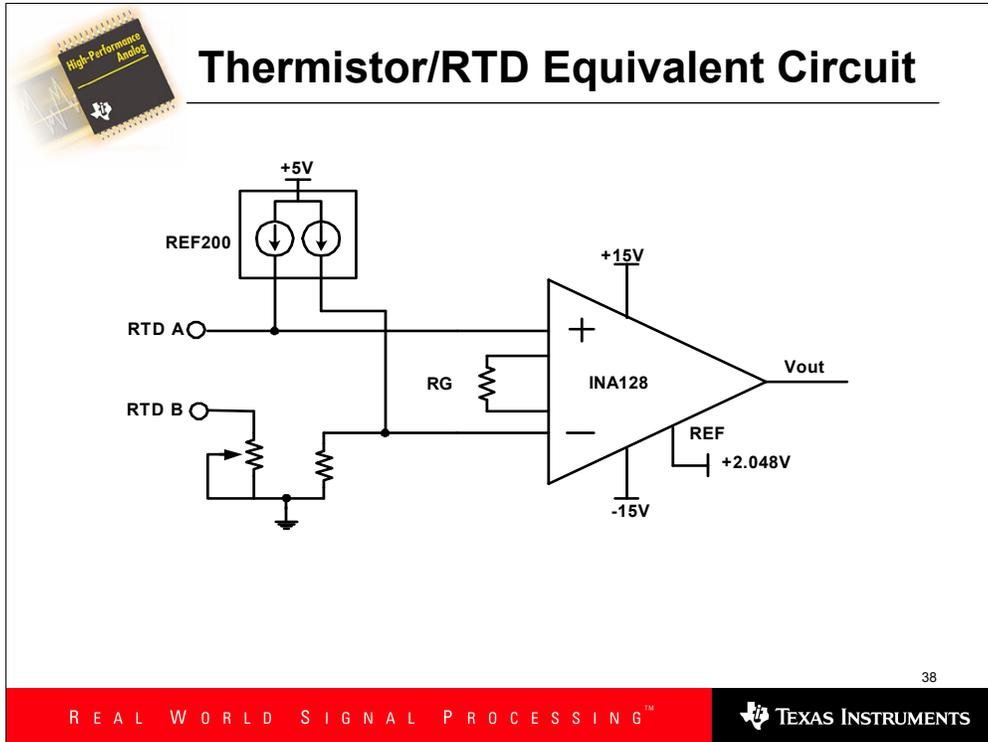
Using the same offset technique, we establish a different divider ratio for the $\pm 10V$ range, which has a 20V span.

That concludes the design for the simple single-ended voltage input ranges. Now we move into a bit more involved designs as we look at the current and thermal inputs.

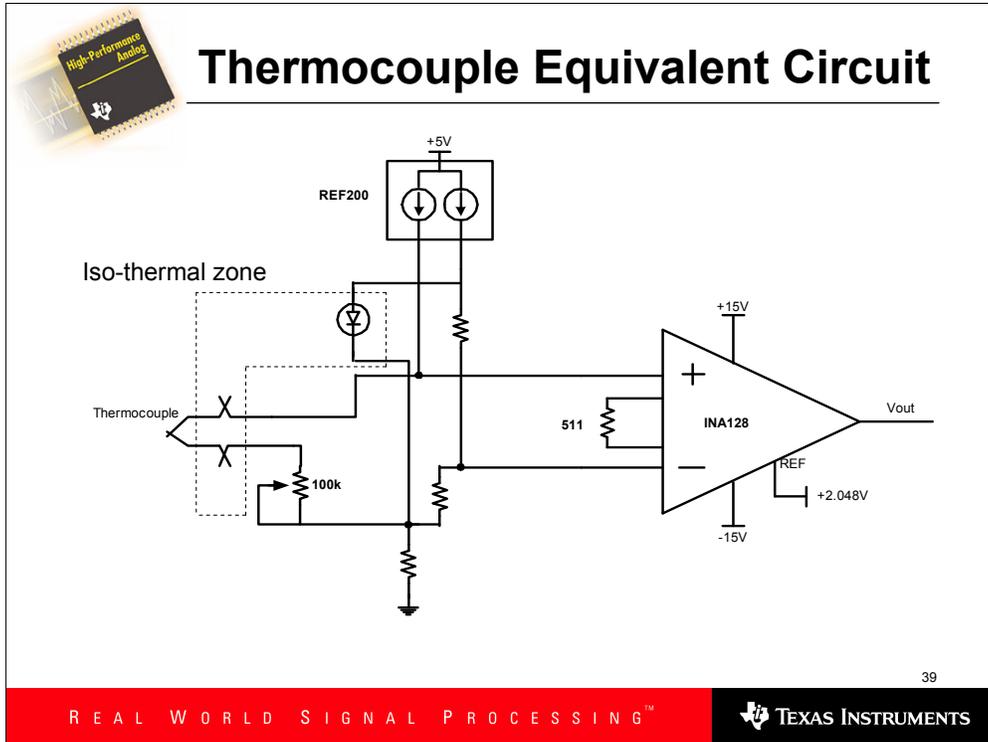


The current input is set up for a simple instrumentation current loop. Typically these are 4-20mA current loops; some are 0-20mA. We've opted to use only the 0-20mA range, as it encompasses the 4-20mA range.

Typically, one simply drops a 250ohm resistor across a current loop to get a 5V full scale signal, which is sensed across the resistor. To accommodate our ADC input full scale range, we simply use (ideally) a 204.8Ω resistor, which will give 4.096V across it with a 20mA current input.



The Thermistor and RTD both indicate temperature by a change in resistance. One easy method to measure resistance is to pass a known current through it and measure the voltage developed. In this case the known current is 100uA. The value of R(Zero) is set to be equal to the resistance of the sensor when it is at the temperature associated with a zero voltage out of the INA128. Knowing the resistance value of the sensor at maximum temperature then allows calculating the voltage developed across it and therefore, determination of the gain necessary for the INA. If the temperature is lower than the R(zero) set point then the output voltage will be negative – we therefore offset the output with 2.048V so that our output doesn't go below 0V.



A thermocouple develops a voltage based on the difference of temperature between the measurement junction and the “cold junction”. In this circuit a Si diode is used to measure the temperature within the iso-thermal zone. This is the cold junction of the thermocouple. See the app note **“Voltage Reference Scaling Techniques Increase Converter and Resolution Accuracy”** <<http://www-s.ti.com/sc/psheets/sbaa008/sbaa008.pdf>> for more ideas on thermocouple cold junction compensation.



Error Sources in our UFE

- Calculated:
 - Offset: $\pm 550\mu\text{V} = 35.2 \text{ LSB}$
 - Can be compensated for in software
 - Gain: $1.074\% = 43.99\text{mV} = 2815 \text{ LSB}$
 - Can be compensated for in software
 - Probably doesn't get us in trouble reducing dynamic range
 - Drift: $1.025\text{mV} = 65.6\text{LSB}$
 - May be compensated for if we measure temperature
 - Noise – we'll look at after filter

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Now that we've examined the different circuit topologies, let's look at the error sources in the front end. We'll take a look at the maximum error specifications of all of the components in the circuit.

The INA128 is our active component. The errors associated with it are:

Offset is listed as a maximum of $\pm 50 \pm 500/G \mu\text{V}$; this is an input-referred offset number.

Drift is listed as $\pm 0.5 \pm 20/G \mu\text{V}/^\circ\text{C}$, again as an input-referred error.

Gain error at a gain of 1 is $\pm 0.024\%$, and changes $10\text{ppm}/^\circ\text{C}$.

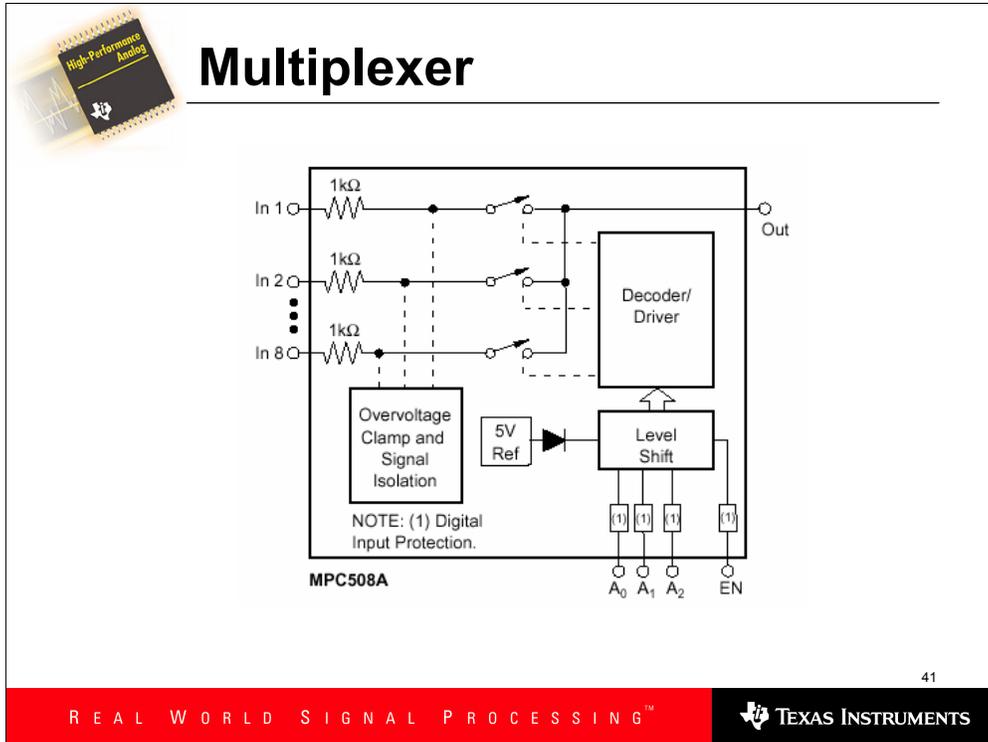
The resistors used for the divider and gain setting are at best 0.1% , and unless you really pay a lot for them, perhaps $20\text{ppm}/^\circ\text{C}$. There are 9 of these resistors in our front end for voltage inputs.

So, for our voltage ranges, the errors would look something like this, assuming an operating temperature range of 0 to 50°C , which is typical of many data acquisition systems of this type:

Resistors: $9 \times 0.1\% = 0.9\%$ initial

$50 \times 20\text{ppm}/^\circ\text{C}$ (we'll assume the resistors all drift the same direction) = 0.1%

TOTAL: 1% - this will show up as a gain error in our system



Now we must choose the means to multiplex eight analog channels into one. A multiplexer is simply a set of analog switches which have one common terminal, and can be easily addressed and turned on under digital control.

The first important parameter for a multiplexer is obviously the number of channels that it has, and whether or not it handles single-ended or differential inputs. In our system, the inputs are all single-ended, since our signal conditioning and filtering have provided us with single-ended signals. So a simple single-ended 8-channel multiplexer is all that is required.

As shown above, the analog switches in a multiplexer may have significant on-resistance – in the one shown above, it is 1kΩ. Because of this, the output of the multiplexer is usually buffered with an op amp.



Throughput Issues

- Channel switching time
 - Usually specified
- Settling time
 - May or may not be specified, and probably not to 18 bits.
- Throughput limited by switching + settling times
 - MPC508: $4\mu\text{s} = 250\text{kHz}$, but...
- Need to evaluate and see what will work
 - MPC508: $6\mu\text{s} = 167\text{kHz}$

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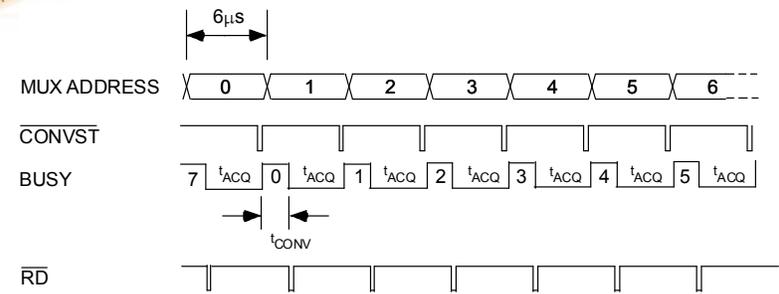


Since the multiplexer is the device responsible for switching from one channel to the next, another important parameter is the time it takes for the mux to switch from channel to channel. Once switched to a new channel, how long does it take for the output to settle?

The first parameter is often shown on a mux datasheet. Looking at the MPC508 which was shown on the previous slide, it takes $0.5\mu\text{s}$ to change from one channel to the next. Its settling time is only listed to 0.01% - and this takes $3.5\mu\text{s}$! So switching from one channel to another would take at least $4\mu\text{s}$ – and that is only to 12 bits! Some experimentation is needed to determine that for this multiplexer, about $6\mu\text{s}$ is needed to settle adequately.



System Timing – First Look



- Overlapping mux and conversion
- Total throughput: 167kHz
- Per channel: 20.8kHz

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We now need to consider our system timing, at least to a first approximation. We need to determine just what throughput our system will have, as this will affect decision we make about our antialiasing filters.

Because we control the time at which the multiplexer switches, and the time the converter starts its conversion, we can take into account the overall settling of the multiplexer and its buffer op amp, if used. This slide shows a timing diagram of how we command the multiplexer to switch and start conversions. The key here is to switch the multiplexer, wait 6µs, then start a conversion. Once the conversion has started, the A/D converter has the input held on its internal sampling capacitor, so we are free to change the multiplexer channel, allowing it to begin settling while the converter is converting the previous channel's data that it has acquired. Once that conversion is complete, we read it as quickly as possible, so that the reading of the data is not occurring during the critical acquisition time of the ADC, which could potentially cause noise and corrupt the acquired signal.

From this, we can see the overall throughput that is attainable by our system: 167kHz sample rate, which equates to a 20.8kHz rate per channel if we were scanning through all eight channels. However, if we wanted to switch to one channel and stay there, then we wouldn't have to allow for mux settling, and could potentially sample at the full 500kHz rate the ADS8383 is capable of doing.



Demonstration

Settling Time

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[A live demonstration illustrating allowing adequate time to settle will be performed during this slide]



Crosstalk

- Amount of feedthrough from adjacent channels
- Could show up as noise or offset
 - MPC508: as much as 1% of OFF signal

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A further specification that is often shown on multiplexer datasheets is crosstalk. This is the amount of signal that may feedthrough from off channels when one channel is selected. This would commonly show up as noise in the channel of interest, but may also manifest itself as an offset, depending upon the signals used and the particular multiplexer in use.

Again, this may or may not be specified. If it is, it may be in a curve plotted against signal frequency – higher frequencies will tend to feedthrough more as the mechanism of crosstalk is usually parasitic capacitances associated with the analog switches.



Error Sources in our Mux

- On-resistance
 - Not a problem as buffered on both sides
- Noise
 - Crosstalk
 - Digital feedthrough

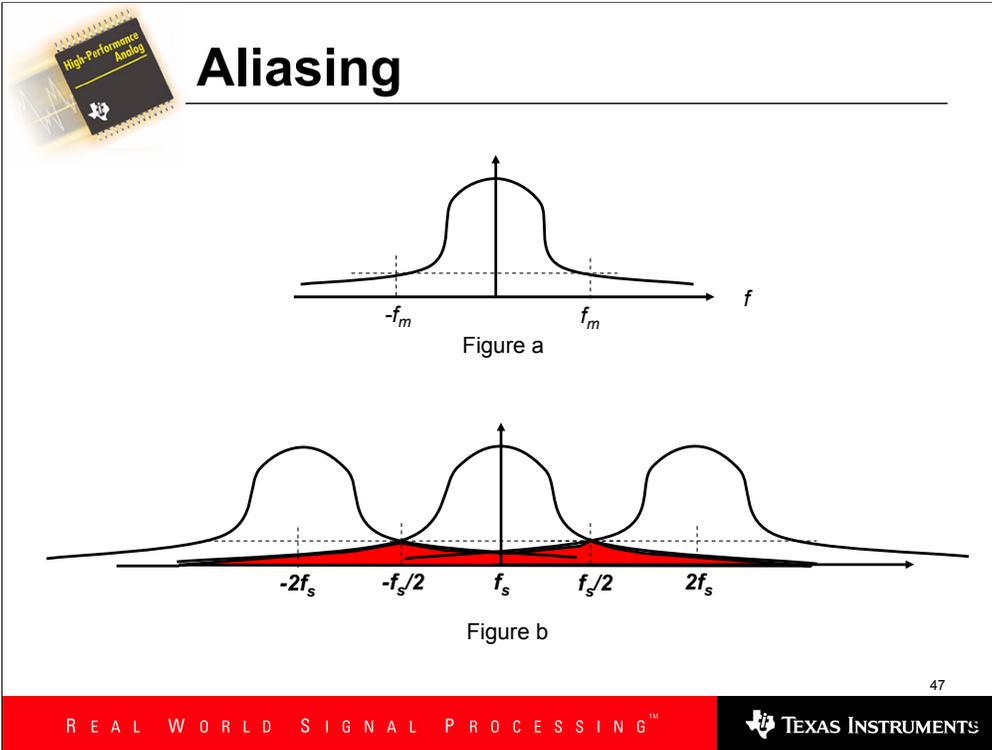
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Since multiplexers are simply switches, and not so much an “active” component, they do not specify offset or gain errors. The main error source with multiplexers is their on-resistance, which is easily handled by driving them with an op amp and buffering the output with an op amp. In our system, the antialiasing filter op amp drives the mux input, and the ADC buffer buffers the output of the multiplexer, so this is not a concern.

Noise, however, can be a problem with multiplexers as the crosstalk and feedthrough of digital signals into the analog path can contribute noise.



In the real world we rarely come across a pure sine wave. Typical signals have a wide spectrum of components, which we can show above - fig. a. Information above or below a certain frequency may not be meaningful to the desired measurements, and so is usually considered surplus. Assuming that f_m is the maximum frequency of interest, we would like to sample at a rate of f_s , where $f_s = 2f_m$.

If we do this, and look at the frequency spectrum, as shown in figure b, we can see that the bands will overlap and produce aliasing in the output signal. To avoid this we must first use a low-pass filter to remove any frequency components above f_m .



Demonstration

Aliasing

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[A live demonstration of aliasing will be shown during this slide]



Helps to Know Your Signal!

- Is it inherently band-limited?
 - Temperature
 - Pressure
 - Physical properties
- Could harmonics of your signal cause aliasing?
- Need filtering to help reduce noise.

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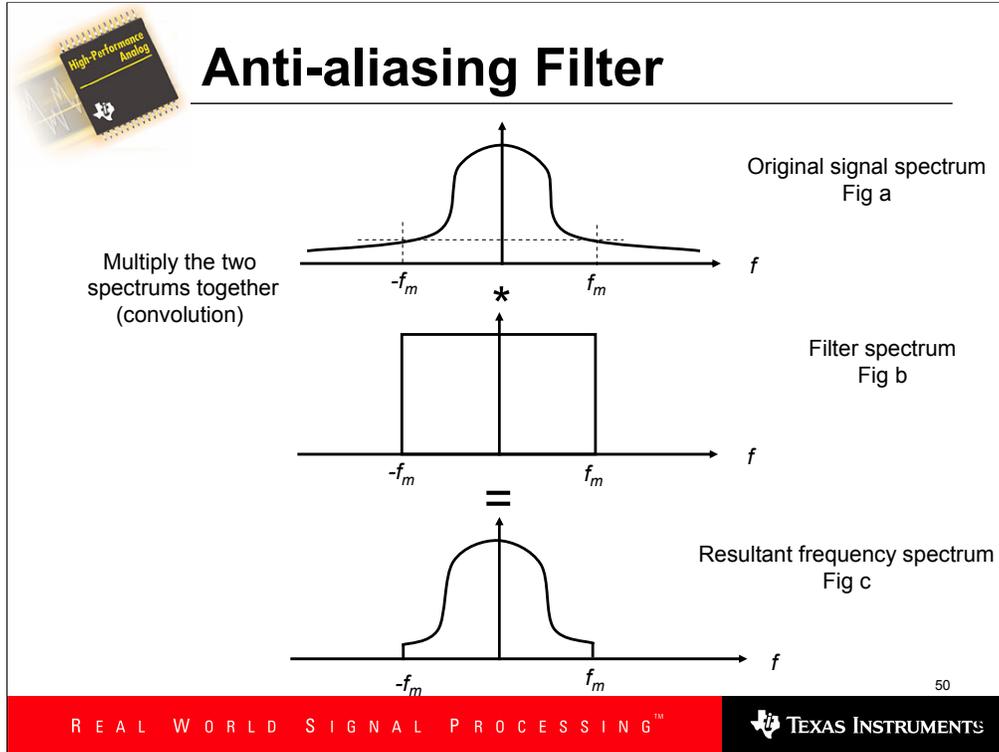
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This implies that we must have some knowledge about the signals that we are trying to digitize and measure. Having some understanding of the nature of the signal we are trying to convert to digital helps us to know what frequencies are of interest to us, and determines f_m , and thus, the required sample rate, f_s .

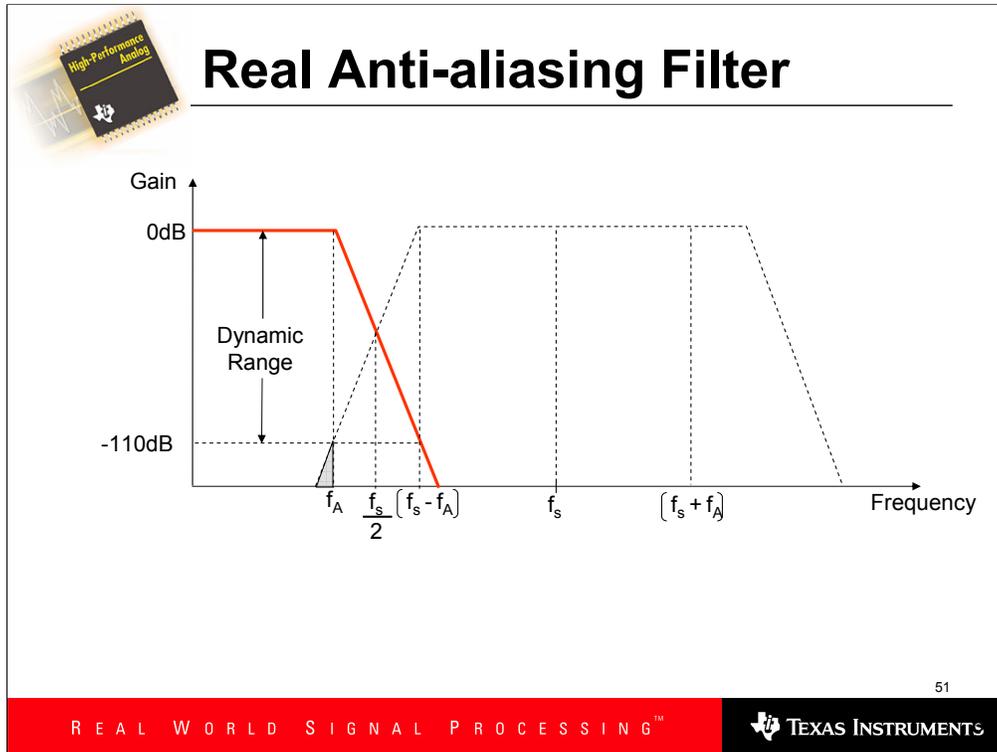
In many cases, the signal we are measuring is inherently band-limited. For example, temperature or pressure signals are usually fundamentally limited in how fast they can change by the physical world. Even in these cases, however, harmonics of the signal of interest could still pose a potential source for aliasing to occur. It is important to consider this possibility when designing a data acquisition system and determining its usable bandwidth.

Even if the signal is inherently band limited, some filtering will be useful, to help eliminate noise and prevent it from affecting the converted signal.



The signal's spectral characteristics and the system's dynamic range requirements must be completely understood before beginning the design of an anti-aliasing filter.

The characteristics of an ideal anti-aliasing filter are shown above in Figure b. It should be flat over the pass-band and zero at all other points. The resulting spectrum would have no frequencies above $f_s/2$.



A real-world anti-aliasing filter will have some rolloff characteristic, and some aliasing may still occur. The filter used then must sufficiently attenuate the out-of-band signals so that their aliased components are below the noise floor of the ADC. Not doing so will degrade the dynamic range in the frequency range of interest available from the ADC.

For a 16-bit system, remembering that $SNR=6.02n + 1.76$ dB, we require an SNR of around 98 dB. At the 18-bit level, this requires 110dB dynamic range.

What this implies is that the point at which the aliasing occurs would result in signals below the resolution of the converter, and thus be benign.



What Filter Cutoff do we Need?

- Mux affects effective sample rate!
 - f_s split across N channels gives effective sample rate of f_s/N :
 - $167\text{kHz}/8 = 20.8\text{kHz/channel}$ sampling
- What if we stay on one channel?
 - Then we could, potentially, sample at 500kHz .

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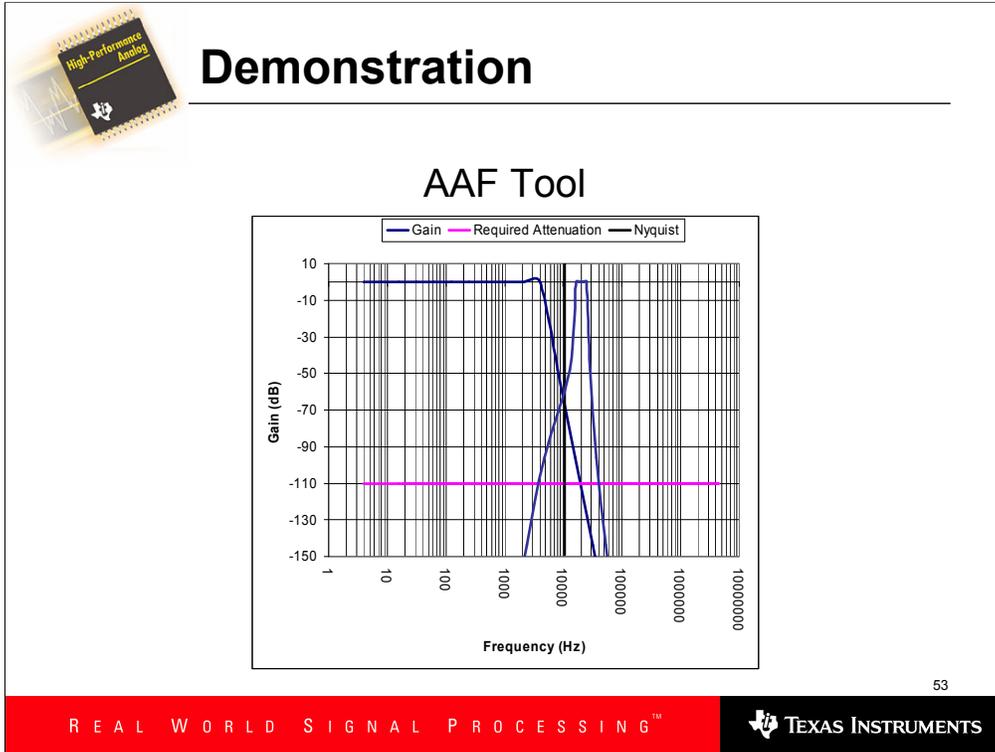
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In the case of our example system, the ADC is sampling at 167kHz. But is this the sample rate to each channel? No, because each of the 8 channels is sampled 1 time out of 8 conversions, so the effective sample rate per channel is $167\text{kHz}/8$, or 20.8kHz.

At best then, each channel can have a bandwidth of half that sample rate, or 10.4kHz. But we can't use all of this bandwidth, because in order to prevent aliasing, we must provide a filter which limits each channel so that at 10.4kHz and above, all the frequencies are attenuated sufficiently so that aliased components will be below the noise floor of the converter.

This assumes, of course, that the system is constantly scanning all eight channels. What if we wanted to stay on just one channel and convert at 500kHz? Then we must provide a filter which attenuates frequencies above 250kHz. A reasonable value might be to plan to digitize frequencies up to 100kHz.



[A live demonstration of the spreadsheet will be shown during this slide]

A simple spreadsheet can help in determining what order of filter may be required for a given resolution of converter and given sample frequency. This graph shows the results of “playing” with the tool, and determining that a 8th order filter with a cutoff at 4kHz will give sufficient attenuation at frequencies above 4kHz to do the job.

Note that there will be some aliasing above the noise floor at frequencies above 4kHz – the region where the two blue lines cross above the magenta line. We are not so concerned with these in our application because we can digitally filter out those frequencies if required (we know they’re above 4kHz). If we didn’t want to do that and had to have all components below the noise floor, a 14 pole filter will be required.



Before or After mux?

- Per channel:
 - Can tailor filtering needs to each channel
 - Complex circuitry repeated
- After mux:
 - Less cost and complexity
 - Limits possibilities for doing only one channel at higher bandwidth
 - Transient response a factor

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Because the filters required to provide sufficient attenuation are complex, and therefore costly, you might be tempted to not duplicate the circuitry on each input channel, and use only one after the multiplexer.

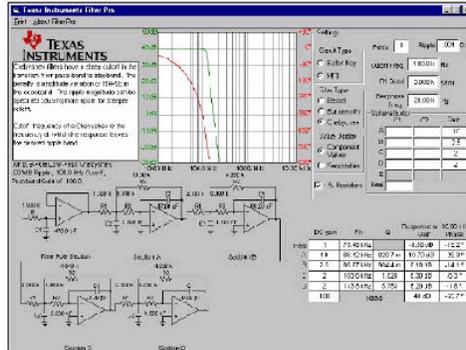
There are tradeoffs associated with this. If in your system you know that you will always be scanning through all the channels, and therefore that no channel can be sampled faster than the f_s/N rate, using one filter after the multiplexer can save cost and complexity. However, this limits the system in that there is no way to then select only one channel and attempt to use it for higher bandwidth.

Furthermore, the transient response of the filter will be an even more important factor, because when switching from one channel to the next, the filter must have time to adjust to this abrupt change, and will require a settling time that may be longer than the next acquisition period. This means that some conversions may not be accurate and would need to be discarded. This affects the overall throughput of the system.



Demonstration

FilterPro



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[A live demo of FilterPro will be shown during this slide]

Texas Instruments makes available a filter design program, FilterPro, which can aid in the design of these filters. Plugging in our requirements found previously, we can realize a circuit for the antialiasing filter we need.



Use FilterPro to Design Circuit!

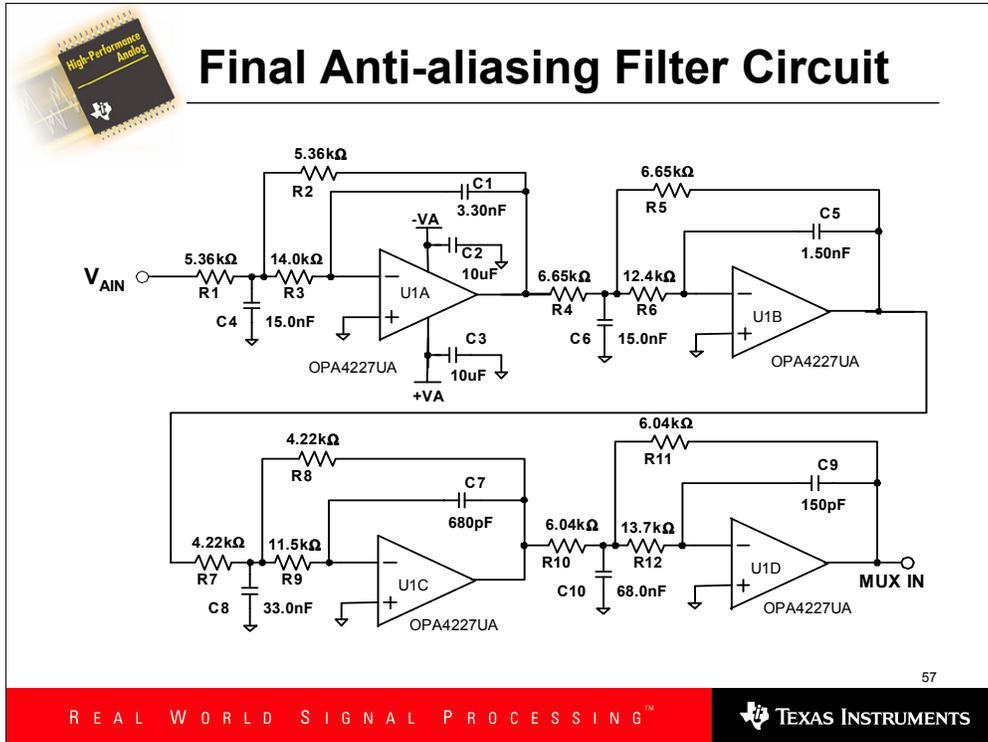
- Caution: check results for reality.
- Note that MFB requires less of the op amps than S-K

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Like any design tool, use the results of FilterPro with caution. FilterPro will happily design a circuit requiring op amps with gain bandwidth products that just don't exist in real op amps today! When this happens, consider changing some parameters or filter requirements. For example, multiple-feedback topologies generally require op amps with less GBW than Sallen-Key filters.



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TEXAS INSTRUMENTS

The 8th order filter circuit is shown here. A quad op amp makes this complex looking circuit relatively small.



Demonstration

Antialiasing Filter

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[A live demo of the designed antialiasing filter will be shown during this slide]



Error Sources in our AAF

- Calculated:
 - Offset including drift: $\pm 100\mu\text{V} = 6.4\text{LSB}$
 - Gain = 4 stages x 0.2%/stage
 - RSS: $\sqrt{4(0.2\%)^2} = 0.4\% = 14.3\text{mV} = 917.5\text{LSB}$

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The errors of the OPA4227 we are using for the antialiasing filter are specified as

Offset: $\pm 100\mu\text{V}$ over the -40 to $+85^\circ\text{C}$ range

Assuming 0.1% resistors again, we can assume the gain error is 0.2% for each stage. Since these may not be correlated, the errors per stage add in a root-sum-square fashion.



Noise

- Noise from UFE

- 4kHz: $\sqrt{(0.2\mu V / 6)^2 + [(8nV / \sqrt{Hz})\sqrt{(4000-10)}]^2} = 506nV_{rms} = 0.03LSB$

- Negligible, even at gains up to 16

- 100kHz: $\sqrt{(0.2\mu V / 6)^2 + [(8nV / \sqrt{Hz})\sqrt{(100000-10)}]^2} = 2.5\mu V_{rms} = 0.16LSB$

- Still small, but at gains >3 could be contributor

- Noise from AAF

- 4kHz: $\sqrt{3\left(2\sqrt{(15nV)^2 + [(3nV / \sqrt{Hz})\sqrt{4000-10}]^2}\right)^2} = 658nV_{rms} = 0.042LSB$

- 100kHz: $\sqrt{3\left(2\sqrt{(15nV)^2 + [(3nV / \sqrt{Hz})\sqrt{100000-10}]^2}\right)^2} = 3.27\mu V_{rms} = 0.2LSB$

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Let's assume then that we're dealing with noise in either a 4kHz or 100kHz bandwidth. Now we can do our noise calculations for the front end and the antialiasing filter.

For the input stage, the INA128 has noise up to 10Hz of 0.2μVp-p, after that it's 8nV/√Hz. This yields a noise contribution of 0.03LSB; at gains up to 16, this would result in less than half an LSB of noise.

The antialiasing filter consists of four stages of op amps with unity gain inverting amplifiers. This means each stage has a noise gain of 2. The OPA4227 used in the filter has noise of 15nVrms to 10Hz, 3nV/√Hz above 10Hz.

From this analysis, noise is not a major problem at this point; however, if the front end has significant gain, the noise from it will begin to contribute a bit.



Selecting Op Amps for Data Converters

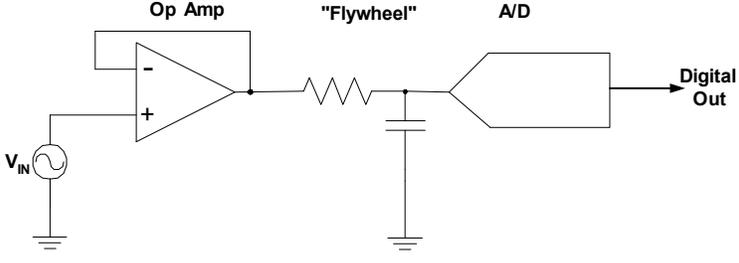
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Input Buffer & Flywheel



- Choosing the right op amp to drive your ADC
- Picking the best RC circuit

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Now that we have our multiplexed signal, we are ready to present it to the A/D converter, through a circuit similar to what is shown here.

The question that often gets asked is, “Which op amp is best for a certain data converter?”. The answer is rarely simple. And that little RC circuit – what is that for? How do you choose the values to use? We’ll examine the answers to those questions in this next section.



Factors of Concern

- DC:
 - Power Supply Rails
 - Size of LSB
 - Offset
 - Drift
- AC:
 - Noise
 - Bandwidth
 - Distortion
 - A/D Architecture

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The main factors to concern ourselves with initially are the power supplies we have available, the size of the least significant bit (LSB) of our converter, and how these relate to our signal range and the error sources that may be introduced by adding an op amp driving the analog-to-digital converter (ADC). The ADC architecture also plays a role in choosing the best driving solution.



Power Supply Rails

- Bipolar
 - $\pm 15V$
 - Implies:
 - $\pm 10V$ signals
- Single Supply
 - +5V
 - +3.3V
 - +1.8V
 - Signal Ranges:
 - +1.5V to +5V

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Bipolar supplies in a data acquisition system used to mean $\pm 15V$, and this implied a $\pm 10V$ signal range. Today, single supply applications are becoming more prevalent, and these can imply signal ranges anywhere from 1.5V to 5V.



LSB Size

- Signal range is critical
 - $\pm 10\text{V}$ is a 20V range
 - 12 bits: $20\text{V}/4,096 = 4.88\text{mV}$ per LSB
 - 16 bits: $20\text{V}/65,536 = 305\mu\text{V}$ per LSB
 - +5V range
 - 12 bits: $5\text{V}/4,096 = 1.22\text{mV}$ per LSB
 - 16 bits: $5\text{V}/65,536 = 76.2\mu\text{V}$ per LSB
 - 24 bits: $5\text{V}/16,777,216 = 298\text{nV}$ per LSB
 - +3.3V range
 - 12 bits: $3.3\text{V}/4,096 = 806\mu\text{V}$ per LSB
 - 16 bits: $3.3\text{V}/65,536 = 50.4\mu\text{V}$ per LSB
 - 24 bits: $3.3\text{V}/16,777,216 = 196\text{nV}$ per LSB

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What this means to your data acquisition system is a decreasing LSB size. Where $\pm 10\text{V}$ gives you an LSB of $305\mu\text{V}$, a 5V signal only gives you $76.2\mu\text{V}$ for a 16-bit LSB. In our 18-bit system, with a 4.096V range, the LSB size is only $15.625\mu\text{V}$.



DC Parameters

- If all you have to work with is $38\mu\text{V}$ ($1/2$ LSB)...
 - Offset Voltage becomes significant
 - Offset from differential bias current, too!
 - OPA335 as an example
 - Single Supply
 - Input offset less than $5\mu\text{V}$
- Temperature Changes
 - If your system has to operate from -25°C to $+75^\circ\text{C}$, you have a 100°C range of temperature change.
 - If all you have is $38\mu\text{V}$ ($1/2$ LSB)...
 - And $20\mu\text{V}$ is used up by offset, then you have $18\mu\text{V}$ allowed for drift, so you can handle $180\text{nV}/^\circ\text{C}$ of drift
- Note: Offset effect may be compensated in the system software!

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Sticking with a 16-bit system, if 0.5LSB is $38\mu\text{V}$, offset and drift become significant for even the best op amps. As LSB sizes shrink, going to autozeroing type op amps may be a solution. Even if the initial offset is low, the temperature drift is likewise affected by these shrinking LSB sizes.



AC Parameters

- Noise - depends upon bandwidth
 - Resistor noise $\sqrt{4KTRB}$
 - 1K ohm resistor = 579nV @ 25°C, 20kHz bandwidth.
 - Current noise
 - Voltage noise
 - Sampling Noise of A/D > Tens of μ Volts
- Distortion
 - THD+N of a 16-bit converter should be better than -98dB, or 0.0011% - again, over the bandwidth of interest.
 - Suitable op amps:
 - OPA627 (Dual Supply)
 - OPA350, OPA134 (Single Supply)
- Single Supply Op Amps
 - As common mode voltage changes, op amp passes through different regions of bias - this results in something similar to crossover distortion

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TEXAS INSTRUMENTS

AC parameters such as noise and distortion are also critical as you try to move them below the noise floor of the converter. With single supply op amps, the input stages often have a region where different bias networks are used, causing a shift in offset as common mode voltage changes. We'll examine this in a bit more detail later, but in an AC sense, this can manifest itself as distortion similar to crossover distortion.



A/D Architecture

- Does the A/D have a buffered input?
 - Adding op amp in front of chopper front end can introduce offset and drift errors.
- Is it a pipeline converter?
 - Does it need high-speed differential inputs?
- Does it have a dynamic input impedance?
 - Is it a CDAC SAR or Delta Sigma?
 - Conversion speed can significantly change requirements
 - Need to charge input cap to 1/2LSB accuracy in acquisition time
 - Old-style SAR
 - Same problem, different reason!
 - Changing current requirements provide dynamic input impedance

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Before going further with this topic, it's important to know the A/D converter you plan to use.

For example, some A/D converters have an input buffer amplifier already, and an external one may not be necessary. In some cases, the internal buffers are chopper-stabilized, and adding any kind of external amplifier would simply reduce the effectiveness of the chopper.

Pipeline converters commonly used in high-speed communications applications have their own special driving requirements, usually requiring a differential input. We'll look at these a bit later.

Successive approximation register (SAR) converters have special needs for driving their inputs. Because of the dynamic input impedance of these converters, they present a difficult load to the driving op amp.

We'll look at each of these architectures from an input buffer standpoint next, in turn.



High Resolution – Delta Sigma

- **Signal Conditioning**
 - Usually no amplifier
- **Offset and gain errors**
 - Treated with calibration techniques
- **Reference**
 - Usually has higher input impedance than SAR

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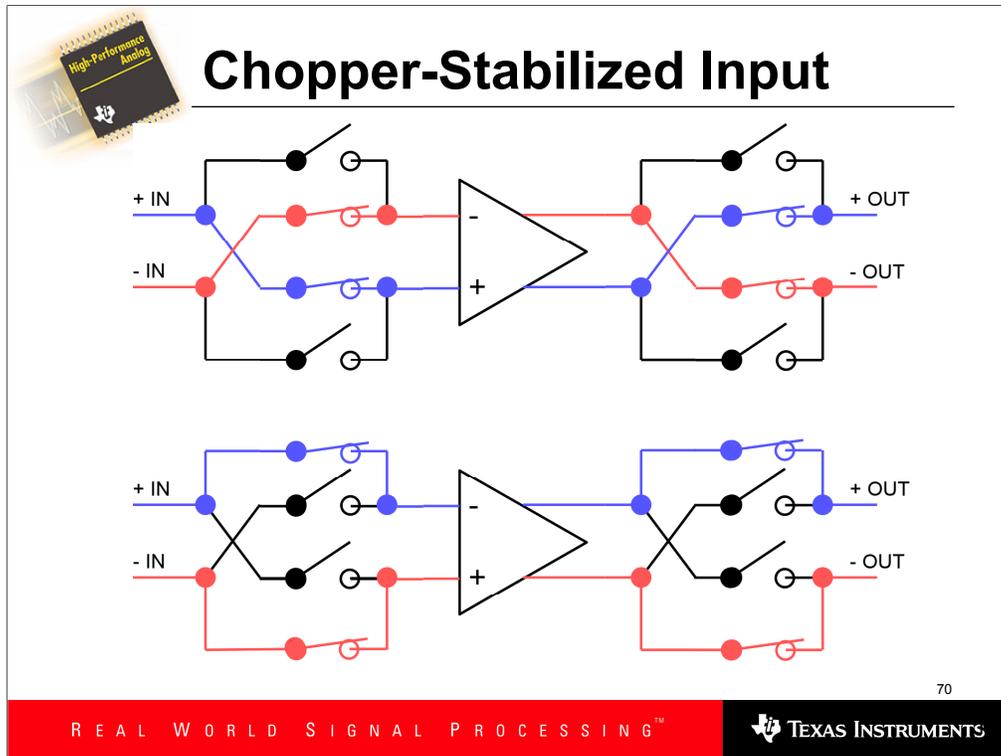
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TI's delta-sigma line of A/D converters are designed to interface directly to sensors, and some feature more specialized signal conditioning interfaces. In particular, many of these converters have a chopper-stabilized front end.

Offset and gain errors can often be removed by using a self-calibration technique available in these converters. This will be discussed later in this seminar.

While our focus is on the input buffer amplifier, converter reference inputs often need buffering as well. Since the delta-sigma converters generally have reference inputs with higher input impedances, choosing an op amp for this function is not too demanding.



There are several methods for implementing a chopper-stabilized input. This is probably the easiest to visualize, but not the simplest to build.

Imagine that you have an offset in this differential op amp that adds 1 mV to the +input. In the top diagram that 1 mV appears on the +OUT signal.

In the bottom circuit the 1 mV is added to the $-OUT$ signal. Since it is alternately added to the positive and then the negative output, the net result is that on average the 1 mV offset doesn't appear on the output. This works particularly well for delta-sigma converters since they integrate the difference signal output.

Drift is a phenomenon where the amount of offset changes with time. The actual value of the offset doesn't matter in the chopper-stabilized circuit. Therefore, the fact that it might drift or change over time doesn't affect the result.

Adding any type of external op amp to a front end like this doesn't provide the opportunity for the chopper stabilization to cancel the offset and drift of the external amplifier. Generally, ADCs which feature this type of input also have internal programmable gain amplifiers, so no external gain is needed. Resist the temptation to add external op amps to these types of converters!



High Speed – Pipeline Topology

Pipeline converters fit high-speed applications (5MHz to 100+MHz). The question for these converters is:

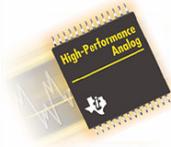
“How do I interface my incoming IF signal to the converter to get the best possible performance results?”

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 TEXAS INSTRUMENTS

Let's now look at driving pipeline converters. This architecture of ADC is used most commonly in high-speed communications applications, where AC performance is paramount, and DC requirements are more forgiving. In a typical digital radio application, an intermediate-frequency (IF) signal would be sent into an ADC for direct digital downconversion. How best to drive an op amp for this type of ADC?



ADC Interface Solutions for High-Speed

Identify an appropriate interface configuration!

Simple Selection Matrix:

	Single-Ended Input	Differential Input
AC-coupled	High Amplitude Signal Required	More Complex Circuit
DC-coupled	Limited Use for This Application	Limited Use for This Application

Note: 'SE' or 'Diff' refers to the immediate A/D input configuration

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AC-Coupled

Single-Ended Input

Bandlimited IF does not contain a dc-component so it is ac-coupled.

Single-ended input requires twice the signal amplitude out of the driver to match ADC full-scale.

ac-coupling eliminates common-mode voltage (V_{cm}) between the driver op amp and the A/D.

Differential Input

More complex driver circuit than single-ended.

Reduced signal amplitude leads to improved distortion due to increased headroom for the driver amps.

Offers common-mode noise and even-order harmonic rejection

DC-Coupled

Single-Ended Input

Limited use because input bandwidth does not include LF or DC.

Differential Input

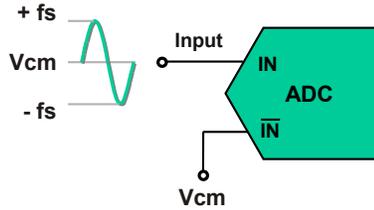
Differential I/O amps may be used depending on input frequency range.



ADC Interface Solutions

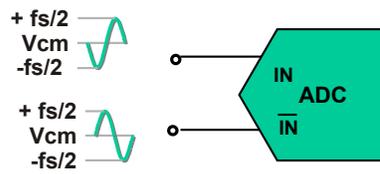
Principle Configuration Choices

Single-Ended Input



Requires full input swing from $+fs$ to $-fs$
2x the swing compared to differential
input signal at IN typically requires a
common-mode voltage for bias
Input IN- also requires a V_{cm} for correct
dc-bias

Differential Input



Combined Differential inputs result in
full-scale input of $+fs$ to $-fs$
Each input only requires 0.5x the
swing compared to single-ended
Both inputs require a V_{cm} for correct
dc-bias

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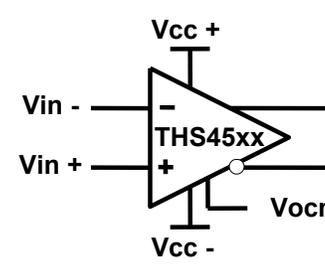
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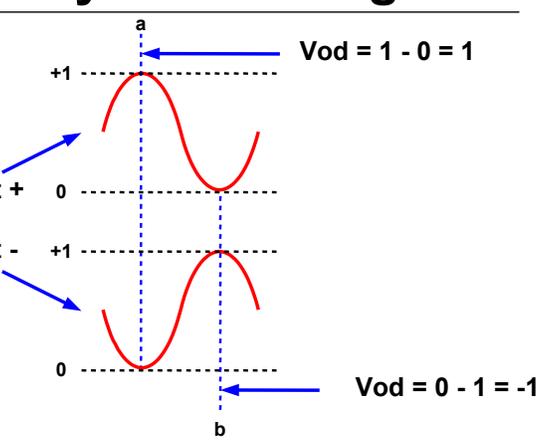
TEXAS INSTRUMENTS

Most CMOS pipeline ADCs are operated on a single-supply. This typically requires the inputs to be biased to a common-mode voltage, V_{cm} , which is typically set to mid-supply ($+V_s/2$). The converter inputs are often provided in differential form, but can be driven from the source in two ways: either single-ended or differential. Both configurations have their advantages and disadvantages.



Increased Dynamic Range





Differential output results in $V_{od\ p-p} = 1 - (-1) = 2X$ SE output

Lower power supply requirements

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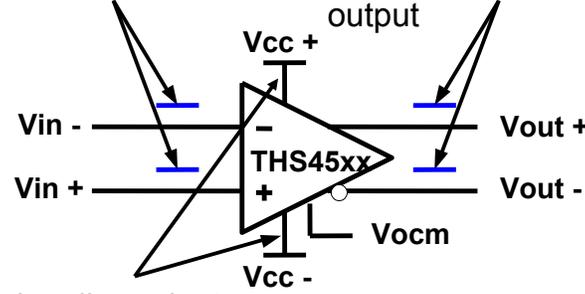

Due to the change in phase between the differential outputs, the dynamic range increases by 2X over a single-ended output with the same voltage swing. This lowers the power supply requirements for a given output voltage swing.



Common Mode Noise Rejection

Differential signaling rejects common mode noise at the input

Differential signaling rejects common mode noise at the output



Differential signaling rejects common mode noise from the power supply

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Invariably when signals are routed from one place to another, noise is coupled into the wiring. In a differential system, keeping the transport wires as close as possible to one another makes the noise coupled into the conductors appear as a common-mode voltage. Noise that is common to the power supplies will also appear as a common-mode voltage. Since the differential amplifier rejects common-mode voltages, the system is more immune to external noise. The figure shows the common-mode noise immunity of a fully differential amplifier pictorially.



Differential Interface

- **Theoretically, differential signaling results in cancellation of even-order harmonics.**

This would be ideal since 2nd HD is usually dominant.

- **In reality, complete suppression is not achievable. However, design optimization includes best possible matching of:**
 - **Components (consider parasitics)**
 - **Layout; i.e. symmetry between signal paths**

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Reduced even order harmonics

Use power series expansion:

Non-inverted output:

$$V_{out+} = k_1(V_{in}) + k_2(\cancel{V_{in}})^2 + k_3(V_{in})^3 + \dots$$

Inverted output:

$$V_{out-} = k_1(-V_{in}) + k_2(\cancel{-V_{in}})^2 + k_3(-V_{in})^3 + \dots$$

Differential output:

$$V_{od} = (V_{out+}) - (V_{out-}) = 2k_1V_{in} + 2k_3V_{in}^3 + \dots$$



Differential signal contains no even order terms

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TEXAS INSTRUMENTS

Expanding the transfer functions of circuits into a power series is a typical way to quantify the distortion products. In general $V_{out} = k_1V_{in} + k_2V_{in}^2 + k_3V_{in}^3 + \dots$, where k_1, k_2, k_3 , etc. are some constants. If the input to this circuit is a sinusoid, trigonometric identities show the quadratic, cubic and higher order terms give rise to 2nd, 3rd and higher order harmonic distortion. In similar manner, if the input is comprised of two sinusoidal tones, trigonometric identities show the quadratic and cubic terms give rise to 2nd, 3rd and higher order intermodulation distortion.

In a fully differential amplifier, the odd order terms retain their polarity, but the even order terms are always positive. When the differential is taken the even order terms cancel.



Implementation of Differential Circuits

- **Active = Op Amps**
 - VFA, CFA
 - Good for providing gain
 - I/O impedance isolation
 - Op Amps have 'SE' I/O
 - Can add noise and distortion
 - Supply sets headroom and common-mode limit
 - DC- and AC-coupling
- **Passive = Transformer**
 - Simple SE to Diff conversion
 - Step-up types for 'noiseless' gain
 - Common-mode voltage can easily be added to center-tap
 - Need impedance matching
 - Bandpass response
 - AC-coupling only

Actual circuit implementations may use a combination of both!

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Driver Op Amp Selection

Observation:

Performance levels of high-speed A/Ds are high and finding suitable driver op amps with sufficiently low distortion is difficult!

Current-Feedback (CFA) vs. Voltage-Feedback Amplifier (VFA):

- CFAs maintain good distortion up to very high frequencies
- CFAs typically have good IP3 performance due to high slew rate
 - Good ‘prerequisites’ for IF-applications/Undersampling
- VFAs typically have superior distortion performance at baseband frequencies

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TEXAS INSTRUMENTS

The op amp used to drive the ADC should have better distortion and noise performance than the A/D converter to preserve the ADC performance. When differential inputs require two op amps, a dual op amp may offer better matching (over temperature) than two singles. Additionally, the output voltage swing of the op amps should accommodate the full-scale input range of the A/D converter to achieve full dynamic range performance. Most high-speed A/D converters use a single supply, but dual supplies are often required to power input drive op amps.

The transient response of the driver circuitry can have a significant affect on the performance of high-speed converters, so the drive circuitry must insure that transient currents and voltages at the output of the amplifiers are sufficiently settled before the A/D converter acquires the input signal sample. The bandwidth should be adequate to prevent attenuation of higher frequencies.



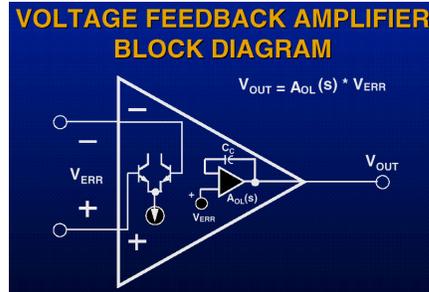
Voltage Feedback Op-Amps

Advantages:

- “Error” signal is a voltage
- Input stage is matched or symmetric
- High levels of DC accuracy
- OPA640, THS4271

Disadvantages:

- Bandwidth is dependent on closed loop gain
- Some are not stable in unity gain (OPA687)



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Current Feedback Op-Amps

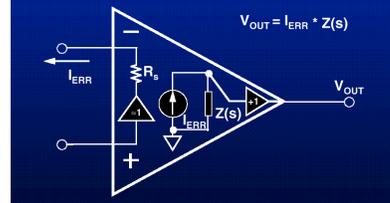
Advantages:

- “Error” signal is a current
- Bandwidth is independent of closed loop gain
- Higher speed
- Always unity gain stable
- OPA642, THS3202

Disadvantages:

- Input stage is not symmetric
- Not as accurate
- Higher bias current
- More current noise

**CURRENT FEEDBACK AMPLIFIER
BLOCK DIAGRAM**



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Driver Op Amp Selection

- **Important Considerations**
- **Review Performance Curves:**
 - **Distortion vs. Frequency and,**
 - **Distortion vs. Amplitude and Load**
 - Op amp specs typically refer to a 100- Ω load, while the input impedance of an A/D converter is in the range of 500 Ω +
 - This will improve the distortion
- **Output impedance vs. frequency**
- **High slew rate, fast settling**
- **Stability with capacitive load**
- **Output voltage swing must match A/D fs-input**
- **Single- or dual-supply system?**

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Several factors have to be considered when selecting the driver op amp. Most data sheets provide specifications and/or typical performance curves for distortion (THD) over a range of frequencies. Almost all high-speed op amps are specified in a 50- Ω environment, thus the standard load condition for the typical performance curves is double-terminated 50- Ω or 100- Ω total load.

The input impedance of a pipeline A/D converter is much higher than 100 Ω , typically, several hundred Ohms, and this higher load condition usually leads to improved distortion performance of the driver amplifier.

The implication is that the pipeline A/D converter has a switched capacitor T&H in its input. This means two things: first, the op amp has to drive a capacitive load; and second, the input impedance of the converter is dynamic.

Z_{IN} is a function of sampling rate, and Z_{IN} declines with an increase in f_s .



Ultra-Wideband, Current Feedback Amplifier OPA685

Features:

- Gain = +2, Bandwidth (900 MHz)
- Gain = +8, Bandwidth (420 MHz)
- Wide Output Voltage Swing: ± 3.6 V
- 90-mA drive capability enables it to drive 2 mixers
- Low Power: 129 mW (± 5 V)
- Low Disabled Power: 3 mW

Applications:

- Wideband ADC Driver
- Cost Effective IF Amplifier
- LO Buffer

Device	V _S (V)	BW _{-3dB} (MHZ)	SR (V/ μ s)	THD _{1MHz} (dB)	IP3 (dBm)	V _{n 10MHz} (nV/ \sqrt Hz)	T _{s(0.1%)} (ns)
OPA685	5-12	1200	4200	80	40	1.7	3

Mini Data Sheet at ± 5 V, 25°C, typ, I_Q per channel

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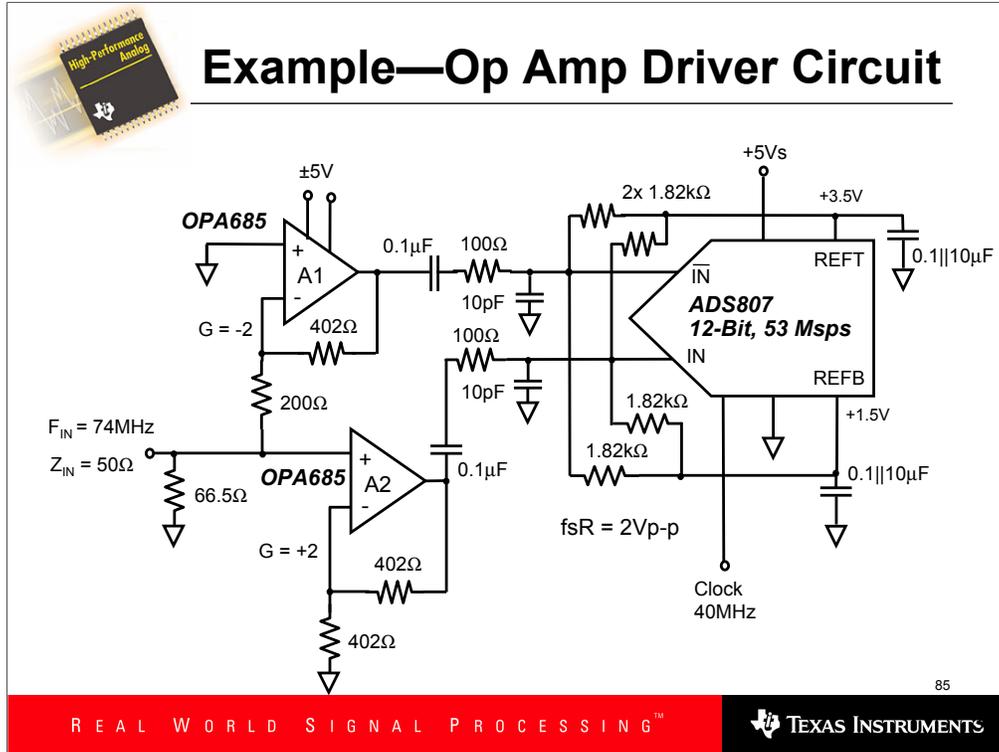
High-Speed A/D Converter Products

Model	Bits	Speed (MSPS)	A-BW (MHz)	SFDR@ 10MHz	SNR @10MHz	Jitter (rms)
ADS826	10	60	300	73dB	58dB	1.2ps
ADS828	10	75	300	68dB	57dB	1.2ps
ADS805	12	20	270	74dB	68dB	2ps
ADS807	12	53	270	82dB	68dB	1.2ps
ADS809	12	80	500	68dB	65dB	0.25ps
ADS5421	14	40	500	83dB	75dB	0.25ps
ADS5422	14	60	500	82dB	74dB	0.25ps

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A selection of high-speed pipeline A/D converters suitable for use in undersampling applications.

Complete information can be found on TI's web site: www.ti.com



This undersampling configuration digitizes a 74-MHz input signal with a 40-MHz sampling rate. The input signal is converted down to a 6-MHz fundamental.

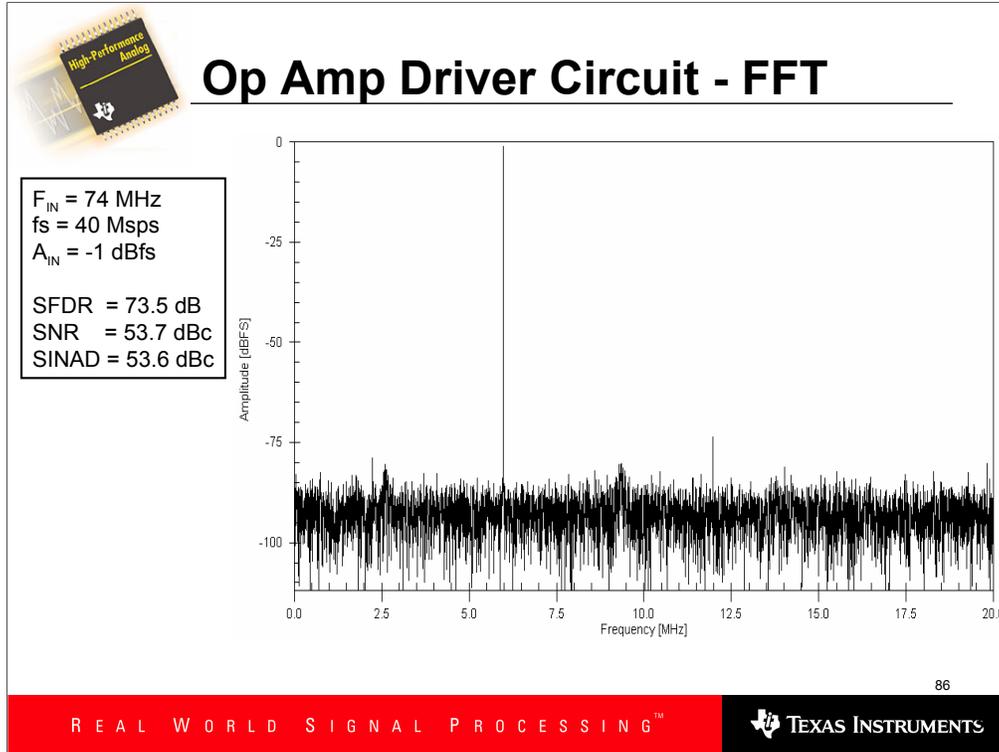
For this circuit example, the OPA685 was chosen to drive the inputs of the ADS807, a 12-bit, 53-Msps pipeline converter.

The OPA685's outputs are ac-coupled to the converter. This allows the input signal amplitude to be centered around 0 V, or mid-supply, in order to maintain a symmetric headroom and consequently minimize the distortion.

For the A/D converter inputs, the necessary common-mode voltage is derived from the internal references. The mid-points of the two-resistor strings (2x1.82k) produce a +2.5-V common-mode voltage.

The amplifiers are set for a signal gain of 2. However, due to their different configuration, their noise gains are not matched which could potentially degrade the performance.

The simple RC filter (100 Ω , 10 pF) provides some attenuation of the high-frequency noise.



This is an FFT of the previous driver circuit, in which the OPA685 is used to drive the ADS807. Even though attention was paid to the symmetry of the differential signal path, the second harmonic continues to be the dominant spur.



Test Results

A_{IN} (dBfs)	SNR (dBc)	SINAD (dBc)	SFDR (dB)
-1	53.7	53.6	73.5
-3	53.6	53.5	77.7
-6	53.3	53.1	78.6
-12	51.8	51.7	86.1
-20	47.2	47.0	85.2

Conditions:

$f_{in} = 74$ MHz, $f_{in}' = 6$ MHz, $f_{sR} = 2$ Vp-p

Input signal filtered with a 80 MHz, 9th order passive BP (TTE)

Clock = 40 MHz,

$V_s = +5$ V, $V_{DRV} = +3$ V

Driver amp: OPA685, Gain 2

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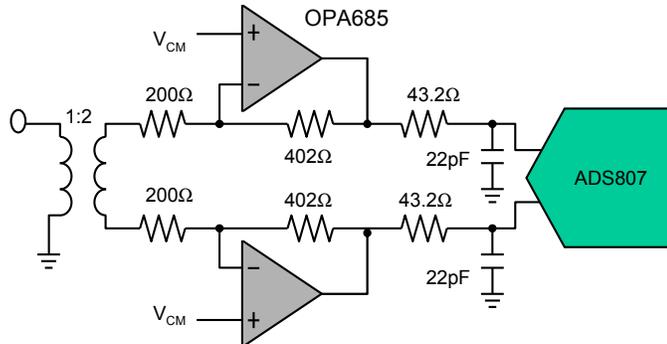
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Listed here in tabular form are more test results from the OPA685 driver circuit. Note that the SNR and SINAD are relative to the fundamental (in dBc) and remain fairly constant. It also shows that an improvement in the dynamic range (SFDR) can be realized by reducing the amplitude of the input signal.



Differential ADC Driver Solutions Two High-Speed Amplifiers



- Noise Gain Matched
- Parts Are Symmetrical
- Excellent Distortion Performance

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TEXAS INSTRUMENTS

Compared to the previously shown circuit, this example improves upon the matching of the differential signal. A transformer provides SE-to-Diff conversion and it is combined with the OPA685 current-feedback amplifier. This allows for both amplifiers to operate in the same inverting configuration resulting in improved noise gain (bandwidth) matching.

The op amps are dc-coupled to the ADS807. The required common-mode voltage (V_{cm}) is applied to the non-inverting inputs of the OPA685s to correctly bias the ADC inputs.

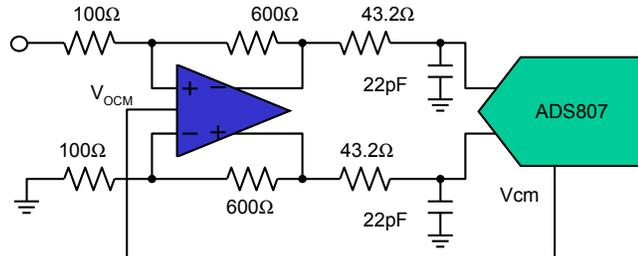
Using a step-up transformer in the input helps reduce the gain requirements for the driver op amps.

This circuit can achieve excellent distortion performance up to very high frequencies (IF).



Differential ADC Driver Solutions

Fully Differential I/O Amplifier



- Ideal Baseband Driver Solution:
 - No transformer
 - VCM matched to ADC
 - Good even-order harmonic rejection
 - Easily configured for gain and low-pass filter

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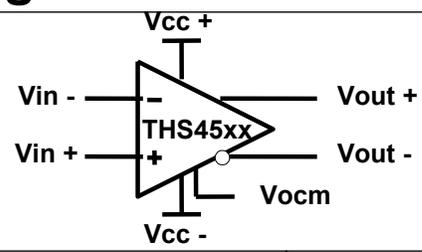
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TEXAS INSTRUMENTS

Fully differential input/output amplifiers have recently become available. These new high-speed devices are particularly suited for driving differential A/D converters. Their features enable a very effective applications solution where dc-coupling is required.



Voltage Definitions



	Differential	Common Mode
Input voltage definition	$V_{id} = (V_{in+}) - (V_{in-})$	$V_{ic} = \frac{(V_{in+}) + (V_{in-})}{2}$
Output voltage definition	$V_{od} = (V_{out+}) - (V_{out-})$	$V_{oc} = \frac{(V_{out+}) + (V_{out-})}{2}$
Transfer function	$V_{od} = a(f) \times V_{id}$	$V_{oc} = V_{ocm}$

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To understand how a fully differential amplifier behaves, it is important to understand the voltage definitions that are used to describe the amplifier. The diagram shows a fully differential amplifier and its input and output voltage definitions.

Input Voltages

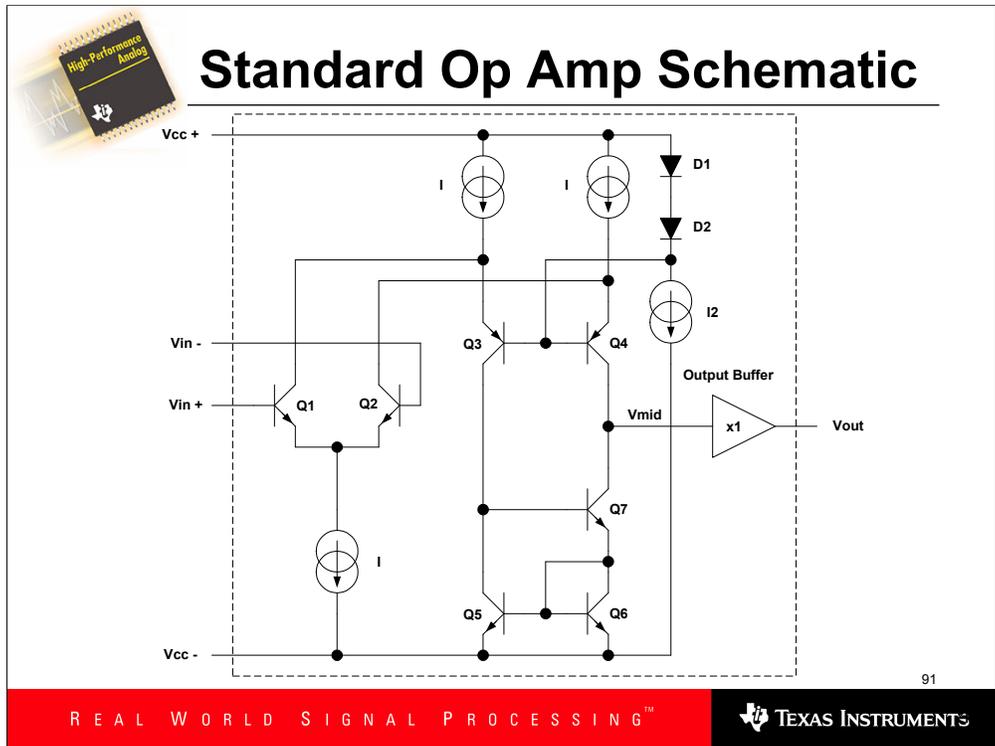
The voltage difference between the plus and minus inputs is the input differential voltage, V_{id} . The average of the two input voltages is the input common-mode voltage, V_{ic} .

Output Voltages

The difference between the voltages at the plus and minus outputs is the output differential voltage, V_{od} . The output common-mode voltage, V_{oc} , is the average of the two output voltages.

Transfer Functions

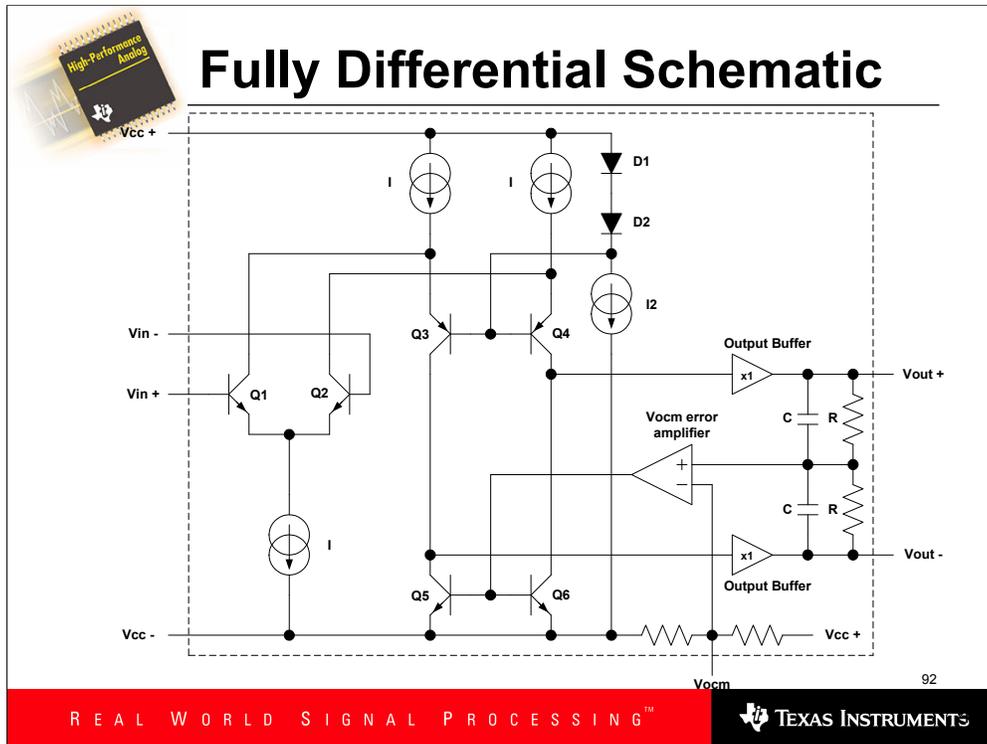
$a(f)$ is the frequency dependent open loop gain of the main differential amplifier so that $V_{od} = a(f) \times V_{id}$. V_{oc} is controlled by the voltage at V_{ocm} .



A simplified schematic of a high-speed op amp is shown. V_{cc+} is the positive power supply input, and V_{cc-} is the negative power supply input. V_{in+} and V_{in-} are the signal input pins, and V_{out} is the signal output. The op amp amplifies the differential voltage across its input pins to generate the output. By convention, the input voltage is the difference voltage, $V_{id} = (V_{in+}) - (V_{in-})$. It is amplified by the open loop gain of the amplifier to produce the output voltage, $V_{out} = a(f)V_{id}$, where $a(f)$ is the frequency dependent open loop gain of the amplifier.

The input pair is balanced so the collector currents are equal when the input differential voltage is zero, $I_{c1} = I_{c2}$. Applying a voltage across the input pins causes $I_{c1} \neq I_{c2}$.

$Q3$ and $Q4$ folds the difference current, $I_{c1} - I_{c2}$, from the input stage into the Wilson current mirror formed by $Q5$, $Q6$, and $Q7$. The mirror presents high impedance to the difference current and generates the voltage at V_{mid} , which is then buffered to the output.



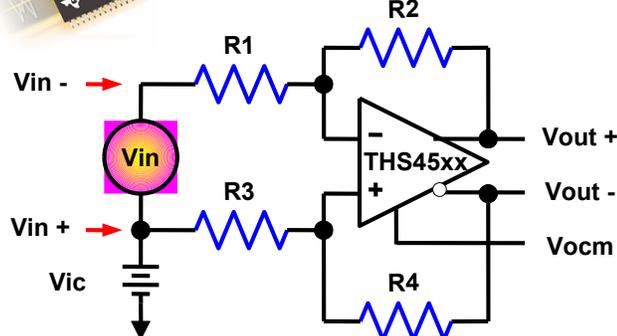
A simplified version of an integrated fully differential amplifier is shown. Q1 and Q2 are the input differential pair. In a standard op amp, the difference current from the input differential pair is used to develop a single-ended output voltage. In a fully differential amplifier, the difference current is used to develop differential voltages at the high impedance nodes at the collectors of Q3/Q5 and Q4/Q6. These voltages are then buffered to the differential outputs Vout + and Vout -.

To first order approximation, voltage common to Vin+ and Vin- does not produce a change in the current flow through Q1 or Q2 and thus produces no output voltage – it is rejected. The output common-mode voltage is not controlled by the input. The Vocm error amplifier maintains the output common-mode voltage at the same voltage applied to the Vocm pin, by sampling the output common-mode voltage, comparing it to the voltage at Vocm, and adjusting the internal feedback. If not connected, Vocm is biased to the midpoint between Vcc + and Vcc - by an internal voltage divider.

Note: there are two feedback paths around the main differential amplifier, and there is also the Vocm error amplifier.



Differential to Differential



$$\beta_1 = \frac{R_3}{R_3 + R_4}$$

$$\beta_2 = \frac{R_1}{R_1 + R_2}$$

$$V_{in} = (V_{in+}) - (V_{in-})$$

$$V_{out} = (V_{out+}) - (V_{out-})$$

Generalized Gain Formula

$$V_{out} = \frac{2[(V_{in+})(1 - \beta_1) - (V_{in-})(1 - \beta_2) + (V_{ocm})(\beta_1 - \beta_2)]}{(\beta_1 + \beta_2)}$$

Symmetrical Case $\beta_1 = \beta_2$ $R_1 = R_3 = R_G$ & $R_2 = R_4 = R_F$ \Rightarrow $\frac{V_{out}}{V_{in}} = \frac{1 - \beta}{\beta} = \frac{R_F}{R_G}$

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In a fully differential amplifier, there are two feedback paths possible in the main differential amplifier, one for each side. This naturally forms two inverting amplifiers, and inverting topologies are easily adapted to fully differential amplifiers. The figure shows a fully differential amplifier with negative feedback around both sides.

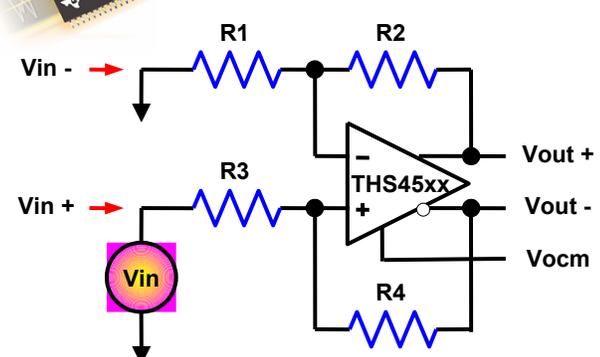
Symmetry in the two feedback paths is important to have good CMRR performance. CMRR is directly proportional to the resistor matching error – 0.1% error results in 60dB of CMRR.

Signals at V_{in} appear as differential inputs to the amplifier, and are amplified to the output. Common mode inputs like V_{ic} are rejected by the amplifier.

The V_{ocm} error amplifier is independent of the main differential amplifier. The action of the V_{ocm} error amplifier is to maintain the output common-mode voltage at the same level as the voltage input to the V_{ocm} pin. With symmetrical feedback, output balance is maintained, and V_{out+} and V_{out-} swing symmetrically plus and minus from the voltage at the V_{ocm} input.



Single Ended to Differential



$$\beta_1 = \frac{R_3}{R_3 + R_4}$$

$$\beta_2 = \frac{R_1}{R_1 + R_2}$$

$$(V_{in+}) = V_{in}, \quad (V_{in-}) = 0$$

$$V_{out} = (V_{out+}) - (V_{out-})$$

Generalized Gain Formula

$$V_{out} = \frac{2[(V_{in})(1 - \beta_1) + (V_{ocm})(\beta_1 - \beta_2)]}{(\beta_1 + \beta_2)}$$

Symmetrical Case $\beta_1 = \beta_2$

$R_1 = R_3 = R_G \text{ \& \ } R_2 = R_4 = R_F$

$$\frac{V_{out}}{V_{in}} = \frac{1 - \beta}{\beta} = \frac{R_F}{R_G}$$

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In the past, generation of differential signals has been cumbersome. Different means have been used, requiring multiple amplifiers, transformers and dc blocking capacitors. The integrated fully differential amplifier provides a more elegant solution. The figure shows an example of converting single ended signals to differential signals.

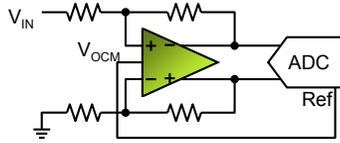
Signals at V_{in} appear as differential inputs to the amplifier. This may include unwanted dc offsets.



TI's Fully Differential Amplifiers

• Key Benefits

- Simplifies Single-Ended to Differential Conversion
- Can be DC Coupled
- Vocm pin sets output Common-mode
- Powerdown feature on all devices
 - THS41x0
- THS412x in CMOS process
 - Low Power applications, 3V only
 - Rail-to-rail output
- THS413x for low noise applications



Part	BW _(-3dB)	SR	t _s (0.1%)	THD _(1MHz)	V _n	I _Q	V _{IO}	I _S	V _S	Package
	(MHz)	(V/μs)	(ns)	(dBc)	(nV/√Hz)	(mA)	(mV)	(mA)	(V)	
THS4120 / 4121	100	43	82	-71	3.7	100	8	5.6	3.0 - 3.6	D, DGN
THS4130 / 4131	150	51	78	-80	1.3	85	2	14	+5 - ±15	D, DGN
THS4140 / 4141	160	450	96	-79	6.5	85	7	15	+5 - ±15	D, DGN
THS4150 / 4151	150	650	53	-84	7.6	85	7	17.5	+5 - ±15	D, DGN

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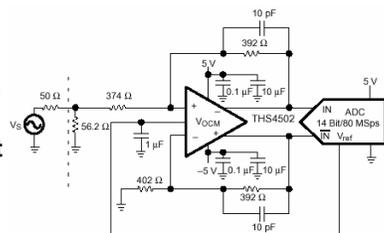
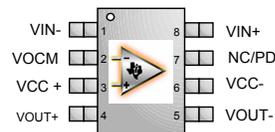


THS4500/01, THS4502/03

Fully Differential Amplifiers

Features

- Differential Input / Differential Output
- Differential Reduced Second Harmonic Distortion
- THS4500/02/04 has Powerdown mode
- 8-pin SOIC, MSOP available now
 - Leadless MSOP soon to come
- THS4500/01/04/05 with Common-mode range to negative rail for single-supply applications
- THS4504/05 is sampling now, release in August



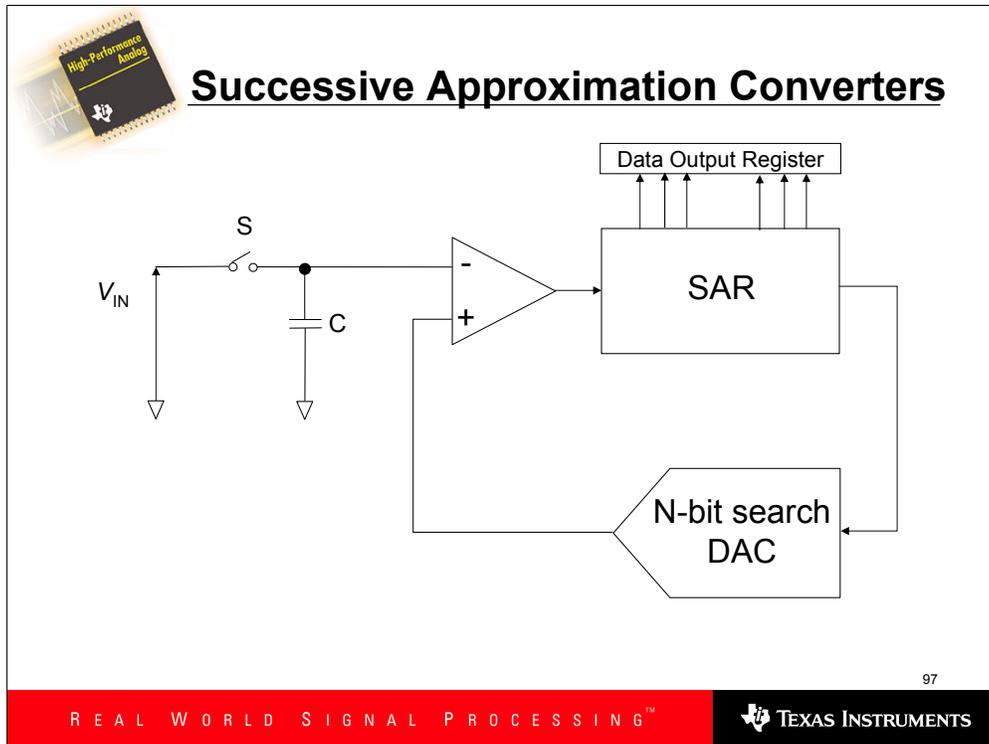
Compatible to:

- AD8138, AD8132, AD8131(G=2)

Part	BW _(-3dB) (MHz)	SR (V/μs)	V _{ICR(+/-5V)} (V)	THD _(30MHz) (dBc)	IMD _{3(50MHz)} (dBc)	V _n (nV/√Hz)	I _o (mA)	V _o (mV)	I _s (mA)	V _s (V)
THS4500 / 4501	370	2800	-5.5 - +2.5	-70	-84	7	120	4	23	+5 - ±5
THS4502 / 4503	370	2800	-3.7 - +3.7	-74	-84	6.8	120	1	23	+5 - ±5
THS4504 / 4505	260	1800	-5.7 - +2.6	-65	-78 (@20)	8	120	4	18	+5 - ±5 ₉₆

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The most popular and versatile converter is the Successive Approximation Register (SAR) type. These converters work by comparing the analog signal voltage to known fractions of the full scale voltage and setting or clearing bits in a data register as a consequence.

Modern SARs use a C-DAC to successively compare bit combinations, set or clear the corresponding bits in a data register, and they also tend to have an integrated sample/hold function.

A typical SAR conversion cycle has two phases; a sampling phase and a conversion phase.

During the sampling phase, the analog input signal is allowed to charge the ADC's Sample-and-Hold (S/H) capacitor to a level proportional to the analog input.

Conversion begins immediately following the sampling phase. Conversion successively compares the unknown value of the charge stored in the S/H capacitor to known fractions of charge. After each comparison, logic on the ADC determines if the unknown charge is greater or smaller than the known fractional charge. The process will be like this

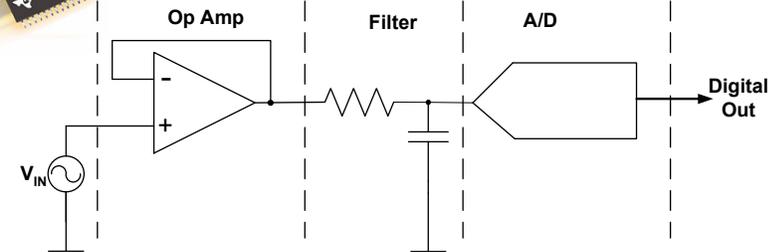
- $x > 1/2 \text{ FS} ? - Y - \text{ set the corresponding bit}$
- $x > 3/4 \text{ FS} ? - N - \text{ clear the corresponding bit}$
- $x > 5/8 \text{ FS} ? - Y - \text{ set the corresponding bit}$
- etc

At the end of the process the data register will contain a binary value proportional to the value initially placed on the S/H capacitor. The user reads this value out as converted data.

As shown in the diagram above, these converters rarely provide any type of built-in input buffer amplifier. So choosing an amplifier to match up to these converters is what we will examine next.



System Design Variables



<p><u>Op Amp</u></p> <p>Noise, Signal BW, CMV Range, Slew Rate, Output Impedance, Settling Time, Load Transient, Gain Error, Power Supply, V_{OS} vs CMV Input, Circuit Topology, THD + Noise</p>	<p><u>Filter</u></p> <p>Noise Filtering, Load Isolation, Charge Bucket</p>	<p><u>ADC</u></p> <p>Acquisition Time, Architecture, Power Supply, Data Rate, Resolution, ADC Input, ADC Ref In</p>
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A typical input stage for a SAR-type ADC is shown above. Some type of buffer amplifier is used, driving a small RC-filter prior to the input to the ADC. We'll examine just what these elements do for us in the next few slides.

As you can see, for each part of this circuit, there are many considerations, all of which potentially affect the accuracy and resolution of the system. In choosing components to use in such a system, you must be mindful of all of these considerations.



Design Procedure Will Use

- Data Sheet Parameters 
- Factory Only Parameters 
- Rules of Thumb 
- Testing 

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We will now discuss a design procedure to assist in choosing the right op amp to drive a particular SAR ADC, and choose the values for the RC filter preceding the ADC.

Many articles have been written about choosing op amps for use in driving ADCs, but all of them (ones published by TI as well!) generally point out many things to watch out for, but give little in the way of useful specific advice to a designer. There is good reason for this: there hasn't really been a rigorous analysis of this published, mainly because many of the specific design criteria are not well understood. As engineers, we can't let this stop us, but we can observe some guidelines and make it easier and faster to get to a good design.

The design procedure we will present, then, contains some rigorous analysis, but also observes rules of thumb, some "tricks", and of course refers to the datasheets of the products we will use. As always with analog circuitry, some testing and prototyping will be required.



A/D Converter Terms

- Acquisition Time (t_{ACQ}):
 - The time the internal A/D sample capacitor is connected to the A/D input.
- Conversion Time (t_{CONV})
 - The additional time the A/D requires to convert the analog input to a digital output after the acquisition time (t_{ACQ}) is complete.
- Throughput Rate [Sampling Rate]
 - Maximum frequency at which A/D conversions can be repeated
 - i.e. 100kHz Throughput Rate [Sampling Rate] implies that an input analog signal may be converted every 10 μ s.

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Before going further, it's important to understand some of the times we'll be considering.

A SAR ADC takes a sample of a signal at a moment in time, and converts that one sample to a digital value. It takes a certain amount of time for the input signal to be connected to the internal capacitor of the ADC and store its voltage on this capacitor. The time to get this voltage stored on the capacitor to the accuracy required by the ADC is the **acquisition time** of the converter.

Once the sample voltage is stored on the capacitor, the actual conversion process takes place, where the sample is successively compared to known fractions of charge. The time it takes to make all of the comparisons and generate the digital value is the **conversion time**.

To accomplish a complete conversion, both the acquisition and conversion times must pass. The fastest a system can sample and convert a signal would be the rate at which it can successively sample. This is referred to as the **throughput rate**. This rate must also include the multiplexer switching and settling time, as well as settling times for the other amplifiers in the signal chain.

Input Buffer Selection

- Charge injection causes large spike which must settle in t_{ACQ} .
- Adding a capacitor (and possibly a resistor) can reduce spike
- Op amp must be capable of charging capacitance in t_{ACQ} to 0.5LSB. Low output impedance at high frequency required.

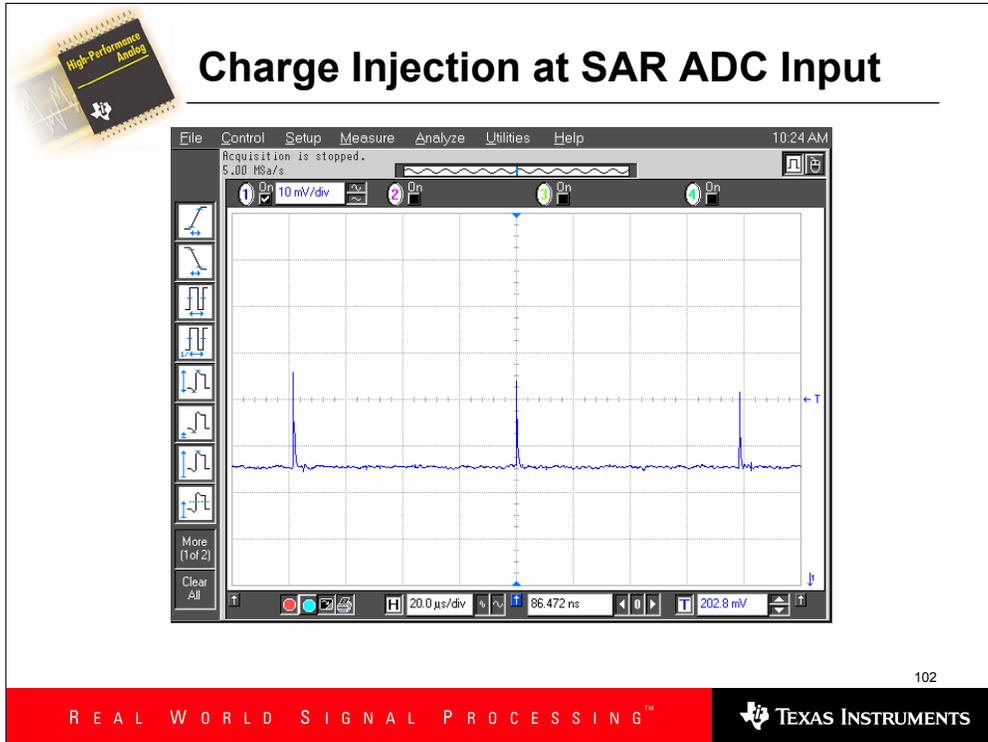
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The input of a modern SAR ADC can be modeled as shown above. The sampling capacitor can at any time have a voltage ranging from 0V to the supply voltage, from sample to sample. As such, this presents a very dynamic load to the driving op amp. Because of the sample capacitor may have residual charge on it from a previous conversion, it is not uncommon for this charge to discharge back out of the ADC input terminal. This “kickback” charge injection can sometimes be seen with an oscilloscope!

To help reduce this effect, and to provide a charge reservoir for charging the sampling capacitor (more on this later), a small RC circuit is usually added between the op amp and the ADC. The op amp must be capable of driving this largely capacitive load, and having it settle within 0.5LSB within the acquisition time of the ADC. Generally, this means that the op amp must have a low wideband output impedance. We’ll look at the op amp requirements in a bit more detail later.



This is a scope capture of the input of a SAR ADC which clearly shows the charge injection. This particular converter shows about a 20mV spike, which is equivalent to a little more than 16LSBs. If you can see spikes like this on the input to your SAR, it means that the impedance of your source is too high!



What Settling Time?

- Think of a linear voltage regulator, there are **TWO** Settling Times.
 - Line Transient
 - Load Transient
- **Same** applies here.
 - Line Transient =
Input Step Voltage; Output Voltage Slew Rate
 - Load Transient =
Output Step Voltage/Current Change

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Choosing the op amp to drive such a difficult input requires that we think of it like a voltage regulator. Voltage regulators usually specify two different settling times: a response to a line transient, which in our case is the input voltage changing, and a load transient, which is the dynamic loading our SAR presents to the op amp.



Settling Time

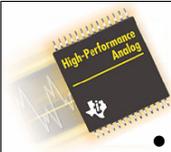
Number of bits	0.5LSB	Time Constants
10	0.0488281%	8
12	0.0122070%	9
14	0.0030518%	11
16	0.0007629%	12
18	0.0001907%	13
20	0.0000477%	15
22	0.0000119%	17
24	0.0000030%	18

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How much time do you need to settle? This table lists the number of time constants required to settle to within a half LSB to a given number of bits. For our 18-bit example, we must allow 13 time constants to pass to be settled to the accuracy required.



Line Transient Becomes

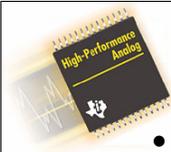
- Response to change in input signal
- Includes Slew Rate.
- Op Amp data sheets MAY address Settling Time to 0.01%
- But we need 0.0001907% for an 18 bit system

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As noted, the input signal changing and the op amp slewing is the line transient for our imaginary voltage regulator. Op amp data sheets may specify a settling time, but if they do it is usually only to 0.01% - which from the previous slide we can see is only about 12 bits. Our 18 bit system needs 0.0001907% settling – and we're not likely to find that specified on an op amp data sheet!



Load Transient is WORST

- We know the load is the input capacitance of the A/D
- We do NOT know the starting voltage.
 - Possible voltages: GND, Mid-Rail, Random
- The Op Amp data sheet does NOT even mention this action.

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The load transient poses the biggest problem for us in choosing an op amp, because while we know the load is the input capacitor of the ADC, we don't know what voltage might be on it at any given time.

No op amp data sheet even discusses the effect of load transients of this nature.



Step by step procedure...

- This is just a starting point
- Tuning for BEST results
 - Filter Capacitor
 - AC Magnitude
 - DC Offset
 - Sample Rate
- Different converters
- Testing DC parameters
- Testing AC parameters
- Rules of Thumb & Tricks
 - To Optimize Op Amp, Filter, A/D System
- You **WILL NEED TO TEST** in your final application



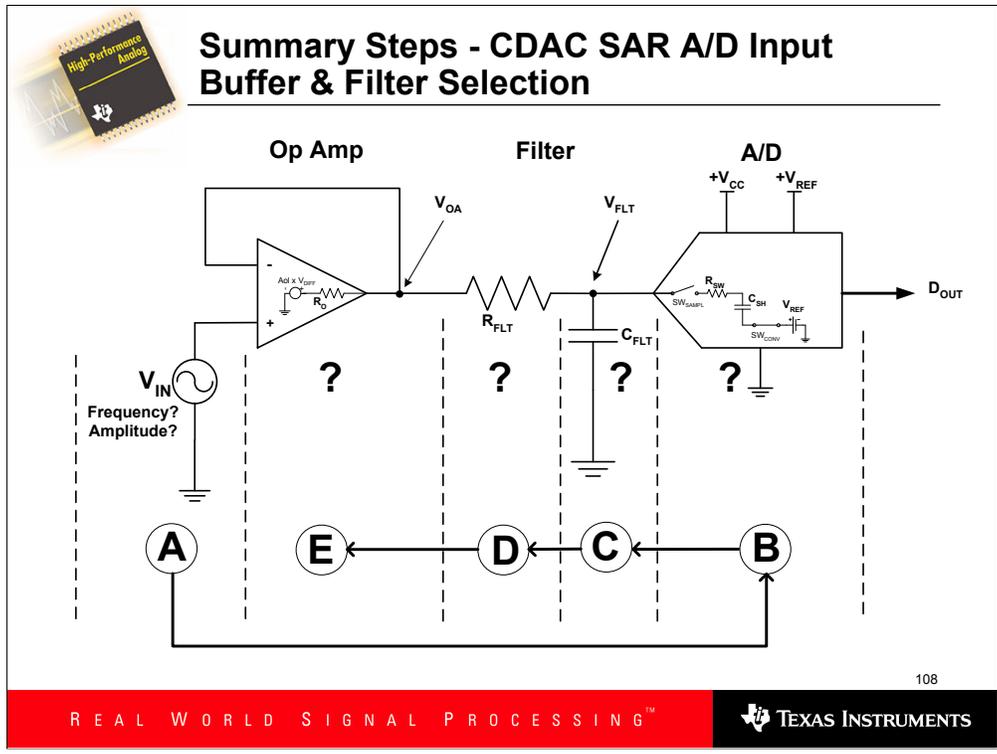
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We know some of the problems we face now; it's time for our design procedure. A disclaimer of sorts: this will provide a starting point, and some tuning of component values will likely be required to meet your specific needs. This procedure has been developed by observing systems that work and those that don't: as such many rules of thumb are used.

You will need to test everything. That's part of life in the analog world.



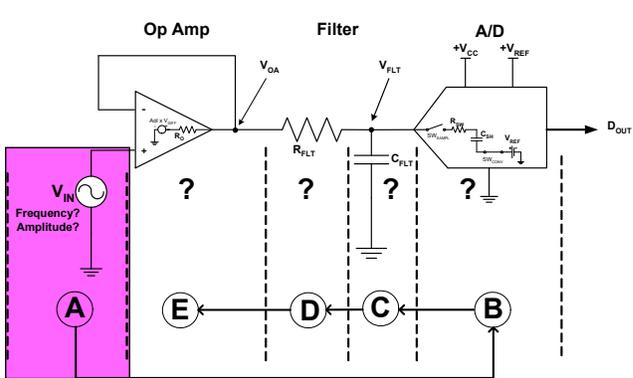
This slide shows the order of steps to take in finding the right components. First, define your input signal amplitude and frequency, as well as the power supplies available. Next, choose the converter you intend to use. These parameters help frame the problem in terms of knowing the full-scale range and LSB sizes you're dealing with.

Next, choose the value for the capacitor, and then the resistor, in the RC circuit. Finally, you will have enough information to narrow down the many choices in op amps you have to just a few that should be suitable for this purpose.

What's not shown? Testing. You'll still have to prototype the system and test it, so you can tune it for optimum performance for you application.



1. Specify System Voltages



- ADC
 - +5V
- Op Amp
 - $\pm 5V$ to $\pm 15V$
 - We have options here...

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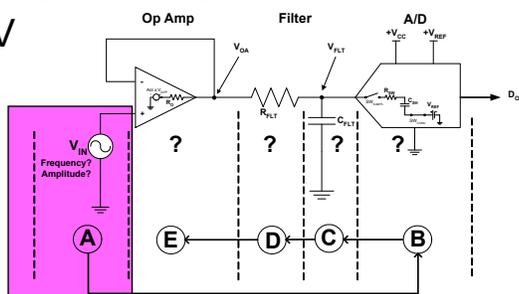
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Let's begin with our power supply voltages. In our system, the ADC operates off of +5V, while the input stage operates off of $\pm 15V$. We probably also have the option of using $\pm 5V$ supplies if needed, so we have several options to consider when choosing our op amp.



2. Define Maximum Input Signal

- Highest Frequency
 - 100kHz (single channel)
 - 10kHz (multiplexed signal)
- Largest Voltage Swing
 - 0 to 4.096V



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We know from our look at the antialiasing filter that in the multiplexed case, our highest frequency per channel is 10kHz, and for a single channel, 100kHz. The largest voltage swing our ADC can handle on its input is 0 to 4.096V – we’ve designed the whole system around this.



3. Choose A/D Converter

- Highest Resolution/Speed Combination
- SAR Architecture – no latency!
- ADS8383

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We've already chosen the ADC – and ADS8383. We went with the SAR architecture for its low latency in this multiplexed application, and chose this particular converter because it offered the highest speed and resolution combination in this architecture.



ADS8383 Application Specs

- “18-BIT, 500-kHz, Unipolar Input, Micropower Sampling Analog-To-Digital Converter With Parallel Interface”
- $V_{CC} = +5V$, $V_{REF} = +4.096V$
- Throughput Rate (Sampling Rate) = 500kHz
- $t_{ACQ} = 0.4\mu s$
- Input Signal = $4.096V_{PP}$, 100kHz max
- SNR = 87dB @ 100kHz
- THD = -90dB @ 100kHz
- SINAD = 85dB @ 100kHz
- SFDR = 90dB

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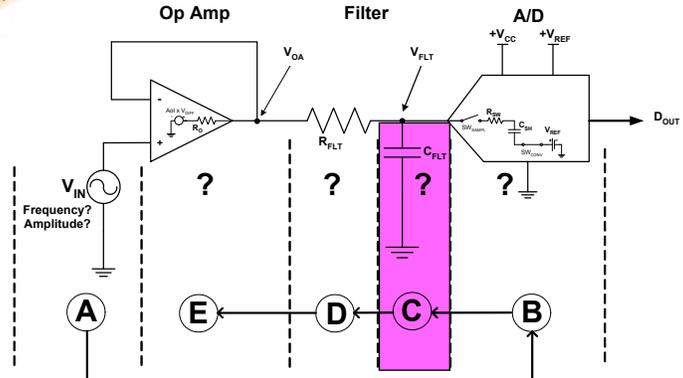
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Here's some of the important specifications we'll need to know about the converter to carry out our design procedure and analysis. Fortunately, all of these parameters are specified in the datasheet!



4. Choose C_{FLT}



- Like a flywheel, this stores energy to charge the internal sampling capacitor
- C_{FLT} is a “charge bucket”

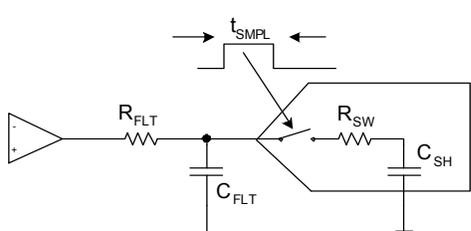
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Now onto the capacitor. This capacitor serves several purposes: to store energy to charge the internal sampling capacitor, to provide a place for the internal capacitor’s charge injection to go, and to reduce noise at the input of the ADC. Due to its storage capabilities, we refer to this sometimes as the “flywheel” capacitor, because like a flywheel, it stores energy for when we need it: during the acquisition time of the ADC. It is a charge reservoir, or “charge bucket” as some like to call it.



Filter Application Specs



- $R_{SW} = 100\Omega$ (Not needed for Buffer & Filter Calculations) 
- $C_{SH} = 45\text{pF}$ 
- Worst case ΔV across C_{SH} is V_{REF} 
 - $V_{REF} = +4.096\text{V}$
- $t_{ACQ} = 0.4\mu\text{s}$ 

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What do we need to know to find the right value for this capacitor?

It would help to know the values of the internal capacitor for the ADC: this is usually specified in the datasheet. But the on-resistance of the sampling switch is not specified, but a good estimate is generally 100Ω.

We don't know the voltage across the internal capacitor at any one time, but we can say that the most the capacitor will see is the reference voltage, which in our case is 4.096V.

Lastly, the acquisition time of this converter is specified in the datasheet as 400ns, or 0.4μs.



Filter Application Specs (cont)

- Charge Transfer Equation: $Q = CV$
- Charge required to charge C_{SH} to V_{REF} 
 - $Q_{SH} = C_{SH} V_{REF}$
 - $Q_{SH} = 45\text{pF} \cdot 4.096\text{V} = 184\text{pC}$
- IDEAL C_{FLT}
 - “Charge Bucket” to fill C_{SH} with only a $7.8\mu\text{V}$ (1/2LSB) droop on C_{FLT}
 - $Q_{FLT} = Q_{SH}$
 - $Q_{FLT} = C_{FLT} (7.8\mu\text{V})$
 - $184\text{pC} = C_{FLT} (7.8\mu\text{V}) \rightarrow C_{FLT} = 23.6\mu\text{F}$
- IDEAL $C_{FLT} = 23.6\mu\text{F}$
 - Not a good, small, cheap high frequency capacitor
 - Not practical for Op Amp to drive directly (stability, transient current)
 - Isolation resistor likely not large enough to help isolate Cloud and still meet necessary filter time constant

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Armed with these specifications and assumptions, we calculate the charge needed to charge the internal sampling capacitor to the reference voltage. Ideally, the “charge bucket” would provide enough charge to the internal sampling capacitor that the voltage on the filter cap would droop by less than 0.5LSB, which in our case is only $7.8\mu\text{V}$. This would require a capacitor of almost $24\mu\text{F}$!

Clearly, this is not practical. The op amp probably couldn’t drive such a large capacitive load, nor could the RC time constant be made short enough that the input signal could settle in a reasonable time. Moreover, the capacitor itself is probably large and perhaps expensive. What else could we do?



Filter Application Specs (cont)

- **Partition the “Charge Bucket”** 
 - 95% from C_{FLT}
 - 5% from Op Amp

- **C_{FLT} value required to provide Q_{SH} with <5% droop on C_{FLT}** 
 - $Q_{FLT} = Q_{SH}$
 - $Q_{FLT} = C_{FLT} (0.05V_{REF})$
 - $184\text{pC} = C_{FLT} (0.05 \cdot 4.096\text{V}) \rightarrow C_{FLT} = 900\text{pF}$
 - We'll use 1000pF

- During t_{ACQ} the Op Amp must replace 5% V_{REF} on C_{FLT} 
 - **Ensure C_{FLT} is at least $10X > C_{SH}$**
 - This implies dominant load for Op Amp Buffer is C_{FLT}
 - $1000\text{pF} = 22.2 \times 45\text{pF} \rightarrow C_{FLT} > 10X C_{SH}$

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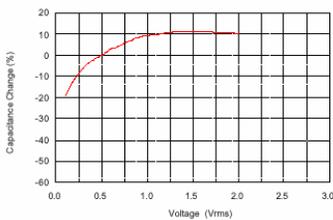
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Let's partition the “charge bucket”, so that the op amp provides some of the current to charge the sampling capacitor. Now the requirement on the filter cap is that it provide a less than 5% droop when supplying the charge. This suggests a more reasonable value of about 900pF – we'll use 1000pF as a close approximation. Remember, all the values we find are starting points, and then we'll optimize, so there's no need to be too rigid about the results. As a check, make sure that the filter capacitor value chosen is at least 10 times the internal capacitor value. In our case, it's more than 20 times the size, so we're meeting that rule of thumb.



Choosing Capacitors for “Flywheel”

- Voltage coefficient causes distortion
 - $C = C_0(1+KV)$
 - Current needed to charge cap varies with voltage
 - Nonlinear error proportional to frequency
 - This happens inside the ADC too!



Source: Murata

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TEXAS INSTRUMENTS

One thing to watch out for in choosing the filter capacitor is distortion. The distortion occurs due to the normal voltage dependant characteristic of the capacitor, meaning that the capacitance changes with the voltage applied.

An equation that describes this change in one region of the voltage curve is:

$$C = C_0 (1 + KV),$$

where

C_0 is the nominal capacitance,

V is the voltage across the capacitance,

K is the voltage coefficient of the capacitor.

A plot of a typical curve of this capacitance is shown in this slide.

This voltage-dependant capacitance causes the current necessary to charge the capacitance to vary with voltage (in addition to frequency).

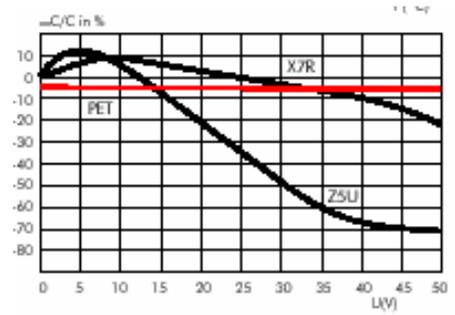
This current travels through the ADC driving impedance, which creates a voltage drop error, which again varies with voltage. Since it is voltage dependant, it creates a non-linear error. For a sine wave, this error contains harmonics, and since this error originates as a current charging a capacitance, the error is non-existent at DC, and gets proportionately larger with frequency.

This characteristic can be more pronounced in semiconductor process



Choosing Capacitors for “Flywheel”

- Use polypropylene – less voltco means less distortion



The graph plots the change in capacitance, $\Delta C/C$ in %, on the y-axis (ranging from -80 to 10) against voltage $U(V)$ on the x-axis (ranging from 0 to 50). Three curves are shown: X7R (ceramic), PET (polyester), and Z5U (ceramic). A horizontal red line at 0% represents polypropylene. X7R shows a small initial increase followed by a gradual decrease. PET shows a moderate decrease. Z5U shows a sharp, significant decrease in capacitance as voltage increases.

Source: WIMA

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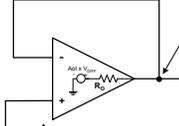
TEXAS INSTRUMENTS

For our larger capacitor outside the ADC, it’s important that we do what we can to reduce the effects of the capacitor’s voltage coefficient, by using good quality capacitors with low voltage coefficients. Polypropylene capacitors, shown as the red line here, have a very stable capacitance vs voltage, as opposed to even some of the better ceramics like X7Rs, as shown in the curve above.



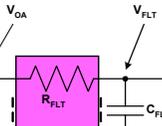
5. Choose R_{FLT}

Op Amp



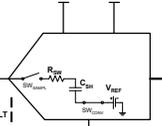
?

Filter



?

A/D



?

V_{IN}
Frequency?
Amplitude?

A E ← D ← C B

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With the capacitor chosen, we move on to the resistor.



Filter Application Specs (cont)

- Time required for C_{SH} & R_{SW} to settle to 1/2LSB @ 18 Bits
 - $R_{SW} = 100\Omega$ (If unknown assume 100Ω)
 - $\tau_{AD} = R_{SW} C_{SH} = 100\Omega \cdot 45pF = 4.5ns$
 - $t_{AD\ settle} = 13 \tau_{AD} = 58.5ns$
 - Small in comparison to t_{ACQ}
- R_{FLT} Calculation
 - $t_{FLT\ settle} = t_{ACQ} = 13T_{FLT}$
 - $t_{FLT\ settle} = 0.4\mu s = 13T_{FLT}$
 - $13T_{FLT} = 0.4\mu s \rightarrow T_{FLT} = 31ns$
 - **$T_{FLT}^* = 0.70 T_{FLT}$** 
 - Margin for:
 - Op Amp Output Load Transient
 - Op Amp Output Small Signal Settling Time
 - $T_{FLT}^* = R_{FLT} C_{FLT}$
 - $0.70 \cdot 31ns = R_{FLT} 1000pF \rightarrow 21.7\Omega$
 - Use $R_{FLT} = 22\Omega$

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TEXAS INSTRUMENTS

The internal RC of the ADC is calculated by multiplying the CDAC capacitance by the switch resistance, which is rarely specified on datasheets. Typically for TI converters, this is somewhere around 100Ω . Using these values and taking the requisite number of time constants for settling to 18 bits, we can find out how long the internal ADC RC takes to settle. This should be small in comparison to the acquisition time of the ADC.

The external RC must also settle within this acquisition time, so we can figure the maximum RC time constant for this circuit from the converter's t_{ACQ} . Then, as a rule of thumb, we will set the external RC settling a bit faster – 70% say, to allow some margin for the op amp load transient and small signal settling time. Using this guideline, we can calculate the required resistance.

6-10. Choose Op Amp

The diagram illustrates a signal processing chain with three main stages: Op Amp, Filter, and A/D. The input signal V_{IN} is characterized by its Frequency and Amplitude. The Op Amp stage is highlighted in pink and contains a question mark, indicating the need to select a suitable op amp. The Filter stage consists of a resistor R_{FLT} and a capacitor C_{FLT} , also with question marks. The A/D converter stage contains a question mark. The output is D_{OUT} . Below the diagram are five circular markers labeled A, B, C, D, and E, with arrows pointing from B to A, C to B, D to C, and E to D. A red banner at the bottom contains the text "REAL WORLD SIGNAL PROCESSING" and the Texas Instruments logo.

With our RC filter values chosen, we can now search for a suitable op amp to drive this system.



Op Amp Buffer Application Specs

- Application:
 - Bipolar or Single Supply
 - Inverting Gain of -1
 - Slew Rate to track 100kHz Input
 - Wideband for good gain flatness: 100kHz, $G=-1$
 - Wideband for fast transient response to Noise Filter Transients
 - Low Noise for 18-Bit performance
 - Fast Settling time for output transients
 - Adequate Output Drive Current for Filter Transients

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As mentioned earlier, knowing what power supplies you plan to use to power the op amp is important. It helps to narrow down the available choices. In our case, we'll opt to use a bipolar supply, since they're available.

This buffer amplifier may be configured as either a follower (noninverting gain of 1) or an inverting gain of -1 amplifier. We've chosen an inverting configuration so that we don't have any issues with common-mode voltages causing distortion. The amplifier must also have sufficient slew rate to track a 100kHz signal (should we use one channel and allow that bandwidth). A wideband amplifier will generally have fast transient response and will be able to handle the load transients better. It should also have sufficient drive current and fast settling time.

Because our system is 18 bit, a low noise amplifier is a must.



Op Amp Selection

- TI has over 600 op amp families!
- How can you quickly narrow the choices down to a few?

- Dual Supply, Single Op Amp, Single Ended Output
 - Number of Op Amp Choices: 74

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Let's begin the selection process. TI alone has over 600 op amp families – how do we narrow down the choices quickly?

Go to www.ti.com, and in the amplifier section, do a parametric search. There are three areas to consider: high-speed current feedback, high-speed voltage feedback, and the regular op amps. Yes, you have to do three searches – but it's easier than looking up all 600 data sheets!

Start with the power supplies: we chose to use bipolar supplies, and need only a single-ended output. This reduces the options to 74 op amp types.



6. Calculate Op Amp Transient Output Drive

- Op Amp Transient Output Drive to R_{FLT} & C_{FLT}
 - $I_{Opk\ max} = (5\% V_{REF}) / (R_{FLT}) = 205mV / 22\Omega = 9.3mA$
 - Number of Op Amp Choices: 74

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TEXAS INSTRUMENTS

Using the value of the filter resistor we found, and remembering that the op amp is asked to supply 5% of V_{ref} to recharge the flywheel capacitor, we can calculate the current drive required. This may help narrow the choices. In our case, all of the bipolar op amps are capable of driving the required current, so we're still left looking at 74 op amps.



7. Calculate V_{OA} Bandwidth

- Calculate Unity Gain BW
 - **Select unloaded Op Amp BW > 4 X $V_{FLT\ f-3db}$** 
 - $V_{FLT\ f-3db} = 1/[2\pi R_{FLT} C_{FLT}]$
 - $V_{FLT\ f-3db} = 1/[2 \cdot \pi \cdot 22 \cdot 1000e-12] = 7.2\text{MHz}$
 - Op Amp BW > 4 X 7.2MHz = 29MHz
 - Number of Op Amp Choices: 26
- $SR\ (V/\mu s) = 2\pi f V_{OP}\ (1e-6)$
 - Minimum Slew Rate to track input sinewave
 - $SR_{min} = 2 \cdot \pi \cdot 100\text{kHz} \cdot (4.096V_{pp}/2) \cdot (1e-6) = 1.29V/\mu s$
 - Choose Op Amp SR > 2 X $SR_{min} = 2.58V/\mu s$
 - Number of Op Amp Choices: 26

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Now we need to find what bandwidth we need for the op amp. The rule of thumb is to select an op amp with a unity gain bandwidth at least 4 times the bandwidth of our RC filter. Doing this in our case finds that we need an op amp with better than 29MHz GBW. This narrows our choices down to 26 op amps.

Now check to make sure the slew rate is adequate for the input signal we expect. As shown here, we want the op amp to be able to slew at least twice as fast as the input signal for low distortion. All of the op amps with sufficient bandwidth have adequate slew rates in our case, so our choices remain at 26.



8. Op Amp Selection - General

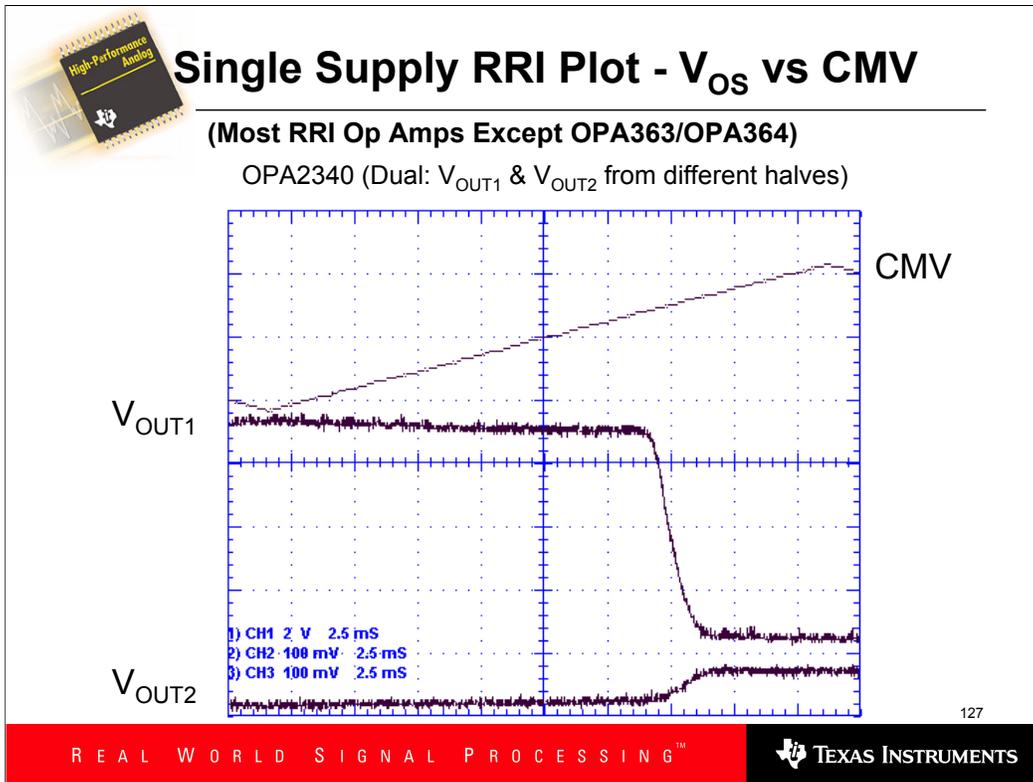
- Choose Buffer or Inverting Buffer Configuration
- If Buffer on Single Supply:
 - Beware of Input CMV Crossover

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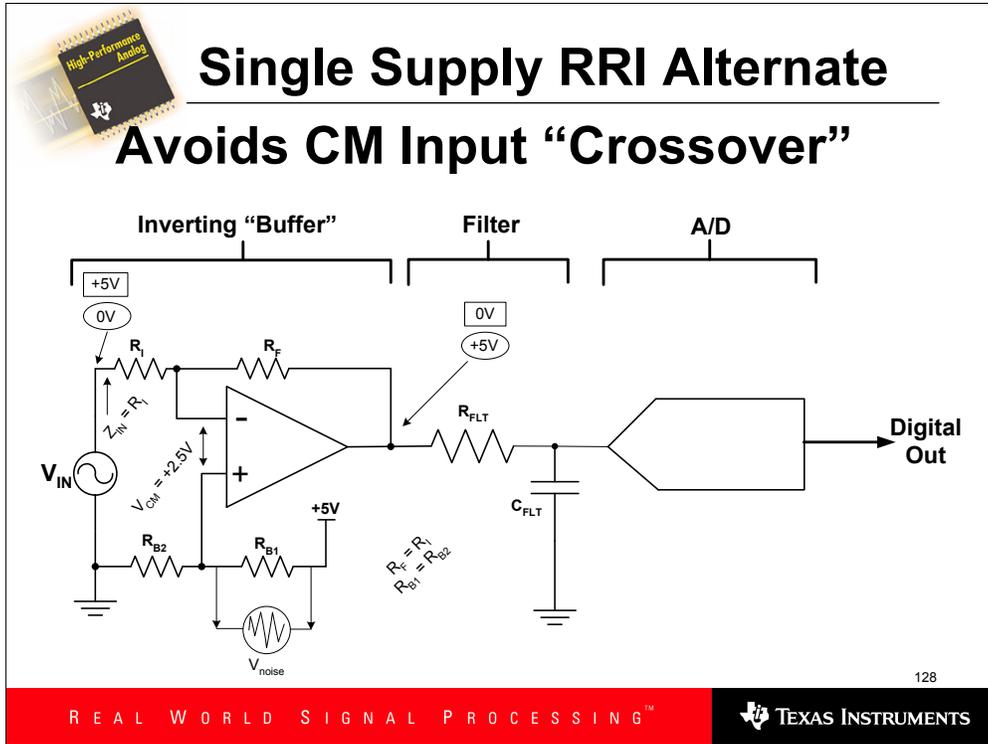


As mentioned, we've chosen a bipolar op amp in an inverting configuration. But you may want to use a single supply. With these type of rail-to-rail op amps, you must be careful of the distortion caused by the common mode transitioning between input bias stages of the op amp.



As the input common-mode signal goes up, rail-to-rail op amps will transition from one input bias stage to another. The middle trace is the output of one OPA340 and the bottom trace is the output of the second OPA340 in the same package. V_{out1} shows the offset of the op amp changing by almost 300mV as the signal sweeps through this transition region. Worse yet, the second op amp in the same package doesn't change by the same amount, and changes in a different direction!

This phenomenon causes distortion in an AC sense, and what might appear to be nonlinearity in a measurement system in a DC sense.



To avoid this common-mode voltage problem, use an inverting buffer topology. On a single-supply, this means biasing the noninverting input of the op amp to a point above the transition region, so that the input common-mode voltage never passes from one bias stage to the other, as shown here.



Single Supply Inverting “Buffer”

- Z_{IN} is R_I (typically $< 100k\Omega$) instead of $1G\Omega$ range
- V_{OUT} of Buffer is Inverted from V_{IN}
- V_{CM} does not move and is steady at $1/2V_{CC}$
- Mismatch in ratios of $R_F / R_I = 1$ and $R_{B1} / R_{B2} = 1$
 - Gain & Offset Errors
- R_I, R_F, R_{B1}, R_{B2} are additional noise sources

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Of course, this presents some tradeoffs: now the input impedance is lower, and the output is inverted. Resistor noise and matching are other potential error sources, but these can be minimized with careful component selection.



8. Op Amp Selection - General (cont)

- Gain Error
 - $AV_{CL} = A_{ol}/(1+A_{ol}\beta)$
 - $A_{ol} @ 1\text{kHz} = 97\text{dB} = 75000$
 - $\beta = 1/2$ for Inverting Gain of 1
 - $AV_{CL} = 10,000/(1+10000 \cdot 1) = 1.99994667$
 - 0.005333% Gain Error @ 1kHz
 - ≈ 13 Bit (1/2 LSB Accuracy)
 - A/D Initial Reference Error (0.02% < Typical Range < 0.2%)
 - Calibrate gain error at system level

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One thing to consider is the open loop gain of the op amp, and how that might contribute to gain error. For example, an op amp with 97dB of open loop gain would give us a gain accuracy only to about a 13 bit level. Is this a problem? Probably not – the other gain error sources in the system, from our front end to the reference, are generally much larger. Calibration at the system level can remove this error, and is generally required of any measurement system.



8. Op Amp Selection - General (cont)

- Settling Time
 - A/D $t_{ACQ} = 0.4\mu s$
 - t_s to **0.01%** < t_{ACQ}
 - Number of Op Amp Choices: 7



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TEXAS INSTRUMENTS

We must make sure that the op amp we choose will settle in the required time. Most op amp data sheets specify settling only to a 12-bit level, but at least here we can do a check to see if the op amp settles to at least that level in the required acquisition time. Doing this in our case narrows the choices of op amps down to a mere 7.

We went from 600 possibilities down to 7 in only a few short steps, and can easily do this using selection guides or parametric search engines.



8. Op Amp Selection - General (cont)

- THD+Noise
 - 18 Bit desired 0.00019% or -114dB (1/2LSB)
 - Number of Op Amp Choices: 3 perhaps
 - Best THD: THS4031
- Open Loop Output Resistance (R_O)
 - “ $1/g_m$ ” dominant for an active device
 - THS4031: 13 ohms



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TEXAS INSTRUMENTS

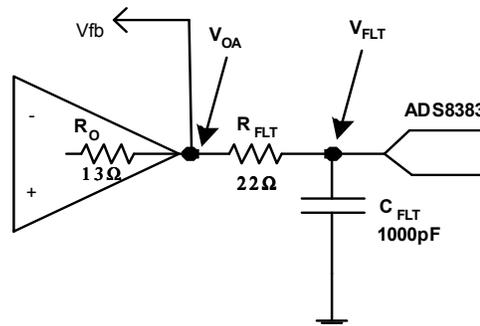
The last consideration is distortion and noise. At our 18-bit level, we'd like something with extremely low distortion in our signal range of interest. This requires looking at the data sheets (but we've only got 7 to look at now!), because this parameter is rarely shown in selection tables. Usually a curve is included in the datasheet showing this even if it is not specified in the op amp specification table.

In our case, three op amps looked like they would come close, and the best distortion appeared to be achievable by the THS4031. So we'll choose that as our op amp to use for the rest of the design exercise.

With the op amp chosen, we now need to find its open loop output resistance. Sometimes, this is specified on the data sheet, but many times it is a factory-only parameter. You may need to call the factory to find this in these cases. Fortunately for the THS4031, this is specified in the data sheet as 13 ohms.



9. Op Amp + Filter Analysis – Small Signal



- Modify Aol due to R_{FLT} & C_{FLT}
 - $f_{PX} = 1/[2\pi(R_O + R_{FLT})C_{FLT}]$
 - $f_{PX} = 1/[2\pi(13\Omega + 22\Omega)1000\text{pF}] = 4.5\text{MHz}$
 - $f_{ZX} = 1/[2\pi R_{FLT}C_{FLT}]$
 - $f_{ZX} = 1/[2\pi \cdot 22\Omega \cdot 1000\text{pF}] = 7.2\text{MHz}$

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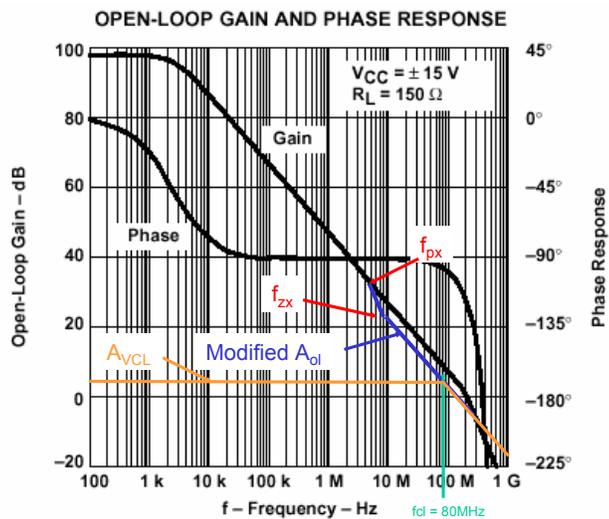
TEXAS INSTRUMENTS

The reason we need the open loop output resistance is that we now must check the small signal performance of the chosen op amp, and check for stability of this op amp driving the RC circuit.

The Aol of the op amp will be modified by a pole present from the open loop resistance plus the RC, and then canceled by a zero from the RC.



9. Op Amp + Filter Analysis – Small Signal (cont)



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TEXAS INSTRUMENTS

Drawing the pole and zero in on the open-loop gain chart shows us the modified A_{o1} . The closed loop gain can then be plotted, so that we can find the closed loop corner frequency of the op amp response.



9. Op Amp + Filter Analysis – Small Signal (cont)

- Buffer Closed Loop Gain Bandwidth
 - $f_{CL} = 80\text{MHz}$
- **Stability Check** 
 - At $f_{CL} = 80\text{MHz}$ “Rate-of-closure” is 20dB/decade $\rightarrow f_{ZX}$ cancels f_{PX} before f_{CL}
 - f_{PX} and f_{ZX} are \leq decade apart
 - Phase of pole will be cancelled by phase of zero
- **$V_{OA} \text{ BW} > 2x V_{FLT} \text{ BW}$** 
 - $V_{OA} f_{-3db} = f_{CL} = 80\text{MHz}$
 - $V_{FLT} f_{-3db} = 1/[2\pi R_{FLT} C_{FLT}] = 7.2\text{MHz}$

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TEXAS INSTRUMENTS

Now that we know the closed loop bandwidth, we can do a stability check. The rule of thumb is to make sure that the rate of closure at the corner frequency is 20dB/decade. Generally this is assured if the zero of the RC cancels the pole before reaching the closed loop bandwidth frequency, and the zero frequency is less than a decade from the pole frequency. In our case, this checks out.

Then we must assure that the op amp bandwidth is more than twice the filter bandwidth, which in our case is quite true.



9. Op Amp + Filter Analysis – Small Signal (cont)

Small Signal Transient Response

- Small Signal Settling Time Constant
 - $t_{\text{settle ss}} = 1/(2\pi f_{\text{CL}})$
 - $t_{\text{settle ss}} = 1/(2\pi \cdot 80\text{MHz}) = 1.9\text{ns}$
- Small Signal Settling Time
 - $t_{\text{settle ss}} = 13\tau = (13)(1.9\text{ns}) = 25.8\text{ns}$
- **Small Signal Transient Response $\leq 30\% t_{\text{ACQ}}$** 
 - $t_{\text{settle ss}} \leq 30\% t_{\text{ACQ}}$
 - $0.026\mu\text{s} < (0.30)(0.4\mu\text{s}) = 0.120\mu\text{s}$
 - Excellent!

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Last, we look at the small signal settling response of the op amp. Knowing the closed loop bandwidth, we calculate the settling time constant, and then find the required number of time constants for our ADC.

Recall that when we designed the RC filter, we set its time constant to 70% of the acquisition time of the converter. This was to allow margin for the op amp to settle. So our op amp must settle in less than 30% of the acquisition time, as that's all that's left! In our case, the THS4031 settles much faster than required, so our system should work as expected.



10. Op Amp + Filter Noise Analysis

- Op Amp + Filter
 - BW = 7.2MHz
 - $V_{noise} = (\text{Op Amp Noise})[(\text{Filter BW})(\text{Single Pole Noise BW Ratio})]$

$$V_{noise} = 2[1.6nV / \sqrt{Hz} \sqrt{(7.2MHz \cdot 1.57)}] = 10.8\mu V_{rms}$$
 - Inverting Amp Noise Gain is 2
 - White Noise Dominant with 7.2MHz BW
 - Resistor Noise = $\sqrt{4KTRB}$
 - B = (Filter BW)(Single Pole Noise BW Ratio) = 7.2MHz·1.57 = 11.3MHz
 - KT = 4.11×10^{-21} @ 25°C
$$22\Omega \text{ noise} = \sqrt{(4.11 \times 10^{-21})(22\Omega)(11.3MHz)} = 2\mu V_{rms}$$

$$Total \text{ Noise} = \sqrt{(V_{noise})^2 + (R_{noise})^2} = \sqrt{(10.8\mu V_{rms})^2 + (2\mu V_{rms})^2} = 11\mu V_{rms}$$

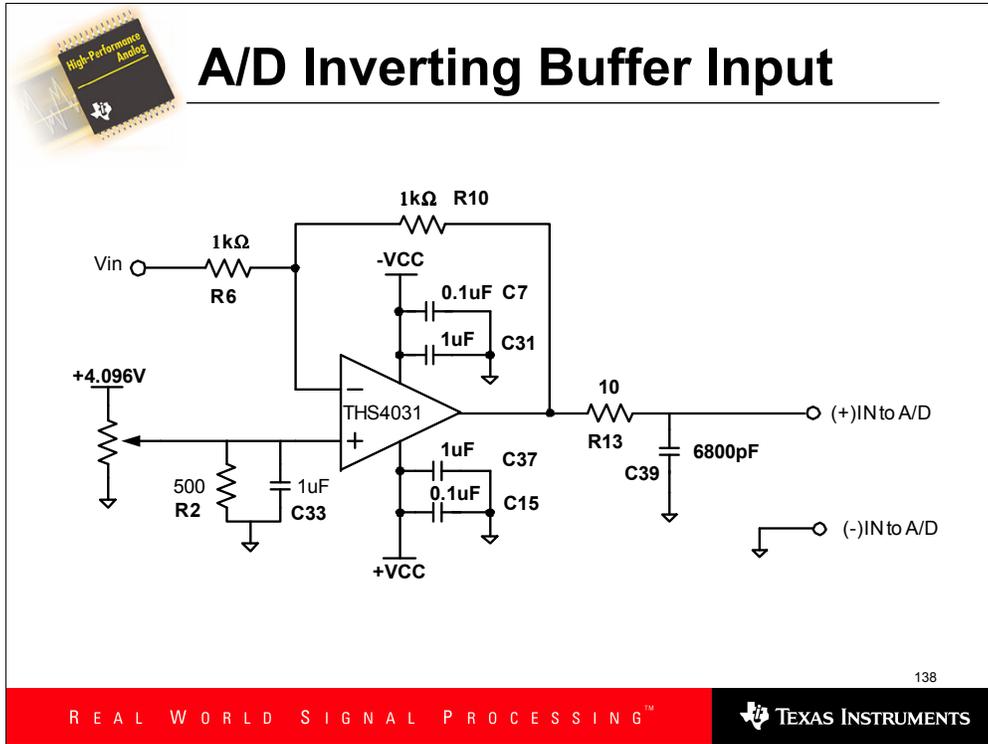
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Let's now proceed with an noise analysis of the circuit we've just designed.

The op amp noise specification for our op amp is a low 1.6nV/√Hz. Since we have an inverting buffer, the noise gain for our amplifier is 2, and this must all multiply the square root of the filter bandwidth, times a factor of 1.57, which accounts for the single-pole rolloff.

Similarly, resistor noise is calculated using the familiar resistor noise equation. The contributions of both the op amp and resistor are combined to provided a total noise contribution of 11μVrms, just over half an LSB.



This is the final buffer circuit that we have arrived at.



Demonstration

Calculated Values

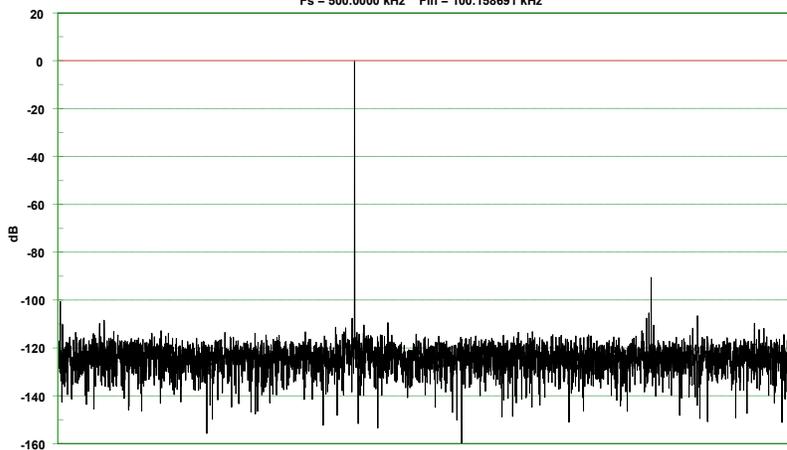
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14. Prototype and Test!



Frequency Spectrum (8192 Point FFT)
Fs = 500.0000 kHz Fin = 100.158691 kHz



SNR = 85.831 SINAD = 84.379 SFDR = 90.632 THD (9) = -89.845 ARL = 96.285

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Demonstration

Modified RC

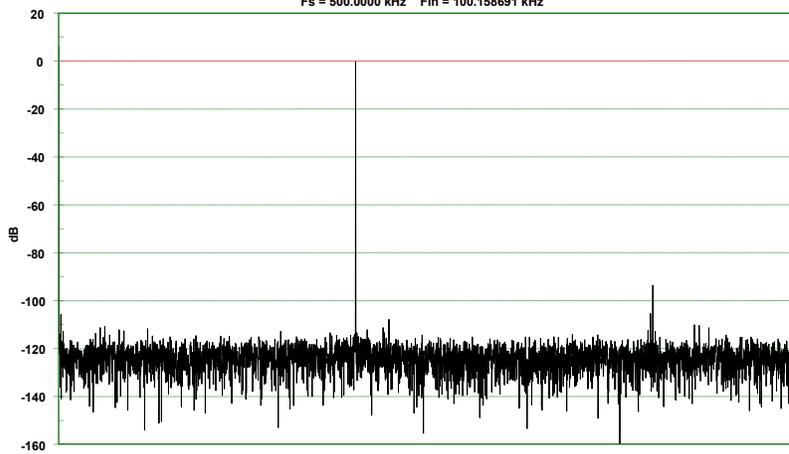
141



Modified RC



Frequency Spectrum (8192 Point FFT)
Fs = 500.0000 kHz Fin = 100.158691 kHz



SNR = 86.012 SINAD = 85.205 SFDR = 93.616 THD (9) = -92.909 ARL = 96.131

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Voltage references

- The measurement is only as accurate as the reference!

$$code = \frac{V_{in}}{V_{ref}} 2^N$$

where:

N is the word length

V_{in} is the input voltage

V_{ref} is the reference voltage

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It may seem obvious, but your ADC is only as accurate as the reference you use.

Analog-to-digital converters don't really measure voltages - they can only *compare* a voltage to another voltage. (Here is something to think about: *all* measurements are, in fact, comparisons.) The slide shows the ideal transfer function for an ADC. Study the equation and think about what happens when the reference voltage V_{ref} changes. From the equation, it follows that if your reference is noisy, so too will your measurement.

An interesting fact is that larger signals tend to be affected by the reference more than smaller signals. An extreme case is measuring a voltage of zero. If the input voltage is zero, it is, according to the equation, not affected by the reference at all.



Voltage references

- Reducing noise
 - Use a quieter reference
 - Use lots of filtering
- Reducing drift
 - Use a low-drift reference
 - Compensate in software
 - Use active temperature control
- Initial accuracy
 - Calibrate

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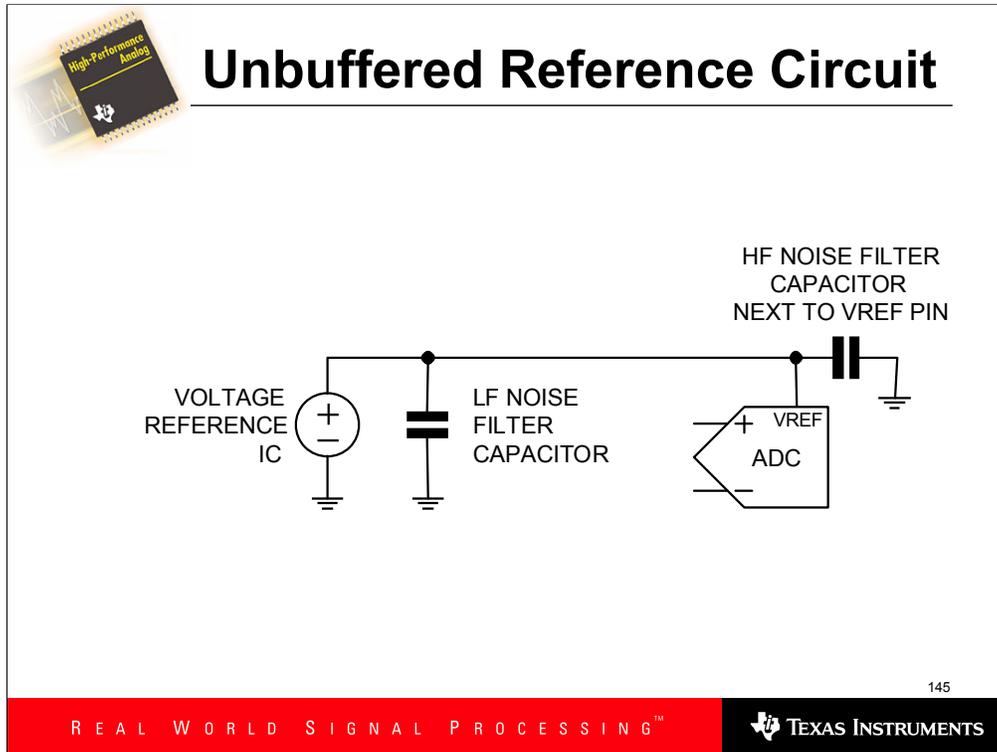
The three main problems to conquer in a voltage reference circuit are noise, drift, and initial accuracy.

Noise is easy to deal with – to a point. The simplest way to reduce voltage reference noise is to add filtering. This is easily done using large capacitors. Typically, the larger the capacitor, the better. There is a diminishing return associated with capacitance, however, so it's always best to start with a reference that's low noise.

Drift is a bit more difficult to deal with. The easiest way to deal with it is to start with a voltage reference that's low drift. Unfortunately, very low-drift references can be quite expensive. A fairly low-cost way to compensate for drifty references is to use a temperature sensor and compensate in software.

For the very serious, it is possible to use direct thermal compensation using “ovens” or Peltier coolers. Small Peltier junctions are available which you can mount to the top of the voltage reference. Control it with a set-point circuit, and you can virtually eliminate drift completely in almost any reference IC. Unfortunately, this approach is very high in cost, and very power-hungry – it is completely unsuitable for battery-powered applications.

Absolute reference inaccuracies must be calibrated out. In many small-signal measurement applications, this happens as part of the overall system calibration process.



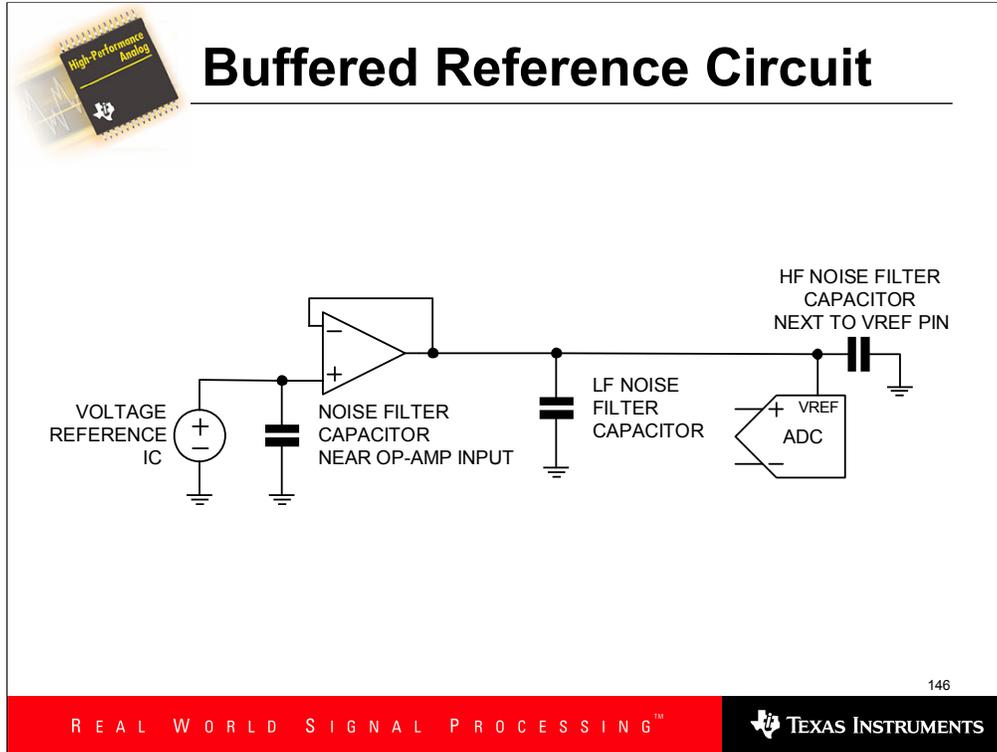
If the ADC's reference input has a high impedance, you can often get away without using a reference buffer. This is a desirable approach, since buffers add noise and cost.

Use a large capacitor for filtering out the majority of the noise. This capacitor can be placed anywhere along the reference trace. Try to find a capacitor with the lowest ESR possible, especially if the capacitor is very large (> 100uF).

Some references cannot tolerate large capacitance. If you still need large capacitors, use a buffer. (A buffered circuit is discussed in the next slide.)

Unless the voltage reference circuit is already very close to the ADC, it's a good idea to add another capacitor next to the voltage reference pin of the ADC. This capacitor need not be large; it's there to filter out RFI and to compensate for line inductance in the reference trace.

If the large capacitor is a tantalum type, use a small ceramic capacitor in parallel with it.



If the ADC's reference input has a low impedance, or your reference cannot drive the ADC, use a unity-gain buffer.

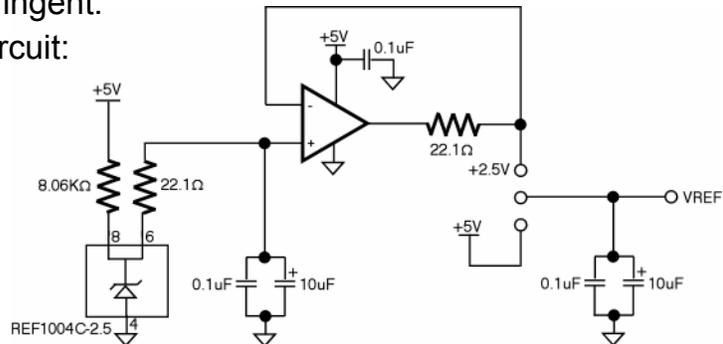
The buffer adds noise, so the main filtering capacitor should be placed after it. Most op-amps can tolerate almost unlimited amounts of capacitance, even if their data sheets list a capacitive load limit. This is because the op-amp in this situation is buffering an essentially unchanging voltage. Nevertheless, it's a good idea to test the op-amp with a large capacitance, to make sure that it will work.

A smaller capacitor should still be connected prior to the buffer, directly to the reference. Some references are designed for a certain capacitance on their outputs, and may oscillate without it.



Reference Buffer Selection

- Reference is DC, right? So a slow op amp is OK?
- No! Same thing happens on reference input as analog input, but it must settle in 1 clock cycle!
- Requirements on reference buffer are even more stringent.
- Circuit:



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You may need to use a high-speed op-amp. The op-amp must be able to respond to changing current demand – as the converter does its work, the current draw through its reference changes, just as it does on the input to the SAR. The problem here is that charge is being drawn out of the capacitor on every clock cycle – every bit decision – of the SAR converter, so the settling time is even shorter. The phenomenon is usually not as pronounced with delta-sigmas as with SARs, but is still important because of the high resolution of a delta-sigma.



Error Sources in the Reference

- Initial Accuracy
 - 0.2% - 524LSBs
- Drift
 - 50ppm/°C
 - from 0 to 50°C, 205μV = 13.1LSBs
- Noise
 - 45μVp-p: about 3LSBs, 0.5LSB rms

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In the reference for our system, we've chosen a REF3040 4.096V reference. Errors associated with this are shown above.

As noted earlier, the initial accuracy, combined with all of the other gain errors, is significant. We must stress again: this can be calibrated out. **All measurement systems will require calibration.**

Drift and noise are manageable. Noise is within a reasonable limit, and filtering can help improve this. Drift is something to be aware of, and if necessary, compensated for provided a temperature measurement can be made and reasonable calibration is done upon a substantial temperature change. Or, as suggested earlier, the reference could actually be put into an environment where its own temperature is controlled in order to minimize drift.



Finally – The Converter!

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We've discussed the A/D converter for our system in many of the previous slides, but we haven't taken a close look at some of the things to consider when choosing an A/D. We'll look at a few considerations now.



What datasheet specs really matter?

- Speed
- Resolution
- INL
- DNL
- Offset
- Gain

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Data converters generally can be chosen primarily on the parameters shown above. Speed and resolution are usually two of the most important factors, followed by the overall accuracy of the converter.



Data Converter Specs - Speed

From ADS8345 datasheet

SAMPLING DYNAMICS							
Conversion Time				16		*	CLK Cycles
Acquisition Time		4.6			*		CLK Cycles
Throughput Rate				100		*	KHz
Multiplexer Settling Time			500		*		ns
Aperture Delay			30		*		ns
Aperture Jitter			100		*		ps
Internal Clock Frequency	$\frac{SINBW}{2}$		2.4		*		MHz
External Clock Frequency		0.004		2.4	*	*	MHz
	Data Transfer Only	0		2.4	*	*	MHz

From ADS8383 datasheet

Sampling Dynamics			
Conversion time		1.5	µs
Acquisition time		0.4	µs
Throughput rate		500	kHz
Aperture delay		4	ns
Aperture jitter		15	ps
Step response		150	ns
Over voltage recovery		150	ns

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TI offers a wide variety of converters for the industrial data acquisition market. The converter speed is always listed until the Sampling Dynamics section of the product datasheet. The speed is referred to as the Throughput Rate of the converter. The throughput or sample rate of the ADS8345 and ADS8383 is 100kHz and 500kHz, respectively.



Data Converter Specs - Resolution

From ADS8383 datasheet:

System Performance				
Resolution			18	Bits
No missing codes	AD883831	$(+IN - -IN) < 0.5 FS$	10	Bits
	AD883831B	$(+IN - -IN) \geq 0.5 FS$	17	
Integral linearity (see Notes 7 and 3)	AD883831	$(+IN - -IN) < 0.125 FS$	-4	4
		$(+IN - -IN) < 0.5 FS$	-6	6
	AD883831B	$(+IN - -IN) \geq 0.5 FS$	10	10
Differential linearity	AD883831	$(+IN - -IN) < 0.125 FS$	-1	2
		$(+IN - -IN) < 0.5 FS$	-1	3
	AD883831B	$(+IN - -IN) \geq 0.5 FS$	-2	7
Offset error (see Note 4)	AD883831		-1	10.5
	AD883831B		-0.75	± 0.25
Gain error (see Note 4)	AD883831	$V_{ref} = 4.096 V$	-0.1	0.1
	AD883831B	$V_{ref} = 4.096 V$	-0.06	0.06
Noise			60	μV RMS
Power supply rejection ratio	A13FFFFh output code		76	dB

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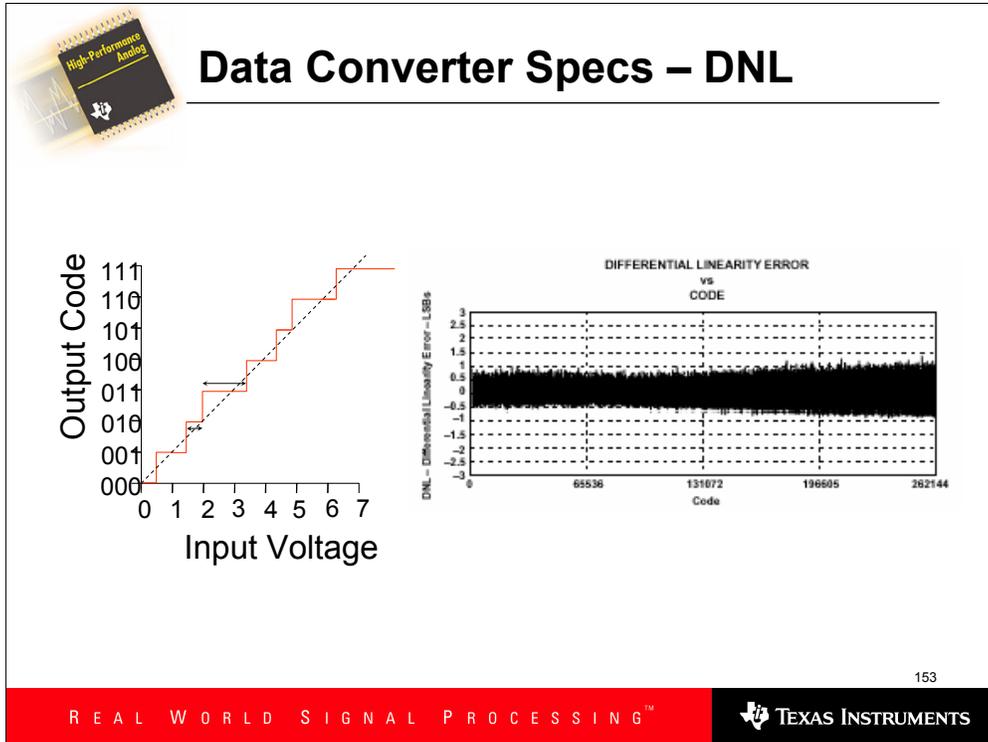
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The Resolution of the converter is listed under the System Performance of section of the specifications table. The ADS8383 is a 18-bit converter.

The resolution of a A/D is specified in bits. It is the number distinct 2^N codes the converter is capable of producing over the full range.

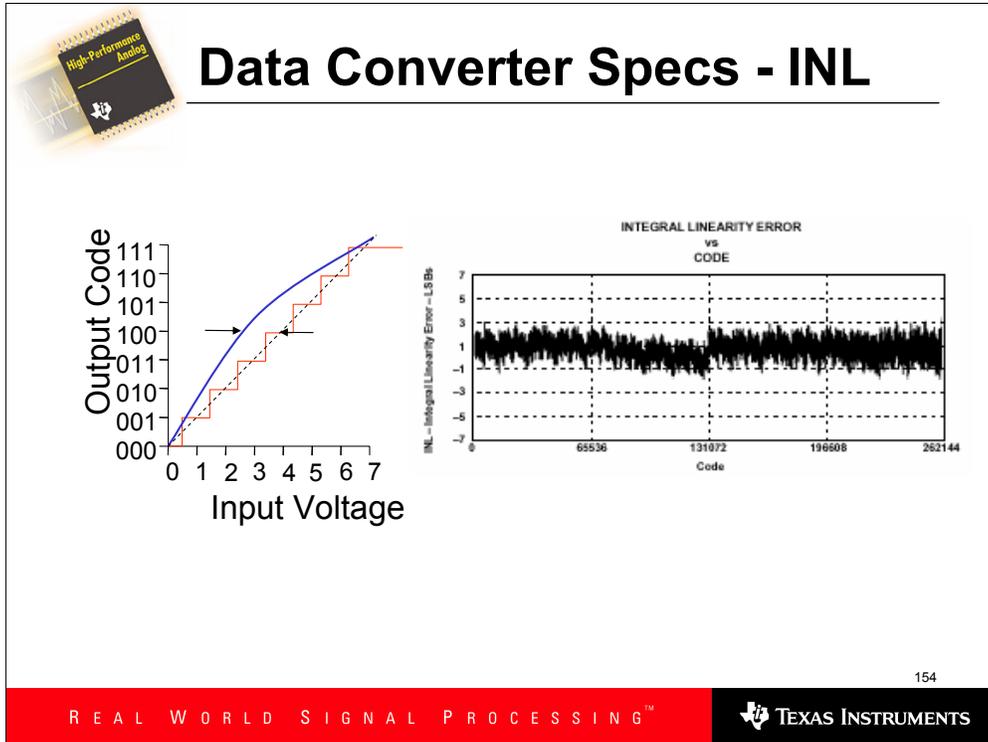
The resolution of the converter doesn't indicate the accuracy of the A/D. We'll talk more about this later.



DNL (differential nonlinearity) specifies the deviation of any code in the transfer function from an ideal code width of 1 LSB. DNL is determined by subtracting the locations of successive code transition points after compensating for gain and offset errors. A positive DNL implies that a code is longer than the ideal code width. A negative DNL implies a code is shorter than the ideal width. DNL is measured in the increasing code direction of the transfer curve. The transition of code N is compared to that of Code N+1.

A DNL error of less than -1LSB implies that at least one code is missing, meaning that there is no analog voltage which will generate a particular code. Most manufacturers will include a “NO MISSING CODES” specification.

A modern SAR A/D converter uses an array of capacitors and a comparator to determine the value of each bit in the conversion result. Variations of the individual capacitors will produce periodic fluctuations in the DNL data. These variations can be seen in DNL vs Code plots of a datasheet.



INL (integral nonlinearity) is defined as the integral of the DNL errors: good INL guarantees good DNL. Some datasheets only specify INL. INL error tells us how far away from the ideal transfer function value the measured converter result is.

Unlike Gain and Offset Errors, INL and DNL errors can not be calibrated or corrected; they are inherent in the design and manufacture of the converter.



Calculating Accuracy from INL

Device Name	RESOLUTION (# BITS)	MAX INL (LSB)	Best Case Accuracy (%)
Device 1	16	6	0.0091553
Device 2	16	5	0.0076294
Device 3	16	4	0.0061035
Device 4	16	3	0.0045776
Device 5	16	2	0.0030518
Device 6	16	1	0.0015259
Device 7	16	0.5	0.0007629

Device Name	RESOLUTION (# BITS)	MAX INL (LSB)	Best Case Accuracy (%)
ADS8345	16	6	0.0091553
ADS8383	18	7	0.0026703
ADS8402	16	3.5	0.0053406
ADS8325	16	4	0.0061035
TLV4541	16	2.5	0.0038147

Ideal Accuracy of Converter	
# BITS	Accuracy(%)
10	0.0976563
11	0.0488281
12	0.0244141
13	0.0122070
14	0.0061035
15	0.0030518
16	0.0015259
17	0.0007629
18	0.0003815
19	0.0001907

Best Case Accuracy of N-bit Converter

$$\frac{\text{MAX INL}}{2^N} \cdot 100 =$$

Where N is # of Bits

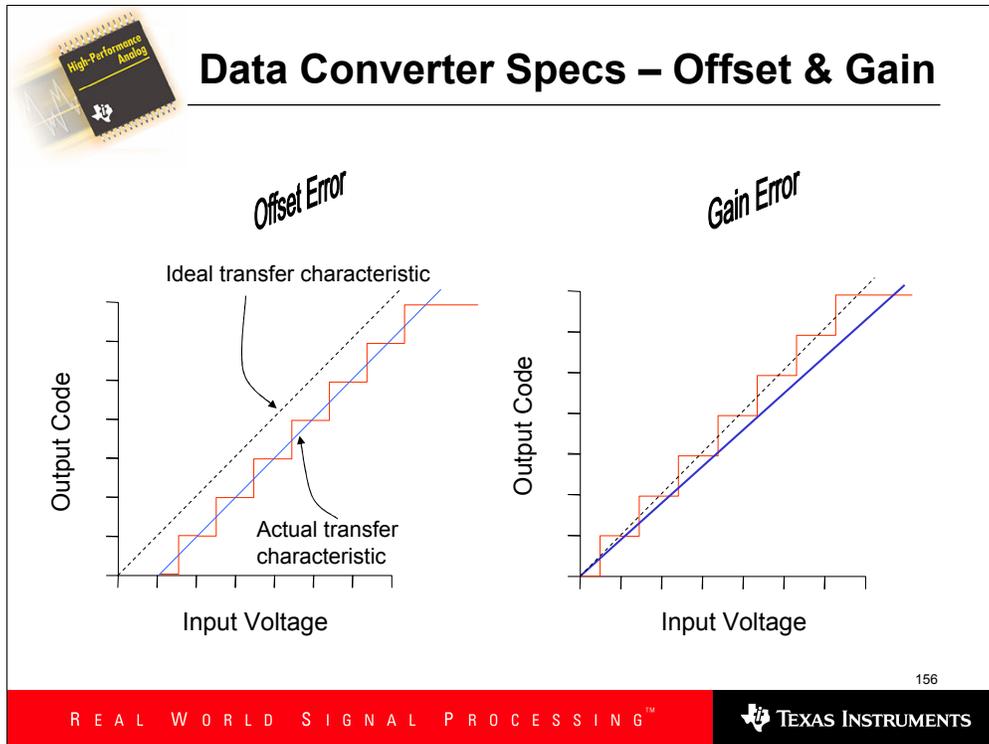
$$\frac{1}{2^N} \cdot 100 = \text{Ideal Accuracy of N-bit Converter}$$

Where N is # of Bits

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Using the MAX INL specification, we can calculate best-case accuracy. We can see that the 18-bit ADS8383 converter is accurate to between 15 and 16-bits.

Does a converter having more resolution (bits) than accuracy make any sense? Of course it does. In many applications, overall accuracy is not a prime consideration – detecting changes in a signal may be more important in a control loop, for example. In our measurement system, overall accuracy does factor in, but having more bits than accuracy is not a problem.



Offset Error is defined as a deviation of the code transition points that is present across all output codes. This has the effect of shifting the A/D transfer curve to the right or to the left. Offset Error is measured by finding the difference between the actual location of the first code transition and the desired location of the first transition.

Gain Error determines the amount of deviation from the ideal slope of the A/D transfer curve. It is important to note that before measuring Gain, Offset Error must be measured and subtracted from the conversion result. Gain error is determined by finding the location of the last code transition and then comparing it to the ideal location.



Offset Correction

- +1mV offset = 64LSBs
 - Subtract 64 from conversion results
 - Reduces dynamic range
 - FSR = $4.096(262080/262144) = 4.095V$
 - Any value above will overrange!
- -1mV offset
 - Signal of at least 1mV needed to get output
 - Dynamic range also reduced

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Correcting for offset error seems simple, but can be challenging. If the offset is positive then applying zero volts to the input will yield the offset error as the conversion result. Unlike bipolar systems, you use part of the A/D input range. If the offset is negative you can't simply apply zero volts and expect the result of the conversion to be the offset error. With a negative offset error, you must increase the voltage slowly until the A/D conversion result is greater than zero. Here again you use part of the A/D input range.

How does offset error work into our accuracy calculations?

If the offset error is 1mV, with a 4.096V reference this corresponds to $(1mV * 4.096/2^{18}) = 64LSBs$ of error for this 18-bit ADC. You must subtract 64 codes from each conversion result to compensate for offset error. So the actual full scale range is now $4.096 * (262080/262144) = 4.095V$. Any Value above this will over-range the A/D. So the dynamic range of the A/D has been reduced.

If the offset error is -1mV, then a small analog input value will not register with the converter. Only when the analog input is +1mV will the converter produce a non zero result. This has also reduced the dynamic range of the A/D.



Gain Correction

- Adjust reference voltage, or
- Apply a correction:

– where
$$y = \frac{M1}{M2} x$$

- M1 is slope of ideal transfer function
- M2 is slope of actual transfer function
- Example: Gain error = +0.06% FS = 157LSBs
 - So upper (157* 15.625μV) =2.453125mV is unused
 - But a full scale code will be output
- Example: Gain error = -0.06% FS = 157LSBs
 - So upper (157* 15.625μV) =2.453125mV is unused
 - With full-scale input applied, 261987 output, not 262144

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If the gain error is negative, then when a voltage greater than full scale is applied the conversion result will result in a full scale code. If the Gain error is positive, then when a voltage less than the voltage for full scale is applied the conversion result will yield a result of full scale code. One of the ways to adjust for gain error is to adjust the reference such that at a specific reference voltage the output gives full scale. Is it also possible to correct this error in software. The price you pay for doing it this way is a potential loss of some dynamic range. Here is an example of where having more bits than accuracy can be helpful.



The Final Analysis?

$$\begin{aligned} \text{Total Gain Error} &= \sqrt{UFE^2 + AAF^2 + REF^2 + ADC^2} \\ &= \sqrt{2815^2 + 917.5^2 + 524^2 + 157^2} = 3010LSB \end{aligned}$$

$$\begin{aligned} \text{Total Offset Error} &= \sqrt{UFE^2 + AAF^2 + BUF^2 + ADC^2} \\ &= \sqrt{35.2^2 + 6.4^2 + 192^2 + 48^2} = 201LSB \end{aligned}$$

$$\begin{aligned} \text{Total Drift} &= \sqrt{UFE^2 + REF^2 + BUF^2} \\ &= \sqrt{65.6^2 + 13.1^2 + 32^2} = 74LSB \end{aligned}$$

$$\begin{aligned} \text{Total Noise}|_{100kHz} &= \sqrt{UFE^2 + AAF^2 + REF^2 + BUF^2} \\ &= \sqrt{0.16^2 + 0.2^2 + 0.5^2 + 0.7^2} = 0.89LSB \end{aligned}$$

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At this point, we now need to consider the overall accuracy of our system. Totaling up all of the errors we've calculated, we find the total errors.

Gain and offset can be compensated for by doing a system calibration.

This leaves the drift and noise as our potential error sources. Note that the noise is still less than 1LSB.



A/D Noise

- SNR A/D = 87dB
- $\text{SNR A/D} = 20 \text{ Log}_{10} (V_{\text{INrms}}/V_{\text{noiserms}})$
- $V_{\text{IN}} = 4.096V_{\text{PP}} = 1.45V_{\text{rms}}$
- $\text{A/D } V_{\text{noise}} = 64.8\mu V_{\text{rms}} = 4.14\text{LSB}$

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The A/D converter we've chosen has an SNR of 87dB. Calculating this back into LSB, we see that the total noise contributed by our system is still significantly less than the noise of the ADC.



System SNR

- SNR System =
$$20\text{Log}_{10} \{ [V_{\text{IN,rms}}] / \sqrt{[(\text{ADC } V_{\text{noise}})^2 + (V_{\text{noise}})^2]} \}$$
- SNR System =
$$20\text{Log}_{10} \{ [(4.096\text{Vpp}/2)(0.707)] / \sqrt{[(64.8 \mu\text{Vrms})^2 + (11\mu\text{Vrms})^2]} \}$$
- SNR System = 86.9dB

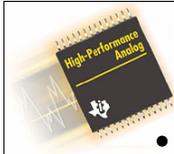
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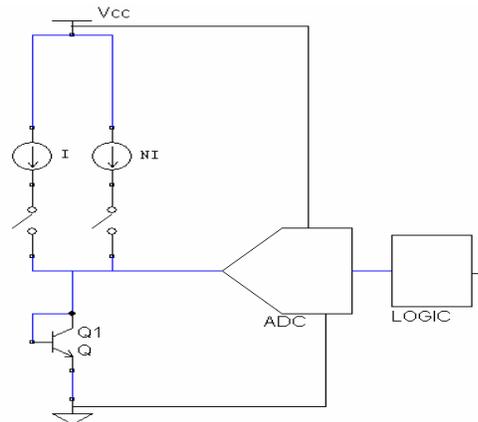
Combining these two noise figures, we find that our signal conditioning hasn't really harmed our overall system noise performance. The limiting factor is the ADC.

The only factor left to deal with is the drift. We can correct for this by measuring the temperature and correcting using a lookup table, for example, or we can factor it into our overall system error. The drift would amount to just over 1mV over the entire 0 to 50°C range.



Correcting for Drift

- Measure temperature
- TMP10x, TMP12x



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If we wanted to measure and correct for temperature, a simple system solution would be to use one of our digital temperature sensors. These devices measure the temperature of the silicon junction inside the device itself, and then converts this to a digital output available over either an I²C or SPI serial bus.



Silicon Temp Sensors

- -55°C to 125°C (150°C)
- ~~Cold junction compensation~~
- ~~Linearization~~
- Digital-Out
 - ~~ADC, comparator~~

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The advantage of a sensor of this type over thermocouples is that no linearization or cold junction compensation is needed. Since the output is digital, an extra ADC or ADC channel is not required to measure the temperature either.



TMP100/101 – I²C Interface

- Specified Accuracy:
 - $\pm 0.5^{\circ}\text{C}$ from -25°C to $+85^{\circ}\text{C}$ (typ)
 - $\pm 3^{\circ}\text{C}$ from -55°C to $+125^{\circ}\text{C}$ (max)
- I²C/SMBus compatible
 - Programmable 9 – 12 bit resolution
 - TMP101 – programmable High/Low Set Points
- SOT23-6
- 50 μA

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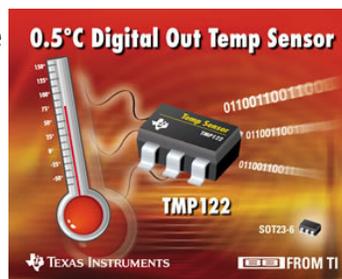


The TMP100 and TMP101 feature high resolution and accuracy over the full temperature range, and comes in a tiny 6-pin SOT23-6 package.



TMP121/122 – SPI Interface

- Specified Accuracy:
 - $\pm 0.5^{\circ}\text{C}$ from -25°C to $+85^{\circ}\text{C}$ (typ)
 - $\pm 1.5^{\circ}\text{C}$ from -40°C to $+85^{\circ}\text{C}$ (max)
- TMP121 – Read Only
 - 12-bit resolution
- TMP122 – Programmable
 - Resolution 9-12 bits
 - High/Low Set Points
- SOT23-6
- $50\mu\text{A}$

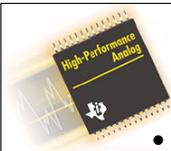


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Our latest temperature sensors feature an SPI interface, and better accuracy. Any of this family of parts could be used to provide a temperature measurement for use in compensating drift in software.



Interfacing to Processors

- Serial Interfaces
 - Occupies little board space, thus lowering cost
 - Generally easy to wire up to processors
 - Slower interface compared to Parallel
- Parallel Interfaces –
 - Faster interface compared to Serial
 - Dumps large switching currents into ground plane
 - Takes up more board space
 - Unique interface to each processor?

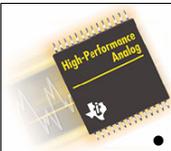
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Once the performance/accuracy related decisions are made as to which converter to design in, the next step is to think about how to interface the converter to a processor. In the next few slides we'll look at serial and parallel interfaces.

Serial converters typically have from 2 to 4 lines to route, which saves PCB real estate. Interfacing is more or less the same from one processor to the next. Parallel Converters take more board area, but generally have faster interfaces. The faster interface will generate large currents into the ground plane. Interfacing to a processor can be a little more complicated because processors don't all have the same memory and address bus architectures.



Some Questions to Ask

- How will I trigger a new conversion?
 - CPU?
 - Timer/PWM?
 - DMA?
 - External Source?
- How will I read from the converter?
 - CPU?
 - DMA?
 - External source?

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A SAR converter must be told when to convert (note: not ALL A/D converters need to be told when to start a conversion!). How will you trigger conversions?

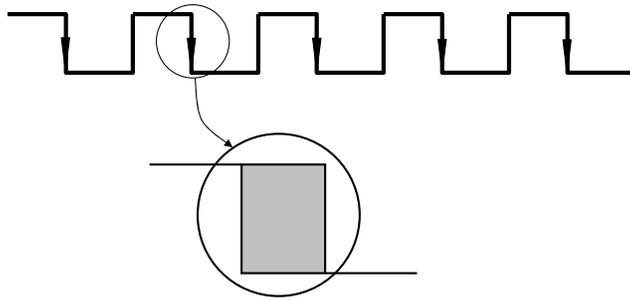
There are several ways you can trigger a conversion. You can use the processor to control the conversion start under program control, or use a Timer or PWM output. Perhaps your processor has a DMA triggered by the CPU or Timer. Maybe the processor shouldn't be involved at all, and external source like clocked FPGA logic should be used. We'll examine some of these in the next few slides.

How will you read the digital code out of the converter? You can use the processor via polling or an interrupt service routine. You can use a DMA triggered by an interrupt from the converter. Or maybe that FPGA can also collect the data into a FIFO buffer for your processor to come along and read at its convenience.



Triggering a Conversion

Sampling jitter is the error in the placement of each clock edge controlling the point when sampling begins.



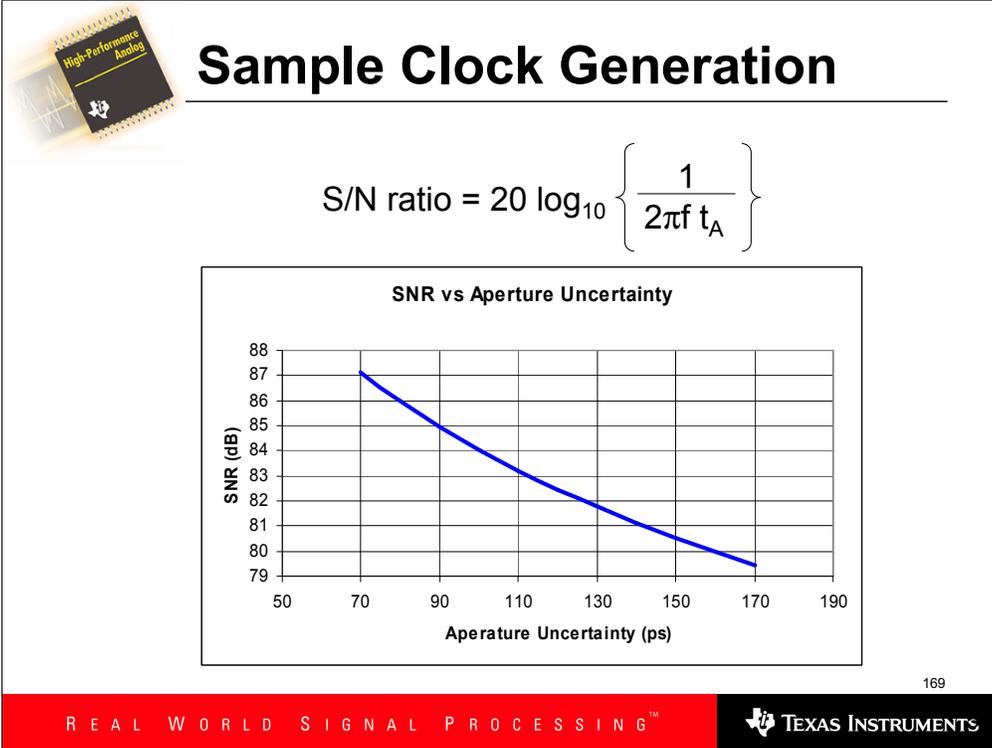
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Sampling jitter is also an important point that should be considered during the design phase – although there may be little that you can do to influence it.

The effect of jitter is to set a limitation on the maximum frequency of input sine wave, because it defines the maximum slew rate of that signal.



Let's assume your task is to digitize a signal with a frequency range of zero hertz up to a few kilohertz, say 100kHz. How much jitter can you tolerate and still accurately digitize a 100kHz sine wave?

The tolerable aperture uncertainty – that is, the uncertainty of the exact moment the sample is taken – can be calculated from the equation above, where f is the frequency of the sine wave you are digitizing, and t_A is the total uncertainty. t_A would include both the aperture uncertainty of the data converter itself, as well as whatever sampling jitter may be present in your convert start signal.

In the case of our ADS8383, the converter SNR is listed at 87dB. From this graph, we can tolerate up to 70ps of uncertainty before we begin to degrade SNR for a 100kHz sinewave input. The ADS8383 has 15ps of aperture uncertainty in the device itself. This leaves 55ps for your design to have without affecting the SNR.



How will you trigger a new conversion?

- Microcontroller Triggered
 - Complete control over the trigger to begin conversion cycle, but...
 - Interrupts may cause jitter.
 - Microprocessor horsepower taken up constantly servicing the A/D.

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Microprocessors and microcontrollers come with all kinds of features. The processor is always an option as a trigger to start a conversion cycle. The microcontroller can write to an address, a serial port, or toggle a pin to start a new conversion.

When high frequency signals are being digitized the jitter of this external trigger becomes very important. Using the microcontroller to start a new conversion periodically may not be possible. The processor maybe involved in other tasks when an interrupt comes which tells the processor to start another conversion. For example, say a 500kHz timer interrupts the processor to tell it to start another conversion. The processor has to halt what it's doing, pop the registers onto the stack and then go start another conversion. If in the next cycle, an interrupt with a higher priority comes along, the processor will go attend to that interrupt routine and then later service the timer interrupt. What's happening is that from cycle to cycle the processor is not very periodic. If the sample rate isn't periodic, the analog signal can not be accurately represented.

This isn't a problem if you're measuring slow signals like temperature. It doesn't matter if you measure a thermistor every $2\mu\text{S}$ or $200\mu\text{S}$: the signal isn't going to change very much in that time. But if you're measuring vibration and want to accurately digitize the signal, then it's really important that the processor start conversions at precise intervals.

To many fast processors, the A/D is a very slow device. A DSP could be running at 225MHz, and asking it to service a 500kHz analog-to-digital converter is not the most efficient use of the processor.



How will you trigger a new conversion?

- Timer/PWM
 - Programmable
 - Processor Interrupt-able
 - Desired frequency may not be possible due to processor clock frequency.
 - It is a programmable output signal
 - Periodic

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We just talked about how a processor may not be able to start conversions periodically because it's been interrupted or is busy executing another function. One option for designers is to use a timer in the processor to generate an interrupt to the processor. If no higher priority interrupt occurs, you can be assured the processor will break and execute the timer interrupt service routine which you've written to start a new conversion.

Another option which many microcontrollers and motor-control type DSPs offer is a PWM timer. The output signal itself can be programmed to be your conversion start signal (for converters offering an external pin for conversion start). Using the PWM/Timer output directly as the convert start signal, frees the processor completely to execute other more important functions.



How will you trigger a new conversion?

- Timer via Processor?
 - Serviceable ISR
 - Some latency to when CPU can respond to ISR.
- Timer via DMA?
 - Direct transfer into memory.
 - Frees CPU to execute other functions.
- External Source
 - FPGA

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If a timer is used, you still have some options to consider:

You can use a Timer interrupted interrupt service routine to start a conversion. If doing this, you'll need to design your algorithm such that jitter between each successive conversion start is no more than 55pS (assuming your digitizing a sine wave). 55pS jitter from a processor function may or may not be a option for you.

If your processor has a direct memory access (DMA) feature, then you can consider using the DMA to generate a periodic conversion start pulse. Again if you are digitizing a 100kHz signal, you'll need ensure the jitter is less than 55pS.

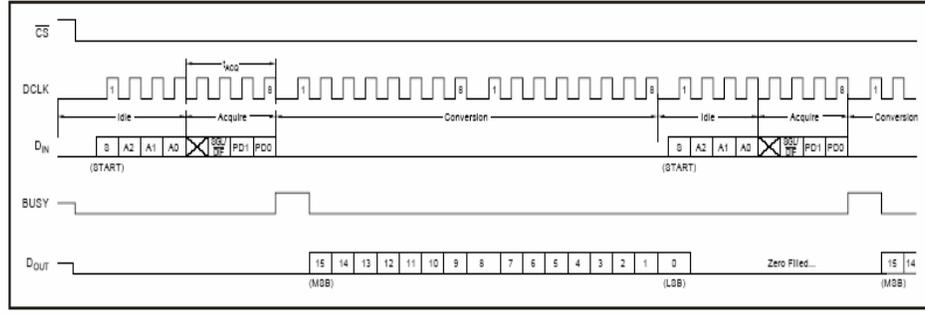
If your processor offers a PWM/Timer, you may be able to bypass the peripherals and processor and directly drive the convert start pin of the converter. Again you need to ensure jitter is less than 55pS.

In all of these cases, it may not be possible to get a low jitter clock from a processor. Your final option maybe to use external source like a CPLD or FPGA synchronized to a low jitter clock. It is common to use a CPLD/FPGA when multiple converters are in the system. This last option leaves it to you to find and create a low jitter control system for the converter.



Conversion Start Trigger- Serial

- Serial Converters often start the conversion upon reception of a specific bit pattern



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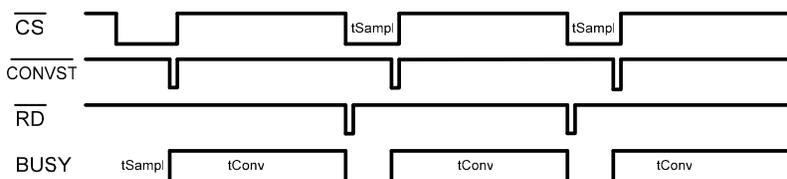

In serial data converters often times it's the CPU which initiates conversion cycles. Controlling jitter precisely for these converters, driven from the processor's serial port, is a challenging task. It means you will have to pay close attention to timing and interrupt overhead.

The Multi-channel serial ports (McBSP) on TI DSPs give users the option of programming the sample rate directly. The sample-rate generator of the McBSP can be programmed to trigger a new conversion periodically. The resolution of the conversion period is dependent on the processor clock rate. Therefore the sample rate will be a submultiple of the processor clock. Some DSPs will allow for an external clock input, using this option you can set the sample rate to whatever you wish.



Conversion Start Trigger- Parallel

- Usually have to pull a pin low to initiate conversion.



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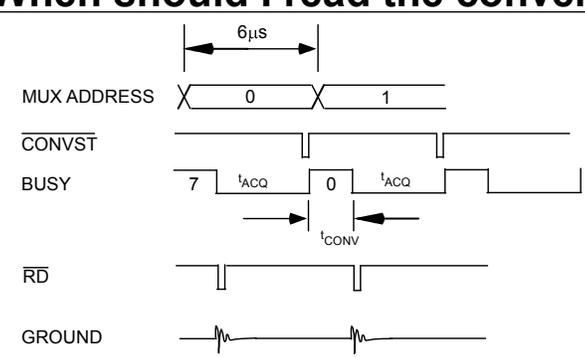
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Most parallel-interface converters have a convert start pin ($\overline{\text{CONVST}}$). Pulling this pin low for a brief period of time takes the converter out of sample mode and holds the signal on the internal sampling capacitor, and triggers a new conversion.



When should I read the converter?



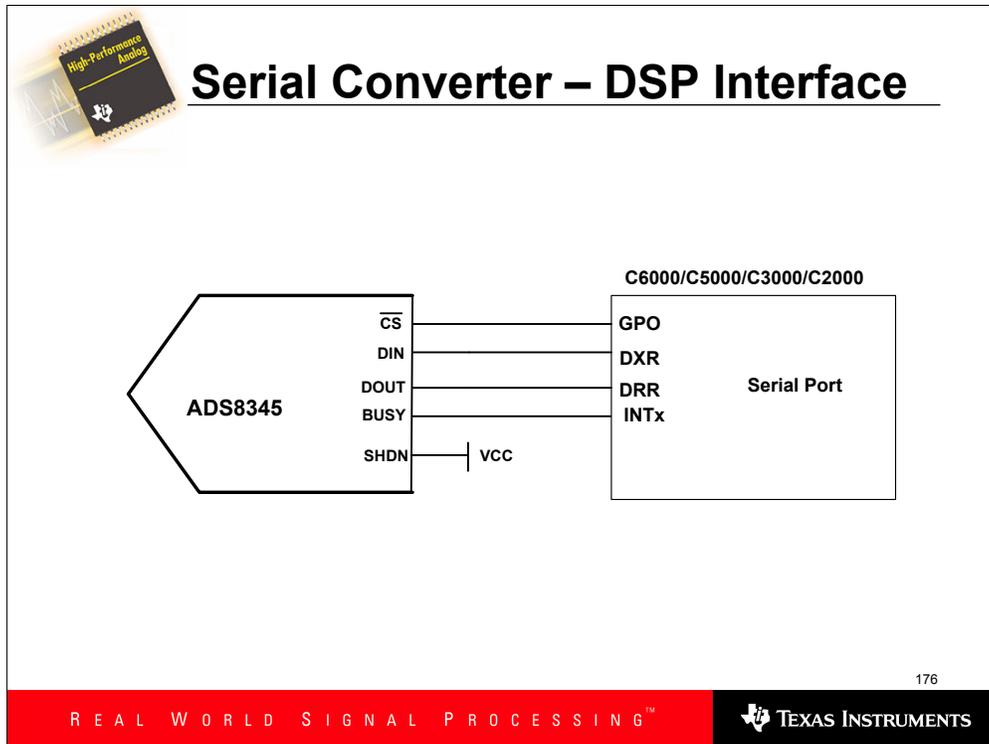
- As soon as possible before next conversion
- Parallel interface dumps large current into ground

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Reading the data out of an A/D converter with a parallel interface poses an interesting problem. When the parallel interface is enabled to read the digital data is put out on the bus, several digital drivers simultaneously switch. This can cause a large amount of current to flow in ground traces, and potentially disturbs the ground potential. If this is going on while attempting to acquire the next sample, this noise could corrupt the input signal. You want the ground plane, and system as a whole to be as quiet (free from switching currents) as possible during acquisition time.

Serial converters generally are clocking out their data at the time the conversion is taking place, and no acquisition is happening. Moreover, the serial interface is only moving a few digital lines, so the current dumped into ground is smaller than the parallel case.

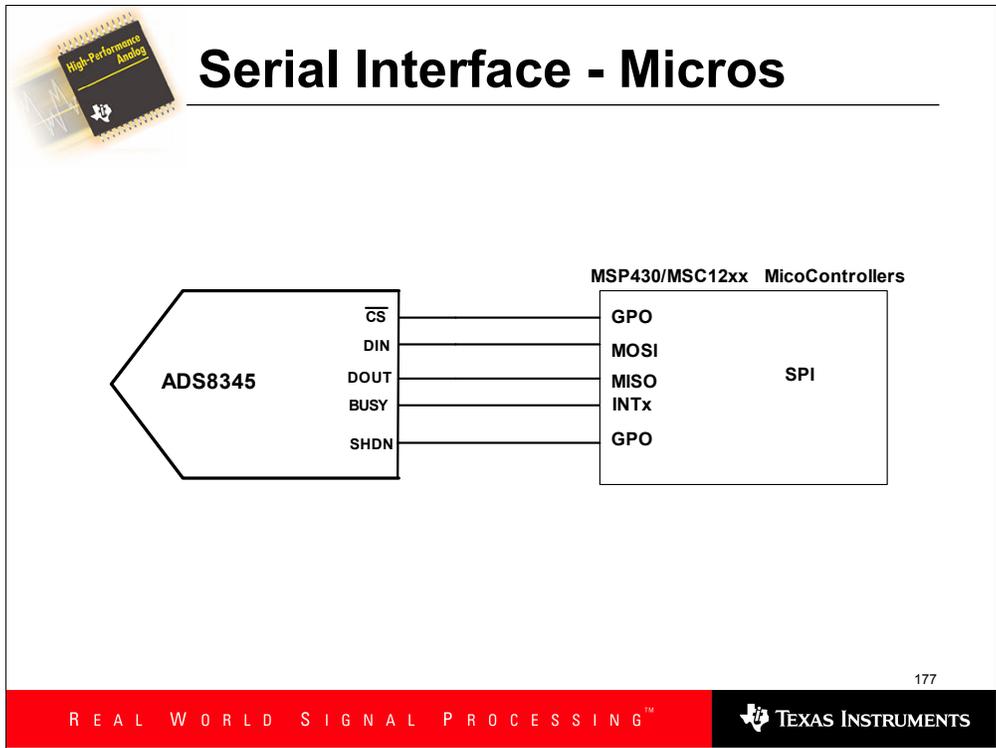


Shown here is a SAR type serial 16-bit 100kHz converter interfaced to the multi-channel buffered serial port (McBSP) on a Digital Signal Processor (DSP) from Texas Instruments. The McBSP can be programmed to emulate the standard DSP serial port, SPI port, or a host of other serial interface standards.

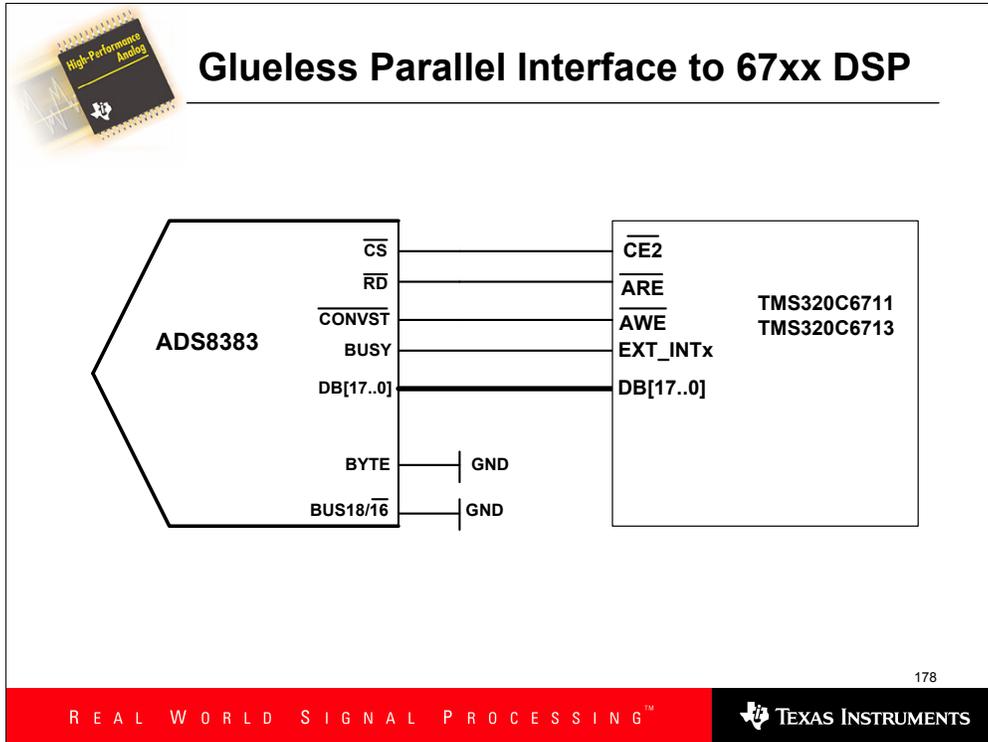
McBSPs can be found on most of the modern Digital signal processors from TI.

Generally /CS is tied to a general purpose output pin. The DATA IN (DIN), DATA OUT(DOUT) lines are wired to data transmit and data received pins. BUSY can be wired to an interrupt pin of the processor, or left floating.

If the application calls for the converter to be active only for short amounts of time, the SHUTDOWN (SHDN) pin of the converter can be tied to a general purpose output pin of the processor. Placing the part into shutdown mode can reduce current consumption by more than two orders of magnitude.



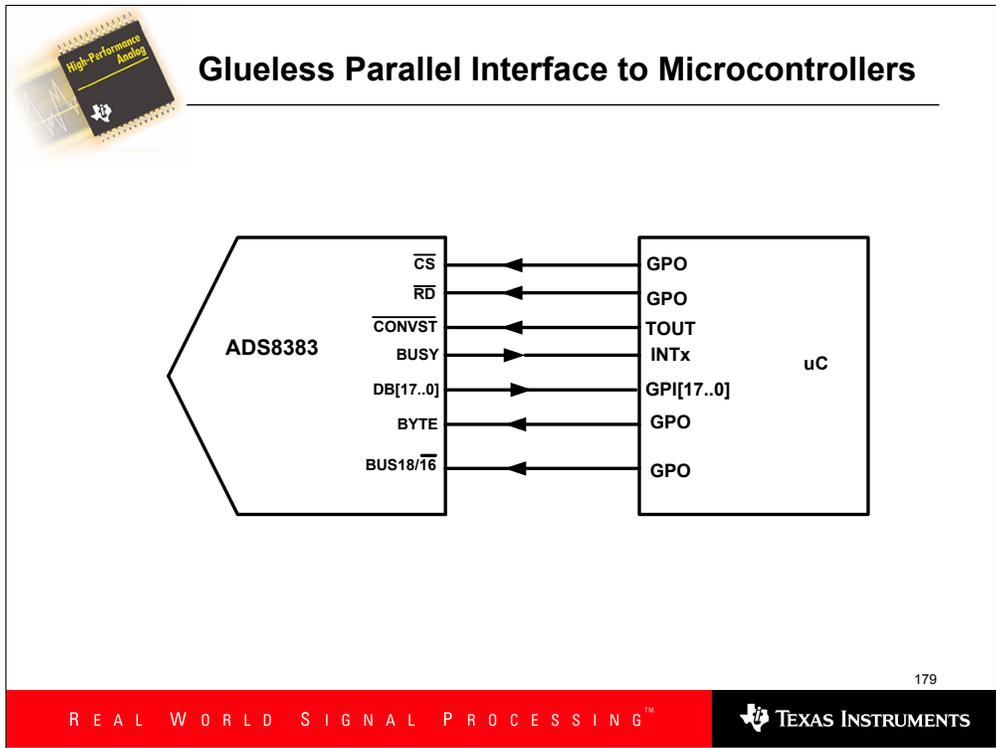
The serial interface to Micro controllers like the MSP430 or the MSC1210 are very similar to the DSP interface just discussed. Like the DSP serial interface case, the chip select signal is tied to general purpose output pin of the micro-controller. DIN is connected to Master Out Slave In(MOSI) pin. DOUT is wired to Master In Slave Out (MISO) pin of the serial port. BUSY can be tied to a interrupt pin, left floating or to a General purpose input pin for polling. The SHDN pin can be tied high to always enable the device, or tied to a general purpose output pin.



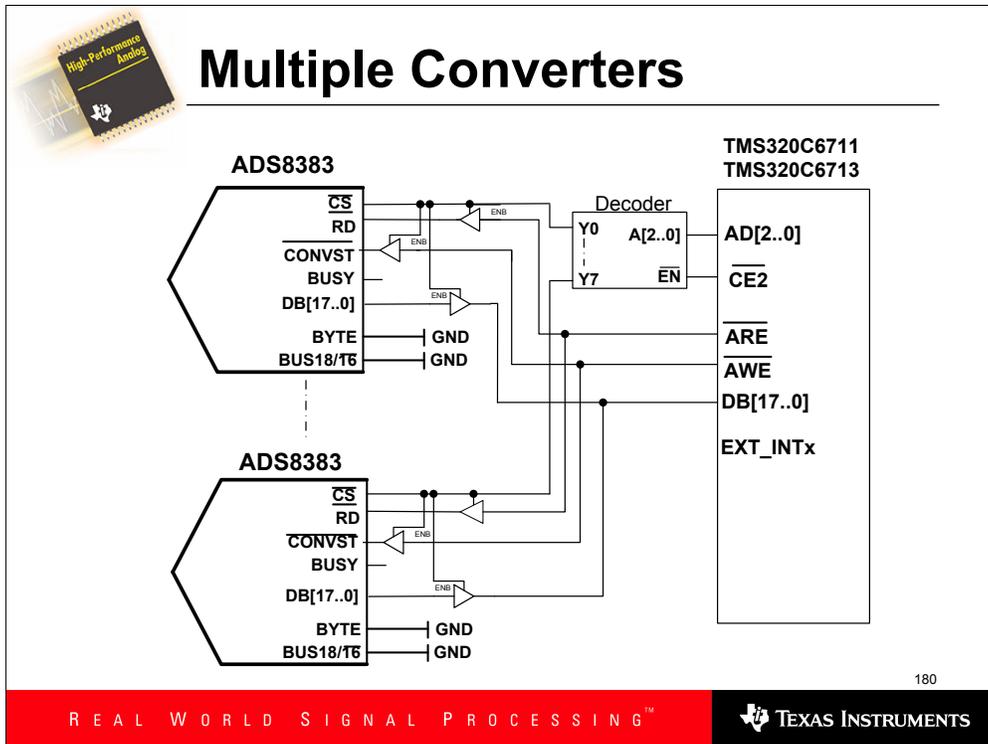
This is an example of a simple interface to a DSP. It's completely glueless. This type of interface may be satisfactory for some DC measurements, but the timing issues highlighted previously may make this unsuitable for cases where the tolerable jitter on the convert start line is low. Most DSPs have peripherals that can be programmed to periodically trigger a conversion and read from the converter.

In the case of the ADS8383 interfaced to the c6713, the EDMA controller can be triggered off a timer to start new conversion cycles at fixed rates. The EDMA channel is dedicated to this purpose, so the conversion start pulses will be periodic. The CPU is not involved at all.

With parallel interfaces that hang off a shared bus, noise on the digital bus can be capacitively coupled into the substrate of the converter, so you may want to isolate the chip from the bus with a buffer to keep the noise around the converter low.



This is an example glueless interface to a Micro controller. If the converter is on a shared bus, it's best to digitally isolate the converter control and data lines from the bus. Otherwise noise on the digital bus will get capacitively coupled into the substrate causing conversion errors.



Here is a recommended interface to a parallel bus for multiple converters.

You'll notice all digital lines to the converter are isolated from the bus.

What's missing in this figure but is recommended are small RC networks on /CS, /RD, and /CONVST. The RC should be adjusted to remove any overshooting and/or undershooting. Significant ringing on the control lines can appear to cause an offset problem, because the ground bounce is affecting the conversion result.



Layout and Grounding

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We really could do an entire seminar on layout and grounding. Even then, we wouldn't necessarily address the myriad possibilities of what your designs present. What we can do briefly is give you some guidelines to follow in your own designs.

Grounding

ANALOG Ground

DIGITAL Ground

- Analog Ground should be kept free from digital “noise”.
- Analog Ground includes signal conditioning circuits, voltage references and the analog power source for the data converter

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Grounding – why is it important?

As with any analog circuit, grounding considerations are critical for reliable data converter designs. For ADCs and DACs, it is essential to have a solid ground reference on the analog side of the device. This includes the analog power connections and reference connections, as well as the analog inputs. Analog ground has to be tied back to the analog inputs to reduce common-mode noise.

This does not imply, however, that the digital section can be ignored. The high currents associated with digital signals can cause ground bounce or “switching noise” which adversely affects the analog section of the data converter. A few millivolts of noise can correspond to hundreds of counts of error in a 16-bit system.



The Chip

PIN CONFIGURATION

Top View SSOP

ADS8361

1	DGND	+V _D	24
2	CH B1+	SERIAL DATA A	23
3	CH B1-	SERIAL DATA B	22
4	CH B0+	BUSY	21
5	CH B0-	CLOCK	20
6	CH A1+	CS	19
7	CH A1-	RD	18
8	CH A0+	CONVST	17
9	CH A0-	A0	16
10	REF _{IN}	M0	15
11	REF _{OUT}	M1	14
12	AGND	+V _A	13

Analog Inputs

Digital control

Internally, the chip is separated into distinct analog and digital sections.

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Careful planning of the layout for a high-resolution data converters actually begins long before the design engineer ever has a part in his hands.

Chip designers often spend a great deal of time and effort on the actual layout of the silicon in order to get the desired performance from the device.

The analog and digital sections are normally well defined on the actual substrate in order to minimize the effects of switching noise on the analog circuitry.

Split or Solid?

Analog
Digital

- Partition the board into Analog and Digital sections when the layout permits.
- Split the ground plane if needed – but don't if you don't have to!

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Split or Solid

To eliminate, or at least minimize, the effects of ground disturbances in high-resolution systems, carefully planned ground schemes are necessary. While people may argue as to whether a “split” ground or “solid” ground plane provides the best performance, isolation and/or filters between the analog and digital sections and well bypassed connections back to the system power supply are essential.

The board depicted on this slide has a distinct analog and digital section. This provides isolated ground structures which prevent the high-speed digital signals from finding a return path through the analog circuitry. However, we do provide a small ground plane underneath the actual converter.

You don't need a solid ground plane under the ADC in all cases - very often we put a very small (5-10mil) connection between the two under the ADC - just so the digital return currents from the ADC can flow back to analog side, since they are connected inside the ADC. There is no need for a big plane here, since these currents are small.

If the split goes completely through the ADC, then you can see that those return paths have to flow all the way down the board, through the power supply, and back up through the analog plane. This is what we're trying to avoid, since now digital signals are on the analog plane, and you have a much larger loop area, increasing the inductance and raising the potential for EMI.

Visualize Return Currents

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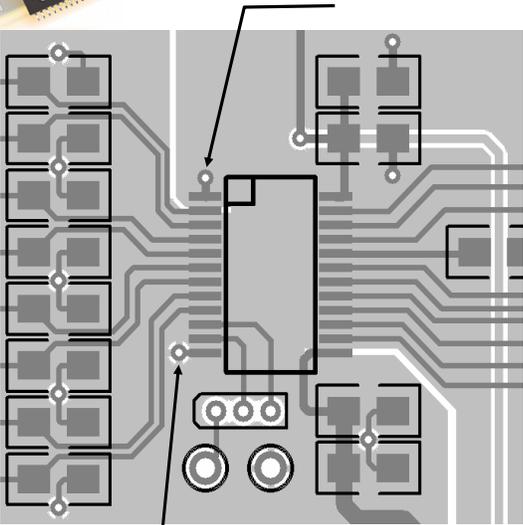
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The most important step you can take in making a good board layout is to visualize the return currents on your board.

Shown here in blue are the analog return currents, in red are the digital return currents, both as they transit the board trying to find their way back to the power supply ground. Note that on this board, we've done a good job of placing the components so that all the analog parts are on one side of the board, and the digital parts are on another. There is no place where the digital currents would need to cross the analog currents in their paths back to the supply.

Digital Grounding



- Keeping ground traces short:
 - minimizes inductance
 - reduces voltage differential between the board and chip substrate
 - improves noise immunity

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The digital circuitry needs to communicate with the main system. Digital communication involves the switching of ones and zeros. All this switching generally involves large return currents through the chip to the digital ground plane.

When the digital section is active, these currents tend to cause transient voltage differences across the substrate of the chip, and between device and the printed circuit board. The digital circuitry is designed to handle these voltage differences. The analog circuitry, however, is not.

The digital ground pin needs a solid, low impedance connection to the system ground. Avoid long traces whenever possible and keep analog signals away from this pin.

Common Ground

- Tie Analog and Digital grounds together at their source.

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Common Ground

Since both digital and analog “islands” are part of the same system, they must be tied together somewhere. The ideal place to do this is directly on the printed circuit board close to the source of the digital and analog power.

In split plane designs, a single bridge between the digital and analog planes is recommended. Poured ground planes should be tied in a star configuration.

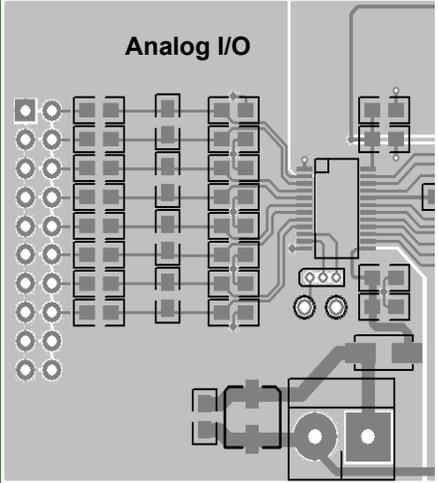
But here’s the exception to the rule: we put a very small (5-10mil) connection between the two planes under the ADC - just so the digital return currents from the ADC can flow back to analog side, since they are connected inside the ADC. Note that the proper place to connect the ground planes is at the supply - but you also need to have that small connection under the ADC. Does this give you a ground loop? Yes. Is it a problem? Probably not, since the only currents that will want to flow under the ADC are its own return currents!

This points out why many times, it's just easier and makes more sense to use a single ground plane, particularly if you can partition the circuit as we have shown into distinct analog and digital portions. If you don't have that luxury, then splits in the plane can help steer currents where you want them to go, and away from sensitive analog circuitry.



Starting the Layout

- Keep Analog I/O symmetrical
- Avoid putting heat sources near the Analog I/O
- Route Digital signals **AWAY** from the Analog signals



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As with a well-designed chip, the ideal board layout consists of well-defined analog and digital sections.

The analog inputs need to be kept short to minimize stray capacitance and inductance. This usually is not too difficult, since the analog circuitry tends to be point-to-point wiring. Symmetry in the analog I/O can improve channel-to-channel performance. By keeping the inputs symmetrical, system noise should remain nearly identical to each input. Symmetry also eases testing, troubleshooting and inspection tasks.

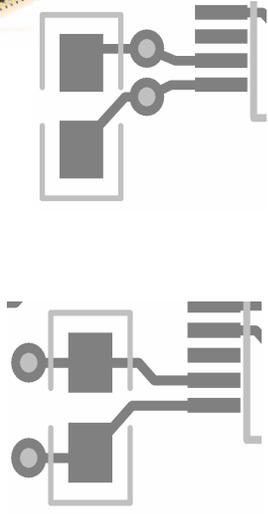
Keep reference circuitry and voltage regulators away from the analog I/O. This helps to reduce the effects of thermal noise and ensures that each analog channel has the same ambient environment.

If the analog and digital signals have to share a common connector, split the connector into a digital and analog section with high-speed clocks and analog inputs as far away from each other as possible.

Always route analog and digital signals away from each other. If your analog signals **MUST** cross digital signals, minimize the possibility of signal degradation by keeping the lines at right angles to each other. Do not allow any signal to cross between the analog and digital planes in a split plane design.



Bypass Caps



- Reduce high-frequency noise
- Keep them close to the power pin
- Route “into” the capacitor

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Bypass capacitors

Bypass capacitors are extremely important in reducing the effect of high frequency noise. Bypass capacitors should be kept close to the power pin it is decoupling. When feeding the power trace from an internal plane, put the via on the outboard side of the capacitor lead. Putting a via to the power plane between the capacitor and power pin can reduce the capacitors effectiveness. Ensure the capacitors have a short, low impedance ground return path as well.



Summary and Conclusions

- Be aware of the characteristics of the signal you want to digitize.
 - Highest Frequency component, rise time,...
- Choose the data converter that meets the specifications that are most important to you.
 - Static or Dynamic specs, Channel count, Speed, Power consumption, Size,...
- Condition and Buffer your analog input(s).
 - Bring signals into the range of your converter
 - This presents a stable, known output impedance to the ADC.
- Understand the role support circuits can play in achieving optimum performance.
 - Voltage reference, Anti-aliasing filter, Low-jitter clock
- Plan PWB fabrication with care
 - Layout, Grounding, Filtering

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