DEM-DAI1850/1851EVM

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1 Description

The DEM-DAI1850/51EVM is an evaluation board for the 96-kHz, 24-bit PCM audio analog-to-digital converter (ADC) with a 6-channel multiplexer, PCM1850/51, with digital audio transmitter, coaxial and optical digital output connector, system clock generator, programmable input filter section, and various mode control switches.

The DEM-DAI1850/51EVM operates with single 5-V analog power supply and supports 6 channels of stereo inputs with up to 2.4-Vrms unbalanced analog input capability.

The DEM-DAI1850/51EVM also supports a programmable low-pass filter in an input filter section so that evaluation can be done under application conditions with end-equipment.

1.1 Block Diagram

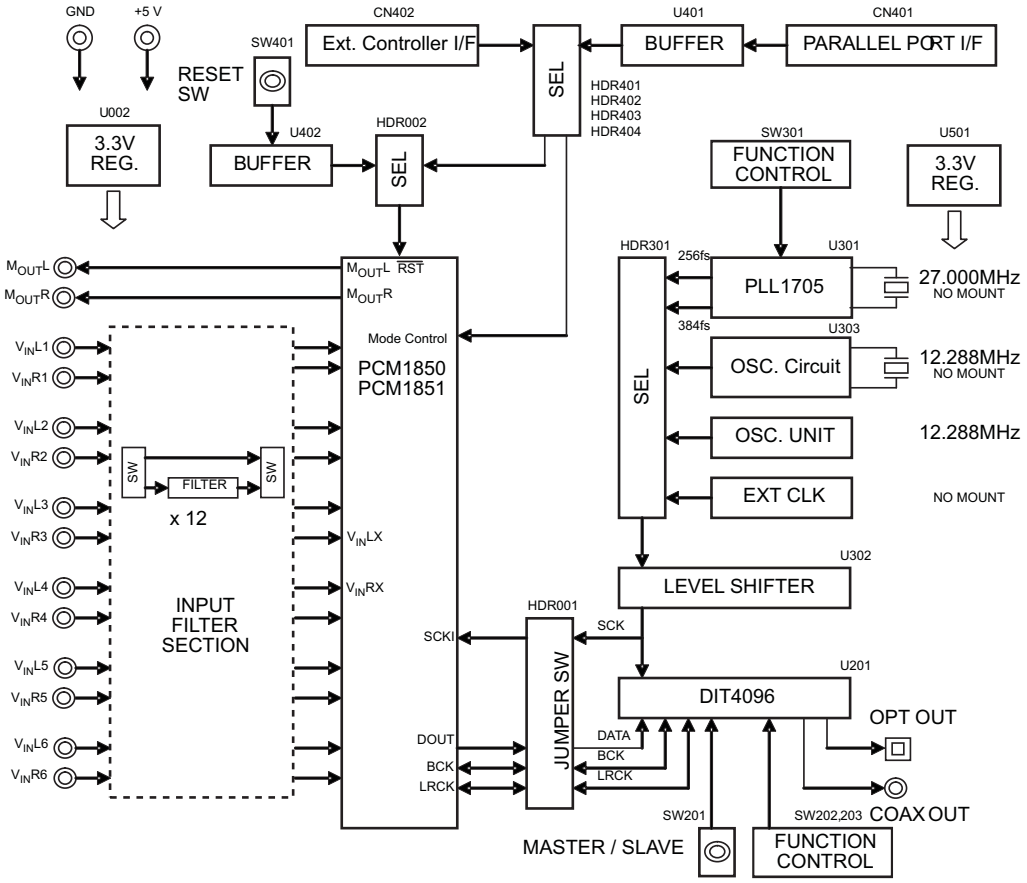


Figure 1. DEM-DAI1850/1851 Block Diagram

1.2 Basic Connections and Operations

DEM-DAI1850

- Install the demonstration software that is provided on the CD-ROM. Copy *VBRJP200.DLL*, *INPOUT.DLL*, *VER.DLL*, and *REGTEST* into any common folder that is desired.
- Connect the printer cable between the parallel port of the personal computer (PC) and this evaluation board.

DEM-DAI1851

- Prepare the host controller or PC and appropriate I^2C control software which can control DEM-DAI1851.
- Install pullup resistors on the SDA and SCL ports, which meet with I^2C port configuration of controller, and connect the evaluation board with the controller through connector CN402 on the board.

In-Common DEM-DAI1850/51 Connections and Operations

- Apply 5-V power supply, appropriate analog input signal on CH1, and then observe analog signal on MOUTL/MOUTR or digital signal on OPT OUT or COAX OUT.

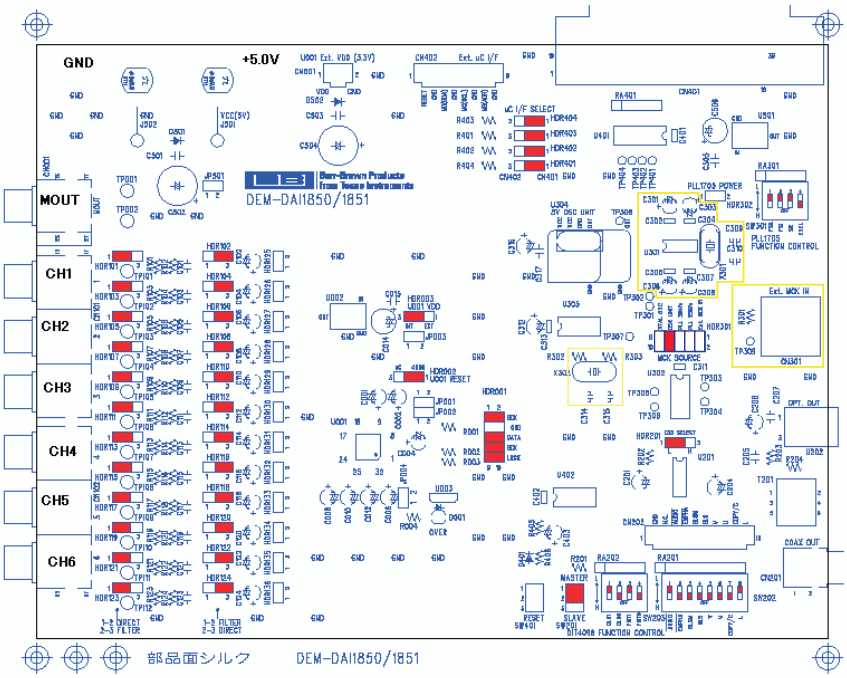
  As the PCM1850/51 is set in default state after power on, a signal on CH 1 can be observed on MOUTL/MOUTR. If the output signal cannot be observed on MOUTL/MOUTR, confirm the setting of the evaluation board, applied power supply voltage, and contact of parts on sockets. The test points TP401-TP404 are provided near the parallel connector for this kind of check.
- Send command by REGTEST through PC printer port (DEM-DAI1850) or by I^2C control software through CN402 (DEM-DAI1851).
- Evaluate and verify with various register setting for application condition of end-equipment.

1.3 Configuration Controls

1.3.1 Default

The default setting of the jumpers and switches for the DEM-DAI1850/51 is shown in red in the following illustration. The DEM-DAI1851 has a different setting on only the microcontroller I/F SELECT setting.

(The components inscribed by yellow lines are not mounted on the standard specification board.)



1.3.2 Reset Switch (SW401)

Send reset signal to DIT4096 and PCM1850/51, if *4096* is selected on HDR002, U001 RESET.

1.3.3 Master/Slave Switch (SW201)

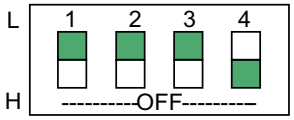
Select operation mode of U201, DIT4096.

MASTER : For operation of PCM1850/1851 in SLAVE mode, U201, DIT4096 must be operated in MASTER mode. (Default)

SLAVE : For operation of PCM1850/1851 in MASTER mode, U201, DIT4096 must be operated in SLAVE mode.

1.3.4 PLL1705 Function Control Switch (SW301)

Select the system clock frequency of PLL1705 (PLL1705 is not mounted on the standard specification board), effective when PLL clock is selected for MCK.



1: FS2 : fs selection 2

2: FS1 : fs selection 1

3: SR : Sampling rate selection, Low = Standard, High = Double

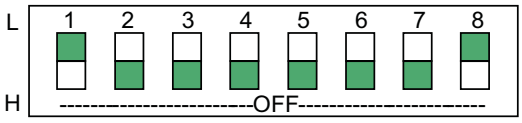
4: CSEL : SOCK01 frequency selection, not used in this evaluation board

Table 1. System Clock Frequency Configuration

FS2	FS1	SR	Clock (In Sampling Frequency)
OFF	ON	ON	32k
ON	OFF	ON	44.1k
ON	ON	ON	48k (Default)
OFF	ON	OFF	64k
ON	OFF	OFF	88.2k
ON	ON	OFF	96k

1.3.5 DIT4096 Function Control Switch (SW202)

Select DIT4096 operation mode and function (not required to change in general).



1: L : Generation Status

2: COPY/C : Copy Status Input / Channel Status Serial Data Input

3: U : User Data Input

4: V : Validity Data Input

5: BLS : Block Start I/O

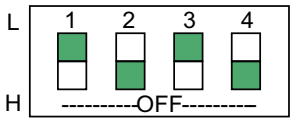
6: BLSW : Block Start Mode Control

7: EMPHA : Preemphasis Status

8: AUDIO : Audio Data Valid Control

1.3.6 DIT4096 Function Control Switch (SW203)

Control DIT4096 master clock selection and interface format selection.



1: CLK1 : Master Clock Selection 1

2: CLK0 : Master Clock Selection 0

3: FMT1 : Interface Format Selection 1

4: FMT0 : Interface Format Selection 0

Table 2. Master Clock Selection

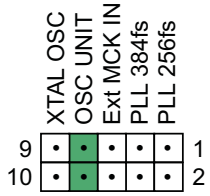
CLK1	CLK0	Master Clock
ON	ON	Unused
ON	OFF	256 fs (Default)
OFF	ON	384 fs
OFF	OFF	512 fs

Table 3. Interface Format Selection

FMT1	FMT0	Interface Format
ON	ON	24-bit left-justified
ON	OFF	24-bit IIS (Default)
OFF	ON	24-bit right-justified
OFF	OFF	16-bit right-justified

1.3.7 Master Clock Source Select (HDR301)

Select master clock source; change if clock sources other than crystal oscillator unit is used.



9-10 : Output of onboard oscillator circuit with X302, crystal of 12.288 MHz
(X302 is not mounted in standard specification board)

7-8 : Output of U304, crystal oscillator unit 12.288 MHz (Default)

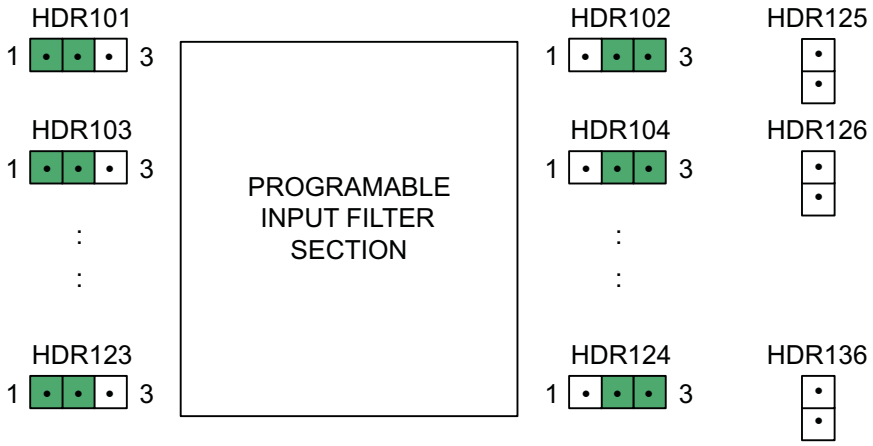
5-6 : External clock through CN301
(CN301 is not mounted on standard specification board)

3-4 : 384fs of U301, PLL1705
(U301 is not mounted on standard specification board)

1-2 : 256fs of U301, PLL1705
(U301 is not mounted on standard specification board)

1.3.8 Input Filter Select (HDR101-124)

Select input signal path to PCM1850/51, direct input (default) or via low-pass filter input. The filter response and input impedance of input filter section are programmable; detailed data appears in Section 1.3.15.



1-2: DIRECT INPUT (Default)
2-3: VIA FILTER

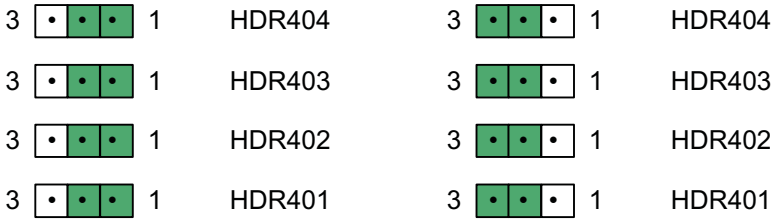
1-2: VIA FILTER
2-3: DIRECT INPUT (Default)

1.3.9 Input Terminate (HDR125-136)

Terminate unused input pins by connecting input pins with VrefS; default is open. Both Lch and Rch should be terminated to VrefS, if unused.

1.3.10 Microcontroller I/F Select (HDR401-404)

Select microcontroller I/F port; not required to change in general if printer port is used. Change if other I/F port is used in place of printer port.

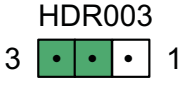


1-2: SPI control through CN401, printer port, default for PCM1850

2-3: Control through CN402, default for PCM1851
(CN402 and pullup resistors are not mounted on standard specification board.)

1.3.11 U001 Vdd Select (HDR003)

Select Vdd source for PCM1850/51; not required to change in general. Use this selection if Vdd source is provided through CN501.



1-2: Select external 3.3-V power supply source

2-3: Select on board 3.3-V regulator, U002. (Default)

1.3.12 U001 Reset Select (HDR002)

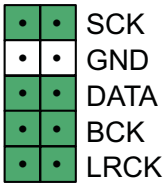
Select reset signal source for PCM1850/51; not required to change in general. Use this selection if reset control through printer port or external microcontroller port are used in place of onboard reset switch.

1-2: Reset signal from on board RESET SW. (Default)

2-3: Reset signal through printer port or external microcontroller port.

1.3.13 Digital Audio Interface (HDR001)

Not required to change in general; use for interface to external audio interface source.



1.3.14 CSS Select (HDR201)

Not required to change in general; use for AES-3 option control.

1-2: LO (Default)

2-3: HI

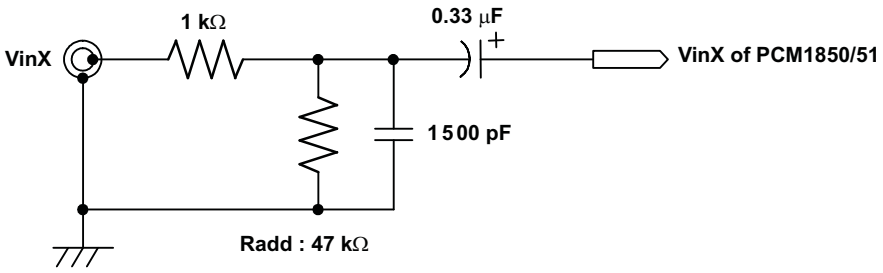
1.3.15 Input Impedance Table for Various PGA Setting With Termination

Table 4. Input Impedance Table

PGA		Radd (Added Resistor in Parallel)								Example of Input Level	
GAIN	Rin	47	56	68	82	100	120	150	180		
dB	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ		
–11.0	201	38.1	43.8	50.8	58.2	66.8	75.1	85.9	95.0		
–10.5	199	38.0	43.7	50.7	58.1	66.6	74.9	85.5	94.5		
–10.0	196	37.9	43.6	50.5	57.8	66.2	74.4	85.0	93.8		
–9.5	193	37.8	43.4	50.3	57.5	65.9	74.0	84.4	93.1		
–9.0	190	37.7	43.3	50.1	57.3	65.5	73.5	83.8	92.4		
–8.5	188	37.6	43.1	49.9	57.1	65.3	73.2	83.4	92.0		
–8.0	185	37.5	43.0	49.7	56.8	64.9	72.8	82.8	91.2		
–7.5	181	37.3	42.8	49.4	56.4	64.4	72.2	82.0	90.2		
–7.0	178	37.2	42.6	49.2	56.1	64.0	71.7	81.4	89.5		<= 2.4-V input
–6.5	175	37.0	42.4	49.0	55.8	63.6	71.2	80.8	88.7		(200 mV +21.5 dB)
–6.0	172	36.9	42.2	48.7	55.5	63.2	70.7	80.1	88.0		
–5.5	169	36.8	42.1	48.5	55.2	62.8	70.2	79.5	87.2		<= 2-V input
–5.0	165	36.6	41.8	48.2	54.8	62.3	69.5	78.6	86.1		(200 mV +20 dB)
–4.5	162	36.4	41.6	47.9	54.4	61.8	68.9	77.9	85.3		
–4.0	158	36.2	41.3	47.5	54.0	61.2	68.2	76.9	84.1		
–3.5	155	36.1	41.1	47.3	53.6	60.8	67.6	76.2	83.3		
–3.0	151	35.8	40.9	46.9	53.1	60.2	66.9	75.2	82.1		
–2.5	147	35.6	40.6	46.5	52.6	59.5	66.1	74.2	80.9		
–2.0	144	35.4	40.3	46.2	52.2	59.0	65.5	73.5	80.0		
–1.5	140	35.2	40.0	45.8	51.7	58.3	64.6	72.4	78.8		
–1.0	136	34.9	39.7	45.3	51.2	57.6	63.8	71.3	77.5		
–0.5	133	34.7	39.4	45.0	50.7	57.1	63.1	70.5	76.5	Final Input Impedance	
0.0	129	34.4	39.0	44.5	50.1	56.3	62.2	69.4	75.1		
0.5	125	34.2	38.7	44.0	49.5	55.6	61.2	68.2	73.8		<= 1-V input
1.0	122	33.9	38.4	43.7	49.0	55.0	60.5	67.3	72.7		(200 mV +14 dB)
1.5	118	33.6	38.0	43.1	48.4	54.1	59.5	66.0	71.3		
2.0	114	33.3	37.6	42.6	47.7	53.3	58.5	64.8	69.8		
2.5	111	33.0	37.2	42.2	47.2	52.6	57.7	63.8	68.7		<= 800-mV input
3.0	107	32.7	36.8	41.6	46.4	51.7	56.6	62.5	67.1		(200 mV +12 dB)
3.5	103	32.3	36.3	41.0	45.7	50.7	55.4	61.1	65.5		
4.0	100	32.0	35.9	40.5	45.1	50.0	54.5	60.0	64.3		
4.5	96	31.6	35.4	39.8	44.2	49.0	53.3	58.5	62.6		
5.0	93	31.2	35.0	39.3	43.6	48.2	52.4	57.4	61.3		<= 600-mV input
5.5	89	30.8	34.4	38.5	42.7	47.1	51.1	55.9	59.6		(200 mV +9.5 dB)
6.0	86	30.4	33.9	38.0	42.0	46.2	50.1	54.7	58.2		
6.5	83	30.0	33.4	37.4	41.2	45.4	49.1	53.4	56.8		
7.0	80	29.6	32.9	36.8	40.5	44.4	48.0	52.2	55.4		
7.5	77	29.2	32.4	36.1	39.7	43.5	46.9	50.9	53.9		
8.0	73	28.6	31.7	35.2	38.6	42.2	45.4	49.1	51.9		
8.5	70	28.1	31.1	34.5	37.8	41.2	44.2	47.7	50.4		
9.0	68	27.8	30.7	34.0	37.2	40.5	43.4	46.8	49.4		
9.5	65	27.3	30.1	33.2	36.3	39.4	42.2	45.3	47.8		
10.0	62	26.7	29.4	32.4	35.3	38.3	40.9	43.9	46.1		
10.5	59	26.2	28.7	31.6	34.3	37.1	39.6	42.3	44.4		
11.0	57	25.8	28.2	31.0	33.6	36.3	38.6	41.3	43.3		

- How to use Table 4:
  If 2-Vrms input at Rin = 47 kΩ is desired, select PGA=-5.5 dB and Radd = 68 kΩ.
  If 800-mVrms input at Rin = 47 kΩ is desired, select PGA = +2.5 dB and Radd = 82 kΩ.

The following illustration shows the default constant of an onboard low-pass filter circuit.

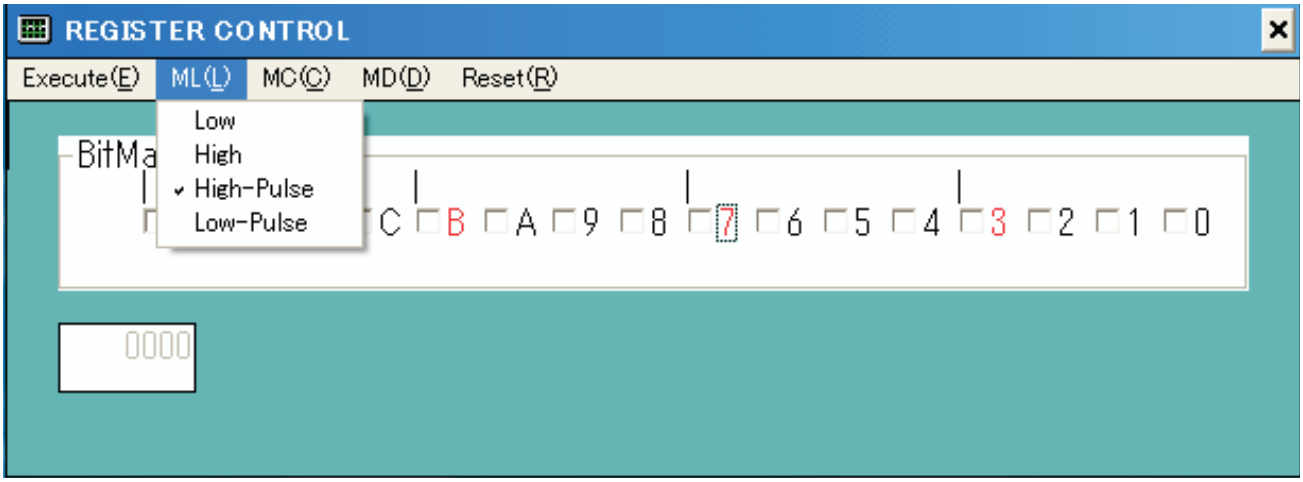


1.4 Operation Guide for REGTEST

The following description explains how to use REGTEST, the register control software for the DEM-DAI1850.

1.4.1 Initialization

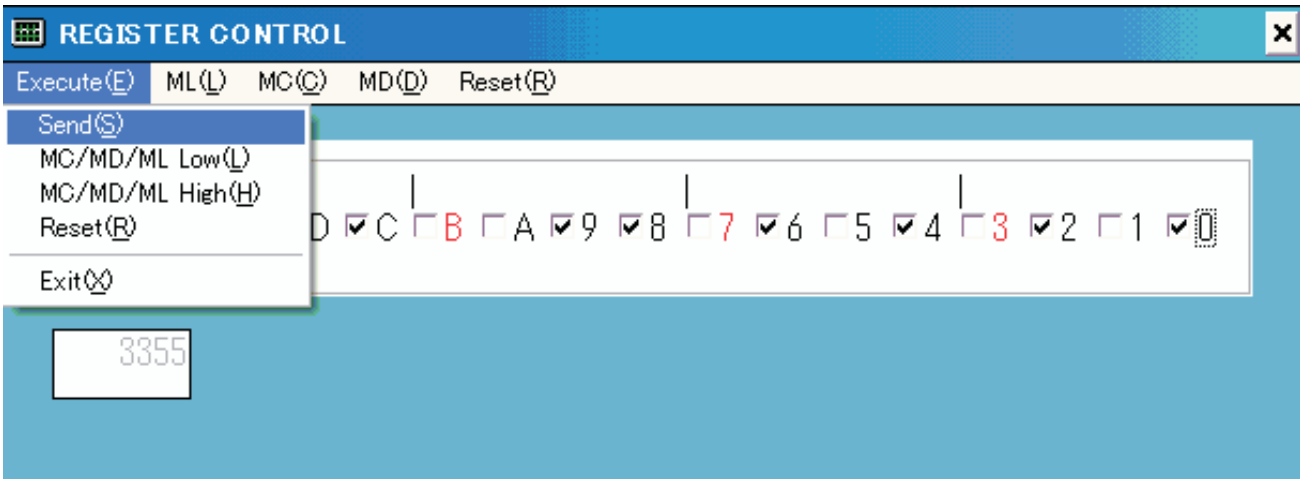
Click pulldown menu, *ML (L)*, and select *High-Pulse* for standard control.



1.4.2 Send Command

Click box which should be set to 1, so that address and data is set to desired value.

Click pulldown menu, *Execute (E)*, and select *Send (S)*, so that command which is already set up is sent through printer port.



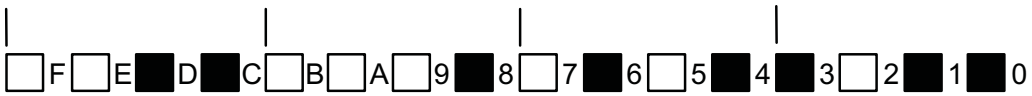
1.4.3 Interface and Operation Check

- Change PGA setting value (case for setting PGA = -5.5 dB)

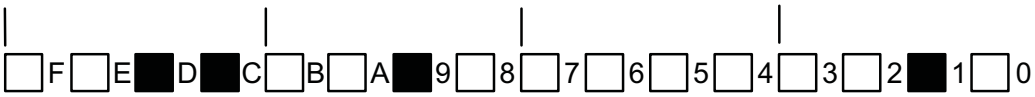
The input full scale can be changed to 2 Vrms from default, 2.4 Vrms by this command, and the signal level change of MOUTL/MOUTR can be confirmed as the right operation of DEM-DAI1850 and REG TEST. The RESET SW resets this setting to the default one again.

1.4.4 Example of Register Setting

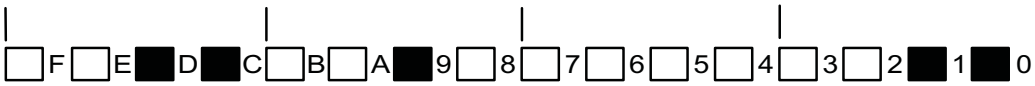
- Change PGA setting value (case for setting PGA = -2.5 dB).



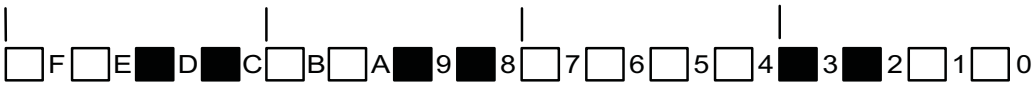
- Change input channel to CH2.



- Change input channel to CH3.



- Change from Slave mode to Master mode (256 fs) operation with RESET command (SRST = 0), need to change SW201 setting from *MASTER* to *SLAVE* after this command.



- Disable RESET command (SRST = 1) with Master mode (256 fs) operation

1.4.5 Summary of PCM1850/51 Register Definitions

Table 5. Bit Map Definition

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REG 31 H	0	0	1	1	0	0	0	1	RSV	MRST	PG5	PG4	PG3	PG2	PG1	PG0
REG 32 H	0	0	1	1	0	0	1	0	RSV	RSV	RSV	RSV	RSV	CH2	CH1	CH0
REG 33 H	0	0	1	1	0	0	1	1	BYP	SRST	RSV	MD1	MD0	FMT2	FMT1	FMT0

Table 6. Default Setting

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REG 31 H	0	0	1	1	0	0	0	1	0	1	0	0	1	0	1	0
REG 32 H	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1
REG 33 H	0	0	1	1	0	0	1	1	0	1	0	0	0	1	0	0

Table 7. PGA Gain Control

PGA	PG5	PG4	PG3	PG2	PG1	PG0
11 dB	1	1	0	1	1	0
10.5 dB	1	1	0	1	0	1
10 dB	1	1	0	1	0	0
9.5 dB	1	1	0	0	1	1
9 dB	1	1	0	0	1	0
8.5 db	1	1	0	0	0	1
8 dB	1	1	0	0	0	0
7.5 dB	1	0	1	1	1	1
7 dB	1	0	1	1	1	0
6.5 dB	1	0	1	1	0	1
6 dB	1	0	1	1	0	0
5.5dB	1	0	1	0	1	1
5 dB	1	0	1	0	1	0
4.5 dB	1	0	1	0	0	1
4 dB	1	0	1	0	0	0
3.5 dB	1	0	0	1	1	1
3 dB	1	0	0	1	1	0
2.5 dB	1	0	0	1	0	1
2 dB	1	0	0	1	0	0
1.5 dB	1	0	0	0	1	1
1 dB	1	0	0	0	1	0
0.5 dB	1	0	0	0	0	1
0 dB	1	0	0	0	0	0
-0.5dB	0	1	1	1	1	1
-1 dB	0	1	1	1	1	0
-1.5 dB	0	1	1	1	0	1
-2 dB	0	1	1	1	0	0
-2.5 dB	0	1	1	0	1	1
-3 dB	0	1	1	0	1	0
-3.5 dB	0	1	1	0	0	1
-4 dB	0	1	1	0	0	0
-4.5 dB	0	1	0	1	1	1

Table 7. PGA Gain Control (continued)

PGA	PG5	PG4	PG3	PG2	PG1	PG0
-5 dB	0	1	0	1	1	0
-5.5 dB	0	1	0	1	0	1
-6 dB	0	1	0	1	0	0
-6.5 dB	0	1	0	0	1	1
-7 dB	0	1	0	0	1	0
-7.5 dB	0	1	0	0	0	1
-8 dB	0	1	0	0	0	0
-8.5 dB	0	0	1	1	1	1
-9 dB	0	0	1	1	1	0
-9.5 dB	0	0	1	1	0	1
-10 dB	0	0	1	1	0	0
-10.5 dB	0	0	1	0	1	1
-11 dB	0	0	1	0	1	0

: Default setting

Table 8. Mode Register Reset Control

MRST	Operation
1	Normal
0	Mode register reset

: Default Setting

Table 9. MUX Input Channel Selection

CH2	CH1	CH0	Input Channel
1	1	1	Mute
1	1	0	Channel 6
1	0	1	Channel 5
1	0	0	Channel 4
0	1	1	Channel 3
0	1	0	Channel 2
0	0	1	Channel 1
0	0	0	Mute

: Default Setting

Table 10. Audio Interface Format Selection

FMT2	FMT1	FMT0	Format
1	1	1	RSV
1	1	0	RSV
1	0	1	24-bit left-justified
1	0	0	24-bit I^2S
0	1	1	16-bit right-justified
0	1	0	RSV
0	0	1	RSV
0	0	0	24-bit right-justified

: Default Setting

Table 11. Audio Interface Mode Selection

MD1	MD0	Mode
1	1	Master, 512 fs
1	0	Master, 384 fs
0	1	Master, 256 fs
0	0	Slave

: Default Setting

Table 12. System Reset Control

SRST	Operation
1	Normal
0	Resynchronization

: Default Setting

Table 13. HPF Bypass Control

BYP	HPF Function
1	Bypass (Disable)
0	Through (Enable)

: Default Setting

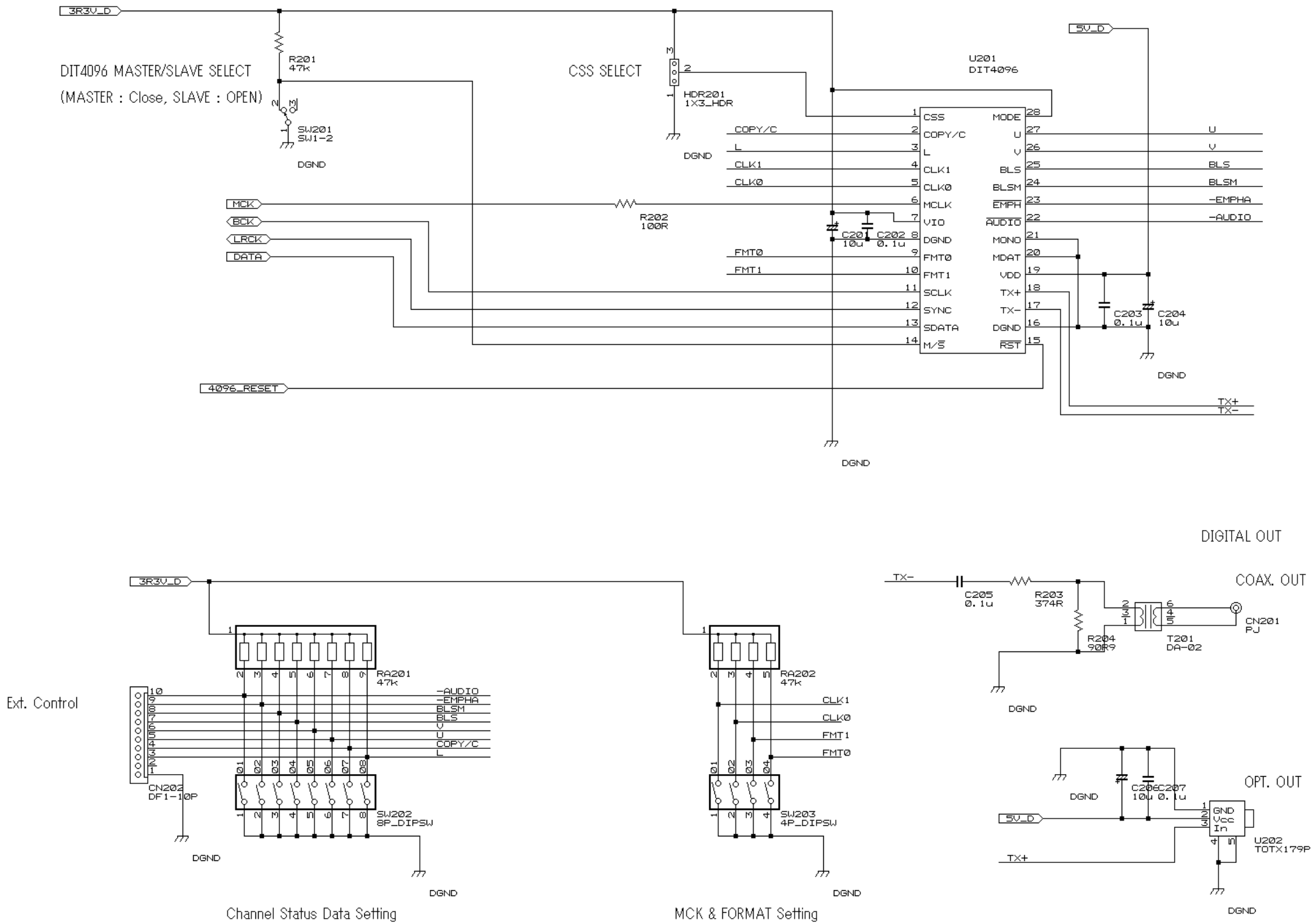
2 Schematics, Bill of Materials, and Printed-Circuit Boards

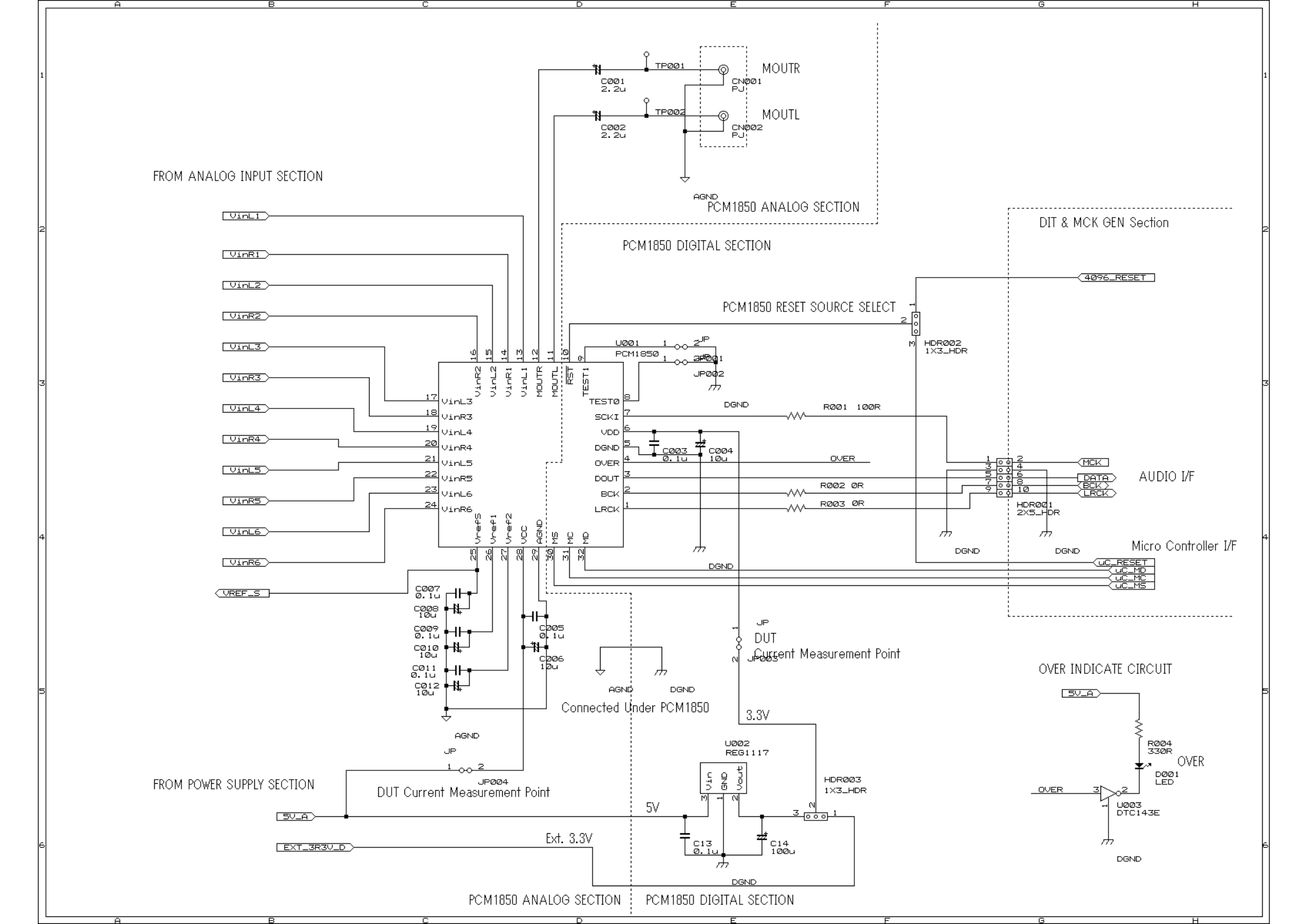
This section presents the DEM-DAI1850/51 schematics, bill of materials, and printed-circuit board layouts.

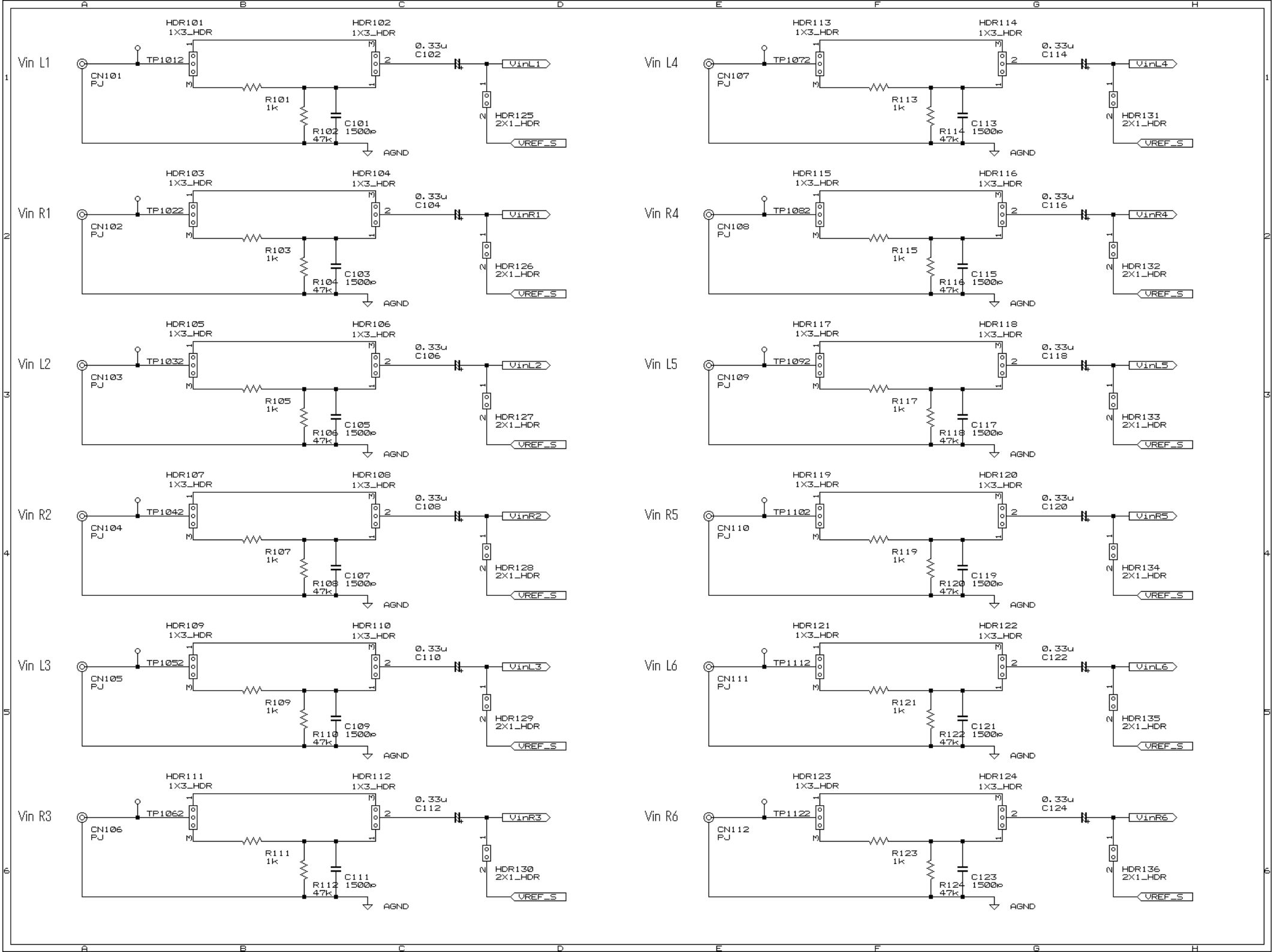
2.1 DEM-DAI1850/51 Schematic

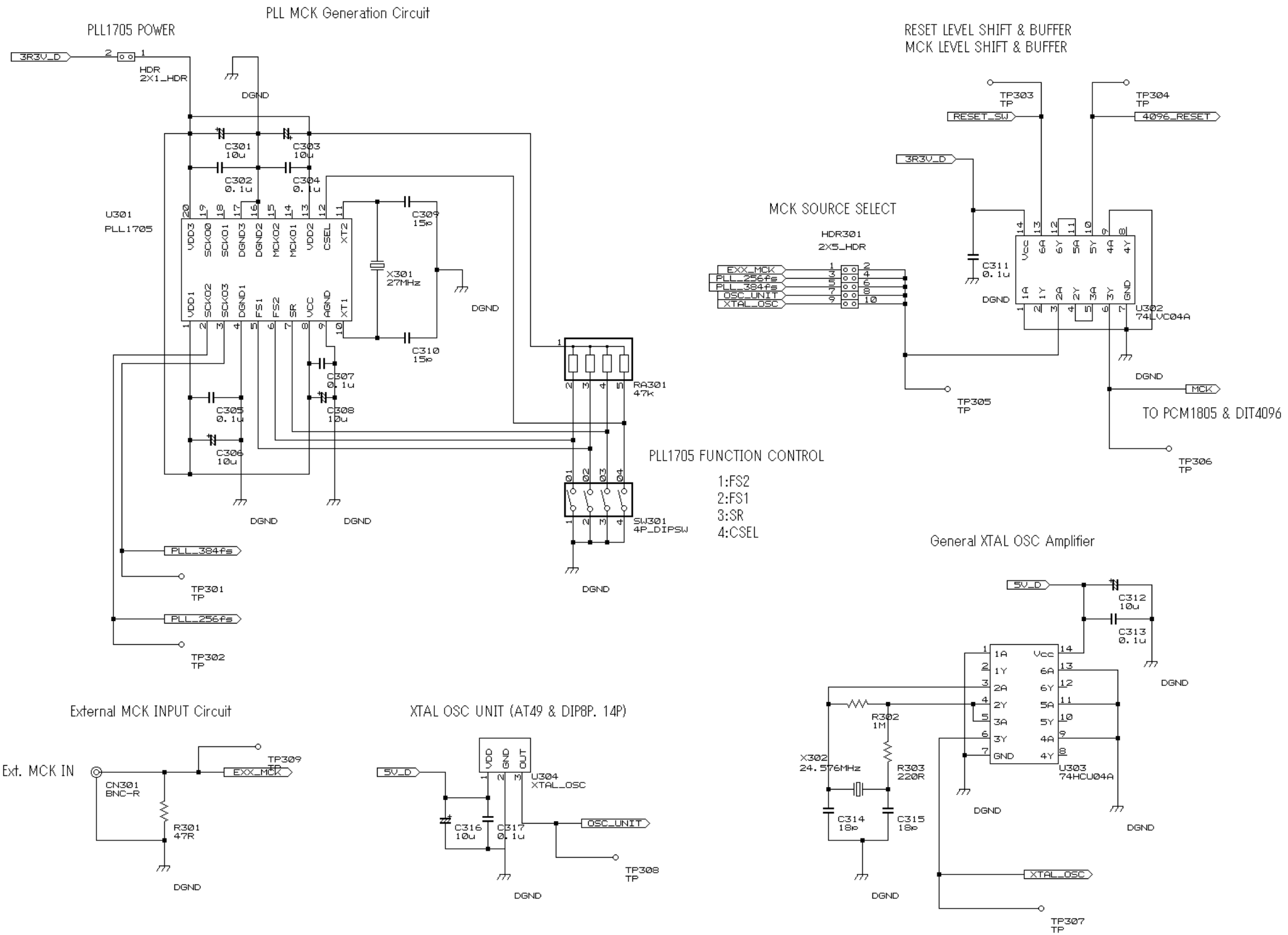
The DEM-DAI1850/51 schematic is affixed to this page and appears in the following sequence:

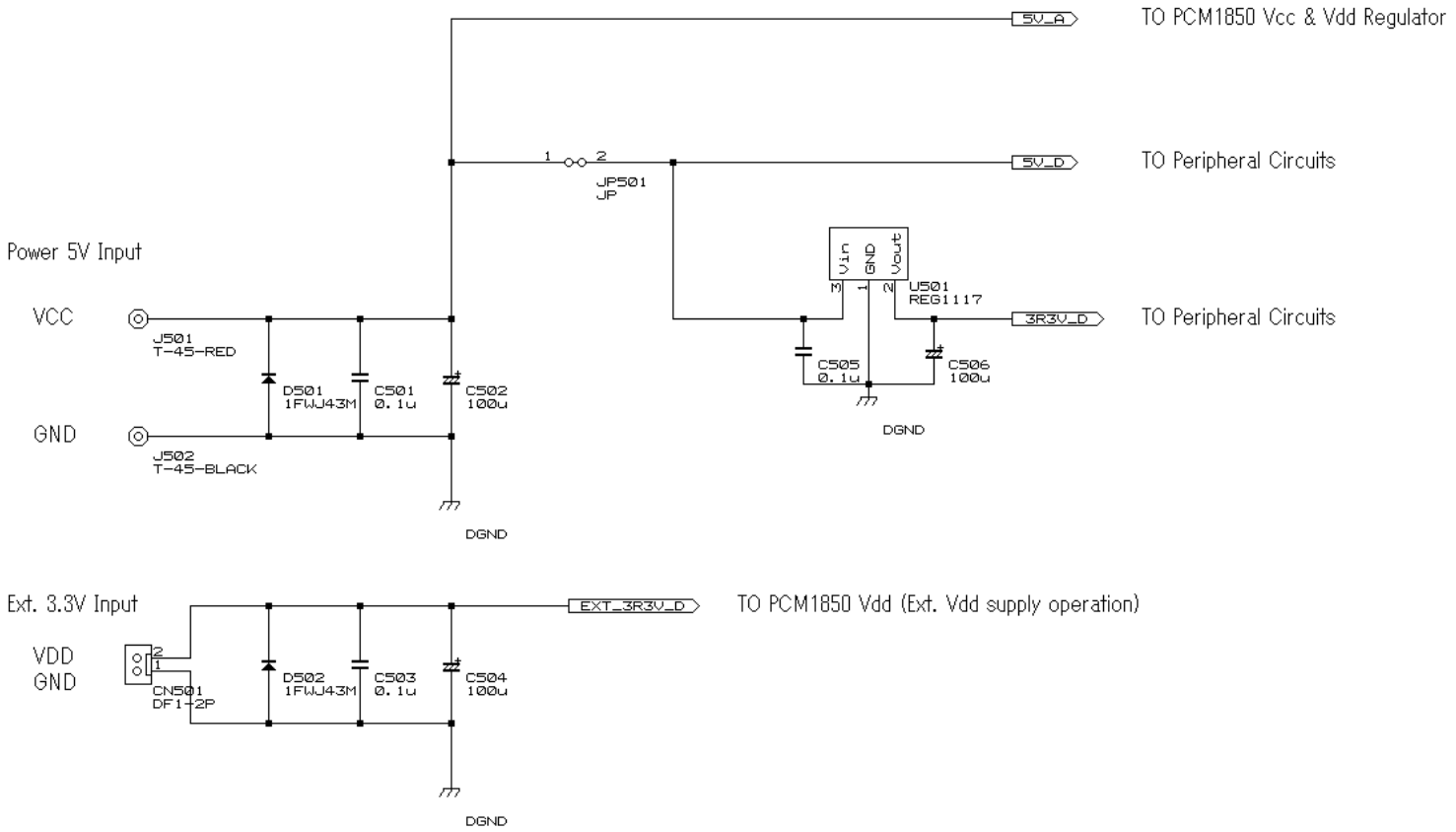
- Digital Interface Transmitter Section
- ADC PCM1850/51 Section
- Analog Input Section
- Clock Generator Section
- Power Supply Section
- Serial Control Port Section

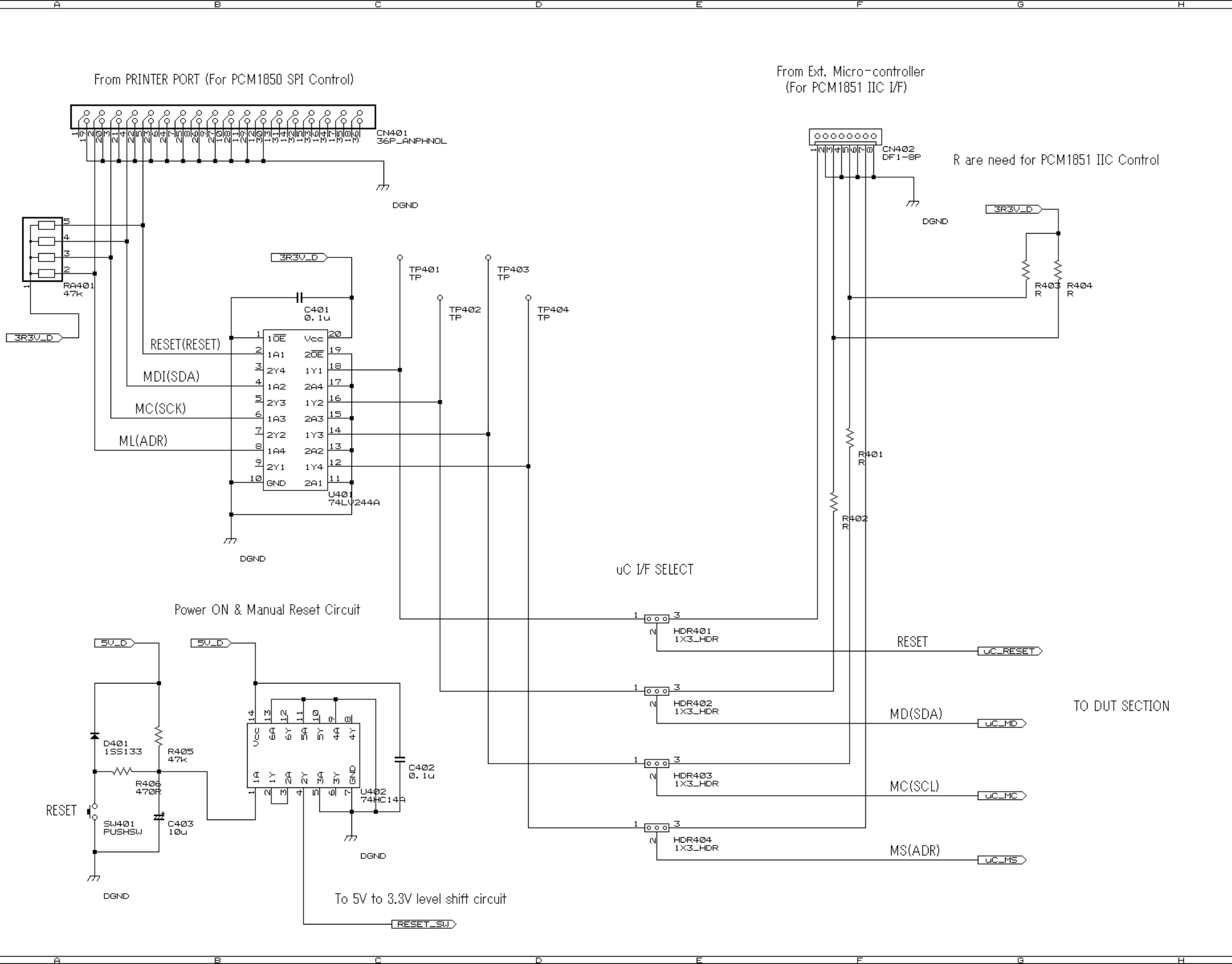

3R3V_D
DIT4096 MASTER/SLAVE SELECT
(MASTER : Close, SLAVE : OPEN)
R201
47k
SW201
SW1-2
DGND
CSS SELECT
HDR201
1X3_HDR
DGND
U201
DIT4096
5V_D
CSS
COPY/C
L
CLK1
CLK0
MCLK
VIO
DGND
FMT0
FMT1
SCLK
SYNC
SDATA
M/S
MODE
U
V
BLS
BLSM
EMPH
AUDIO
MONO
MDAT
VDD
TX+
TX-
DGND
RST
MCK
BCK
LRCK
DATA
R202
100R
C201
10u
C202
0.1u
C203
0.1u
C204
10u
DGND
4096_RESET
TX+
TX-
DIGITAL OUT
COAX. OUT
TX-
C205
0.1u
R203
374R
R204
90R9
T201
DA-02
CN201
PJ
DGND
OPT. OUT
C206
10u
C207
0.1u
DGND
5V_D
TX+
GND
Vcc
In
U202
TOTX179P
DGND
Ext. Control
3R3V_D
RA201
47k
-AUDIO
-EMPHA
BLSM
BLS
V
U
COPY/C
L
CN202
DF1-10P
SW202
8P_DIPSW
DGND
Channel Status Data Setting
RA202
47k
CLK1
CLK0
FMT1
FMT0
SW203
4P_DIPSW
DGND
MCK & FORMAT Setting


FROM ANALOG INPUT SECTION
TP001
MOUTR
C001
2.2u
CN001
PJ
TP002
MOUTL
C002
2.2u
CN002
PJ
AGND
PCM1850 ANALOG SECTION
PCM1850 DIGITAL SECTION
DIT & MCK GEN Section
4096_RESET
PCM1850 RESET SOURCE SELECT
HDR002
1X3_HDR
U001
PCM1850
JP
JP001
JP002
VinL1
VinR1
VinL2
VinR2
VinL3
VinR3
VinL4
VinR4
VinL5
VinR5
VinL6
VinR6
VREF_S
DGND
R001 100R
C003
0.1u
C004
10u
OVER
R002 0R
R003 0R
MCK
DATA
BCK
LRCK
AUDIO I/F
HDR001
2X5_HDR
Micro Controller I/F
uC_RESET
uC_MD
uC_MC
uC_MS
C007
0.1u
C008
10u
C009
0.1u
C010
10u
C011
0.1u
C012
10u
C005
0.1u
C006
10u
AGND
Connected Under PCM1850
JP
DUT
Current Measurement Point
JP003
OVER INDICATE CIRCUIT
5V_A
R004
330R
OVER
D001
LED
U003
DTC143E
JP
JP004
DUT Current Measurement Point
FROM POWER SUPPLY SECTION
U002
REG1117
Vin
GND
Vout
HDR003
1X3_HDR
3.3V
5V
5V_A
EXT_3R3V_D
Ext. 3.3V
C13
0.1u
C14
100u
PCM1850 ANALOG SECTION
PCM1850 DIGITAL SECTION


Vin L1
HDR101 1X3_HDR
HDR102 1X3_HDR
TP1012
CN101 PJ
0.33u C102
VinL1
R101 1k
R102 47k
C101 1500p
HDR125 2X1_HDR
VREF_S
AGND
Vin R1
HDR103 1X3_HDR
HDR104 1X3_HDR
TP1022
CN102 PJ
0.33u C104
VinR1
R103 1k
R104 47k
C103 1500p
HDR126 2X1_HDR
VREF_S
AGND
Vin L2
HDR105 1X3_HDR
HDR106 1X3_HDR
TP1032
CN103 PJ
0.33u C106
VinL2
R105 1k
R106 47k
C105 1500p
HDR127 2X1_HDR
VREF_S
AGND
Vin R2
HDR107 1X3_HDR
HDR108 1X3_HDR
TP1042
CN104 PJ
0.33u C108
VinR2
R107 1k
R108 47k
C107 1500p
HDR128 2X1_HDR
VREF_S
AGND
Vin L3
HDR109 1X3_HDR
HDR110 1X3_HDR
TP1052
CN105 PJ
0.33u C110
VinL3
R109 1k
R110 47k
C109 1500p
HDR129 2X1_HDR
VREF_S
AGND
Vin R3
HDR111 1X3_HDR
HDR112 1X3_HDR
TP1062
CN106 PJ
0.33u C112
VinR3
R111 1k
R112 47k
C111 1500p
HDR130 2X1_HDR
VREF_S
AGND
Vin L4
HDR113 1X3_HDR
HDR114 1X3_HDR
TP1072
CN107 PJ
0.33u C114
VinL4
R113 1k
R114 47k
C113 1500p
HDR131 2X1_HDR
VREF_S
AGND
Vin R4
HDR115 1X3_HDR
HDR116 1X3_HDR
TP1082
CN108 PJ
0.33u C116
VinR4
R115 1k
R116 47k
C115 1500p
HDR132 2X1_HDR
VREF_S
AGND
Vin L5
HDR117 1X3_HDR
HDR118 1X3_HDR
TP1092
CN109 PJ
0.33u C118
VinL5
R117 1k
R118 47k
C117 1500p
HDR133 2X1_HDR
VREF_S
AGND
Vin R5
HDR119 1X3_HDR
HDR120 1X3_HDR
TP1102
CN110 PJ
0.33u C120
VinR5
R119 1k
R120 47k
C119 1500p
HDR134 2X1_HDR
VREF_S
AGND
Vin L6
HDR121 1X3_HDR
HDR122 1X3_HDR
TP1112
CN111 PJ
0.33u C122
VinL6
R121 1k
R122 47k
C121 1500p
HDR135 2X1_HDR
VREF_S
AGND
Vin R6
HDR123 1X3_HDR
HDR124 1X3_HDR
TP1122
CN112 PJ
0.33u C124
VinR6
R123 1k
R124 47k
C123 1500p
HDR136 2X1_HDR
VREF_S
AGND


PLL MCK Generation Circuit
PLL1705 POWER
3R3V_D
HDR
2X1_HDR
DGND
C301
10u
C303
10u
C302
0.1u
C304
0.1u
U301
PLL1705
VDD3
SCKO0
SCKO1
DGND3
DGND2
MCKO2
MCKO1
VDD2
CSEL
XT2
VDD1
SCKO2
SCKO3
DGND1
FS1
FS2
SR
VCC
AGND
XT1
C309
15p
X301
27MHz
C310
15p
C307
0.1u
C305
0.1u
C308
10u
C306
10u
RA301
47k
PLL_384fs
TP301
TP
PLL_256fs
TP302
TP
SW301
4P_DIPSW
PLL1705 FUNCTION CONTROL
1:FS2
2:FS1
3:SR
4:CSEL
RESET LEVEL SHIFT & BUFFER
MCK LEVEL SHIFT & BUFFER
TP303
TP
RESET_SW
TP304
TP
4096_RESET
3R3V_D
C311
0.1u
U302
74LVC04A
MCK SOURCE SELECT
HDR301
2X5_HDR
EXX_MCK
PLL_256fs
PLL_384fs
OSC_UNIT
XTAL_OSC
TP305
TP
MCK
TO PCM1805 & DIT4096
TP306
TP
External MCK INPUT Circuit
Ext. MCK IN
CN301
BNC-R
TP309
TP
EXX_MCK
R301
47R
XTAL OSC UNIT (AT49 & DIP8P. 14P)
5V_D
U304
XTAL_OSC
C316
10u
C317
0.1u
OSC_UNIT
TP308
TP
General XTAL OSC Amplifier
5V_D
C312
10u
C313
0.1u
R302
1M
X302
24.576MHz
R303
220R
C314
18p
C315
18p
U303
74HCU04A
XTAL_OSC
TP307
TP


5V_A
TO PCM1850 Vcc & Vdd Regulator
5V_D
TO Peripheral Circuits
JP501
JP
Power 5V Input
VCC
J501
T-45-RED
D501
1FWJ43M
C501
0.1u
C502
100u
GND
J502
T-45-BLACK
DGND
Vin
GND
Vout
U501
REG1117
3R3V_D
TO Peripheral Circuits
C505
0.1u
C506
100u
DGND
Ext. 3.3V Input
EXT_3R3V_D
TO PCM1850 Vdd (Ext. Vdd supply operation)
VDD
GND
CN501
DF1-2P
D502
1FWJ43M
C503
0.1u
C504
100u
DGND


From PRINTER PORT (For PCM1850 SPI Control)
CN401
36P_ANPHNOL
DGND
RA401
47k
3R3V_D
C401
0.1u
TP401
TP
TP402
TP
TP403
TP
TP404
TP
RESET(RESET)
MDI(SDA)
MC(SCK)
ML(ADR)
U401
74LV244A
From Ext. Micro-controller
(For PCM1851 IIC I/F)
CN402
DF1-8P
R are need for PCM1851 IIC Control
R403
R
R404
R
R401
R
R402
R
uC I/F SELECT
HDR401
1X3_HDR
HDR402
1X3_HDR
HDR403
1X3_HDR
HDR404
1X3_HDR
RESET
MD(SDA)
MC(SCL)
MS(ADR)
uC_RESET
uC_MD
uC_MC
uC_MS
TO DUT SECTION
Power ON & Manual Reset Circuit
5V_D
D401
1SS133
R405
47k
R406
470R
SW401
PUSHSW
C403
10u
U402
74HC14A
C402
0.1u
To 5V to 3.3V level shift circuit
RESET_SW

2.2 DEM-DAI1850/51 Bill of Materials

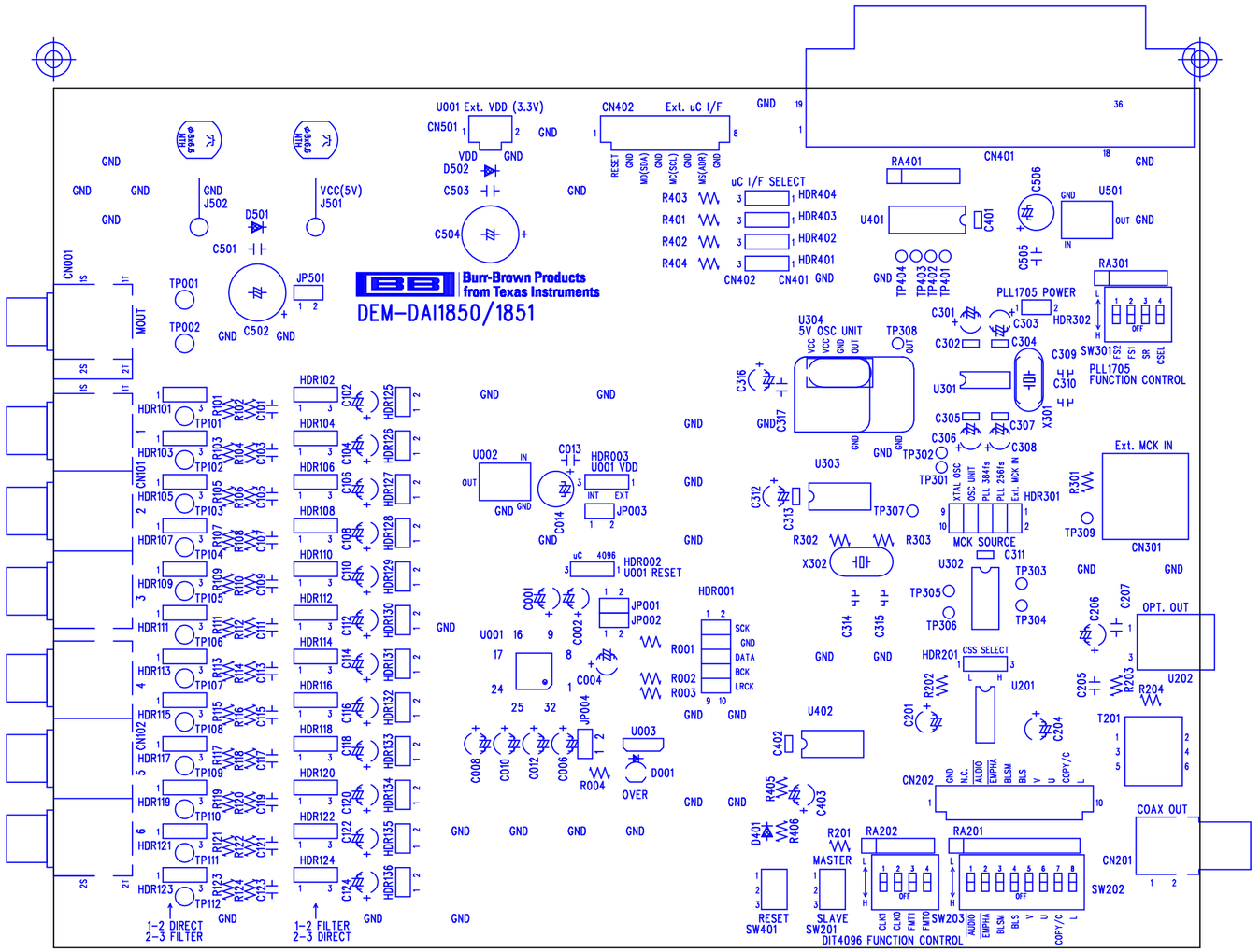
Ref Des	Qty	Description	Specification	MFR. Part No.	MFR.
C309, C310	2	Ceramic Capacitor	15 pF, NP0		Murata
C314, C315	2	Ceramic Capacitor	18 pF, NP0		Murata, With PX-1
C013, C207, C317, C501, C503, C505	6	Ceramic Capacitor	0.1 µF		Murata
C003, C005, C007, C009, C011, C202, C203, C302, C304, C305, C307, C311, C313, C401, C402	15	Ceramic Capacitor	0.1 µF, Chip 1608		Murata
C101, C103, C105, C107, C109, C111, C113, C115, C117, C119, C121, C123	12	Film Capacitor	1500 pF	APSF0100J152	Nissei
C205	1	Film Capacitor	0.1 µF	AMFF0050J104	Nissei
C102, C104, C106, C108, C110, C112, C114, C116, C118, C120, C122, C124	12	Electrolytic Capacitor	0.33 µF	R3A-50V0R033M	ELNA
C001, C002	2	Electrolytic Capacitor	2.2 µF	R3A-50V022M	ELNA
C004, C006, C008, C010, C012, C201, C204, C206, C301, C303, C306, C308, C312, C316, C403	15	Electrolytic Capacitor	10 µF	R3A-16V100M	ELNA
C014, C506	2	Electrolytic Capacitor	100 µF	R3A-6.3V101M	ELNA
C502, C504	2	Electrolytic Capacitor	100 µF	ROA-16V101M	ELNA
R301	1	Metal Film Resistor	1/8W, 47Ω, F		KOA, With PX-1
R204	1	Metal Film Resistor	1/8W, 90.9Ω, F		KOA
R303	1	Metal Film Resistor	1/8W, 220Ω, F		KOA, With PX-1
R203	1	Metal Film Resistor	1/8W, 374Ω, F		KOA
R302	1	Metal Film Resistor	1/8W, 1MΩ, F		KOA, With PX-1
R101, R103, R105, R107, R109, R111, R113, R115, R117, R119, R121, R123	12	Metal Film Resistor	1/8W, 1 kΩ		KOA
R102, R104, R106, R108, R110, R112, R114, R116, R118, R120, R122, R124	12	Metal Film Resistor	1/8W, 47 kΩ		KOA
R001, R002, R003, R202	4	Carbon Film Resistor	1/8W, 100Ω, J		
R004	1	Carbon Film Resistor	1/8W, 330Ω, J		
R406	1	Carbon Film Resistor	1/8W, 470Ω J		
R201, R405	2	Carbon Film Resistor	1/8W, 47kΩ, J		
R401–R404	4	Carbon Film Resistor	1/8W, xxΩ, J		With PX-1, I^2C Termination
RA202, R301, R401	3	Resistor Array	4x47 kΩ, J		
RA201	1	Resistor Array	8x47 kΩ, J		
D401	1	Diode		1SS133	Rohm
D501, D502	2	SB Diode	Schottky Barrier	1FWJ43M	Toshiba
LED001	1	LED Red	Red, 3mm	TLR124	Toshiba
U003	1	Digital Transistor	4.7k/4.7k	DTC143ES	Rohm
U001	1	DUT (ADC)		PCM1850/51	TI/BB
U002, U501	2	3.3V Regulator IC		REG1117-3.3	TI/BB
U201	1	Digital I/F Transmitter		DIT4096	TI/BB

Ref Des	Qty	Description	Specification	MFR. Part No.	MFR.
U301	1	PLL Clock Generator		PLL1705	TI/BB
U302	1	Logic IC		SN74LVC04ANS	TI
U303	1	Logic IC		SN74HCU04ANS	TI
U401	1	Logic IC		SN74LV244ANS	TI
U402	1	Logic IC		SN74HC14ANS	TI
U202	1	Optical Transmitter		TOTX179P	Toshiba
U304	1	Crystal Oscillator Unit	12.288 MHz, 50ppm	(DIP-14P/8P)	With PX-1
X301	1	Crystal Resonator	27.000 MHz	HC-49/U-S, KSS-STD	Kinseki
X302	1	Crystal Resonator	24.576 MHz	HC-49/U-S, KSS-STD	Kinseki, With PX-1
T201	1	Pulse Transformer		DA-02	JPC
SW203, SW301	2	DIP Switch	4 Poles	DSS104	Fujisoku
SW202	1	DIP Switch	8 Poles	DSS108	Fujisoku
SW201	1	Toggle Switch	3 Poles	FT1D-2M	Fujisoku
SW401	1	Push Switch		FP1F-2M	Fujisoku
HDR002, HDR101-HDR124, HDR201, HDR401-HDR404	34	Pin Header		FFC-3AMEP1	Honda
HDR125-HDR136, HDR302	13	Pin Header		FFC-2BMEP1	Honda
JP001-JP004, JP501	5	Pin Header		FFC-2BMEP1	Honda, Not mounted
HDR001, HDR301	2	Pin Header		FFC-10BMEP1	Honda
J501	1	Terminal (Red)	Red	T-45	Sato
J502	1	Terminal (Black)	Black	T-45	Sato
CN201	1	Pin Jack	Yellow	LPR6520-0804	SMK
CN001, CN002	1	Pin Jack 2P	2P	YKC21-3217	JALCO
CN101-CN112	2	Pin Jack 6P	6P	YKC21-3648	JALCO
CN501	1	DF1-2P Connector	2P	DF1-2P-2.5DSA	Hirose
CN402	1	DF1-8P Connector	8P	DF1-8P-2.5DSA	Hirose
CN202	1	DF1-10P Connector	10P	DF1-10P-2.5DSA	Hirose
CN301	1	BNC Receptacle		BNC-R-PC4	DDK
CN401	1	Amphenol Connector	36P	57LE-40360-7700 (D3)	DDK
TP001, TP002, TP101-TP112	14	Test Terminal		LC-2G (Red/White)	MAC8
TP301-TP309, TP401-TP404	13	Test Terminal		LC-4G	MAC8
		Short Plug		DIC-130	Honda
		Socket Pin		PX-1	MAC8

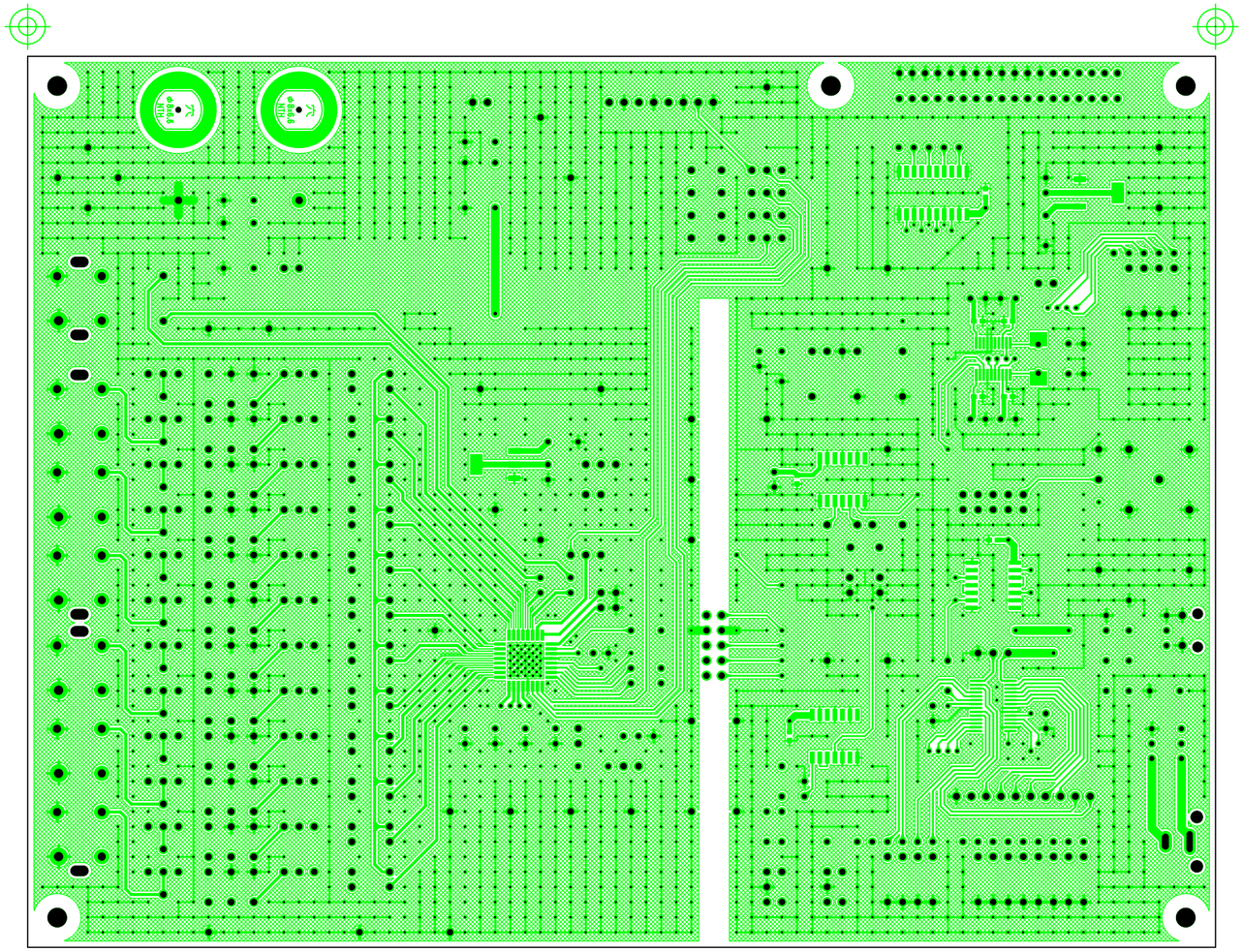
2.3 DEM-DAI1850/51 Printed-Circuit Board

The layers of the DEM-DAI1850/51 printed-circuit board are affixed to this page and presented in the following order:

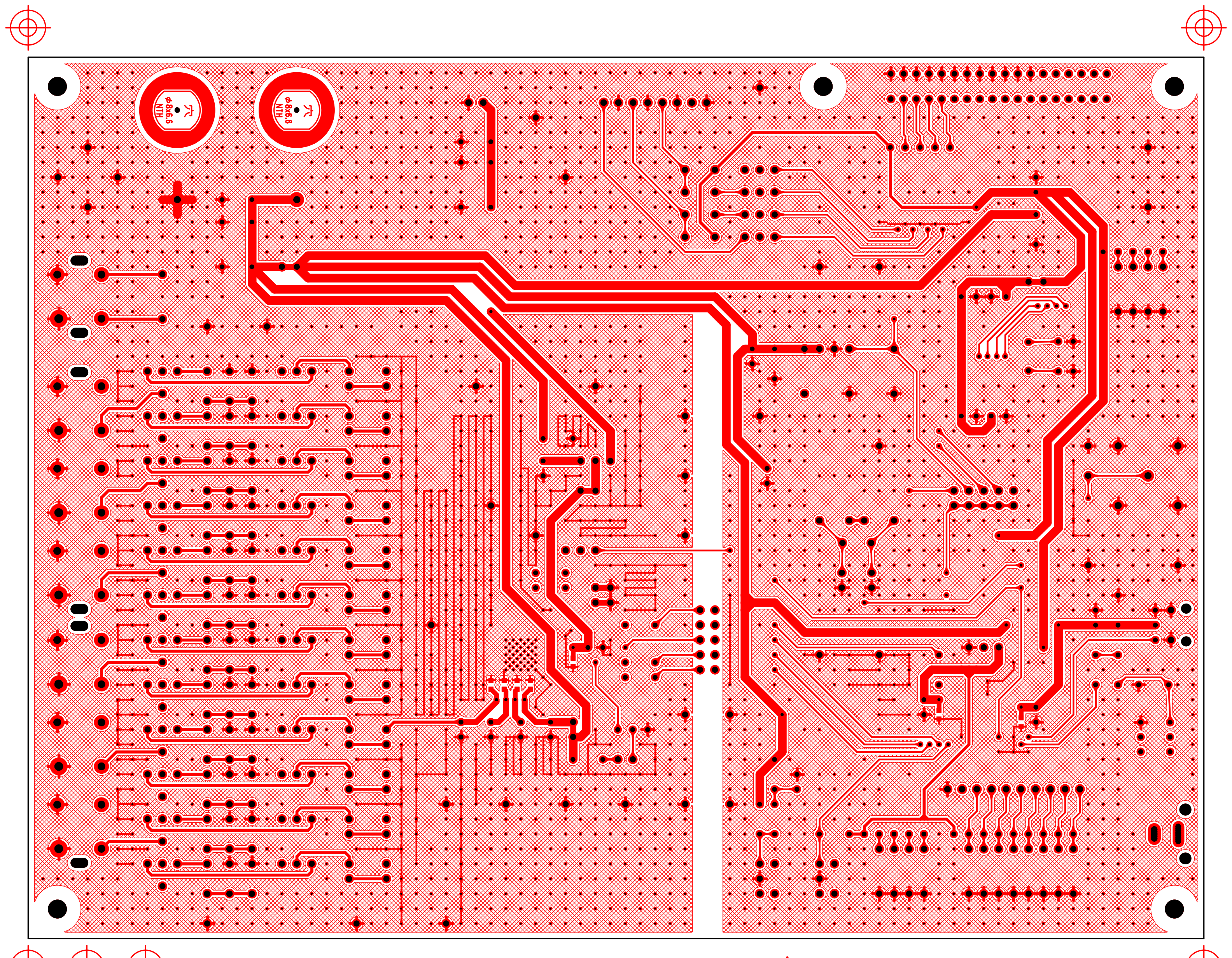
- Silk Screen
- Top View
- Bottom View
- Physical Dimension View



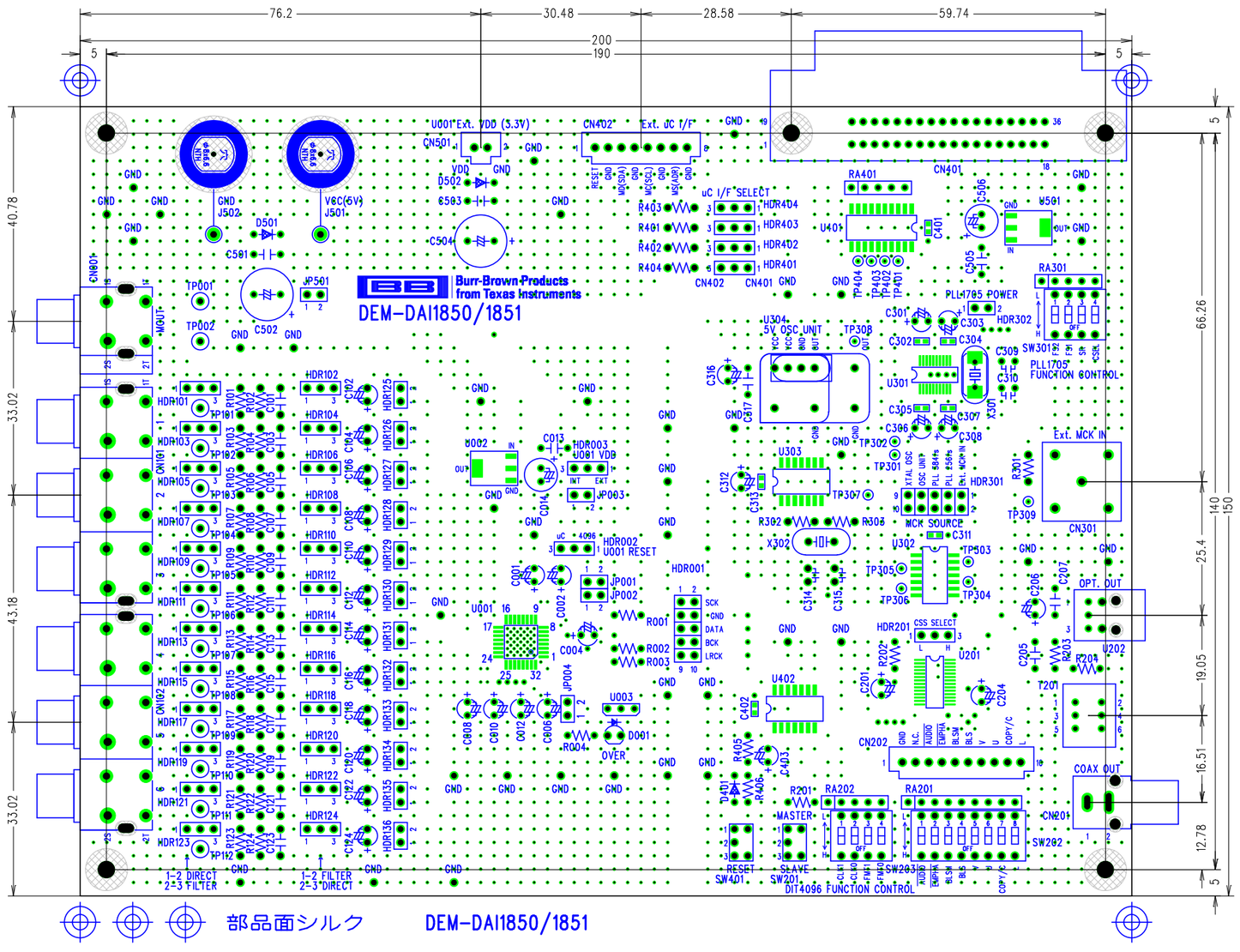
部品面シルク　　DEM-DAI1850/1851



部品面（第1層）　DEM-DAI1850/1851



半田面（第2層） DEM-DA1850/1851


76.2
30.48
28.58
59.74
200
190
5
5
40.78
33.02
43.18
33.02
66.26
5
140
150
25.4
19.05
16.51
12.78
5
Burr-Brown Products
from Texas Instruments
DEM-DAI1850/1851
U001 Ext. VDD (3.3V)
CN402 Ext. I/C I/F
CN501
J502
J501
D501
C501
C502
JP501
TP001
TP002
CN801
CN101
CN102
HDR101
HDR102
HDR103
HDR104
HDR105
HDR106
HDR107
HDR108
HDR109
HDR110
HDR111
HDR112
HDR113
HDR114
HDR115
HDR116
HDR117
HDR118
HDR119
HDR120
HDR121
HDR122
HDR123
HDR124
HDR125
HDR126
HDR127
HDR128
HDR129
HDR130
HDR131
HDR132
HDR133
HDR134
HDR135
HDR136
1-2 DIRECT
2-3 FILTER
1-2 FILTER
2-3 DIRECT
C013
HDR003
U001 VDD
JP003
C014
C001
C002
C004
JP001
JP002
JP004
HDR002
U001 RESET
HDR001
R001
R002
R003
R004
U001
U003
D001
OVER
C003
C006
C008
C010
C012
SCK
DATA
BCK
LRCK
uC I/F SELECT
HDR4D4
HDR4D3
HDR4D2
HDR401
R401
R402
R403
R404
RA401
CN401
U401
C401
C505
C506
U501
RA301
PLL1705 POWER
HDR302
C301
C302
C303
C304
C305
C306
C307
C308
C309
C310
SW301
PLL1705
FUNCTION CONTROL
U304
5V OSC UNIT
TP303
C316
C317
U301
X301
U303
C312
C313
TP307
TP301
TP302
HDR301
R301
TP309
Ext. MCK IN
CN301
MCK SOURCE
X302
U302
C311
TP503
TP305
TP306
TP304
C314
C315
C206
C207
OPT. OUT
U202
R203
R204
C205
HDR201
CSS SELECT
U201
R202
C201
C204
T201
COAX OUT
CN202
C402
C403
R405
R406
D401
U402
R201
RA202
RA201
CN201
MASTER
SLAVE
RESET
SW401
SW201
SW202
SW203
DIT4096 FUNCTION CONTROL
TP404
TP403
TP402
TP401
C116
C117
GND
VDD
VCC(5V)
部品面シルク
DEM-DAI1850/1851

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -4 V to 4 V and the output voltage range of -3 V to 3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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