

Timer Event Control (TEC)

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*.
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Timer Event Control (TEC) module is the interface between Timer modules and the external events. This chapter describes the TEC Module.

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1.1 Timer Event Control Introduction

TEC is a module that connects different Timer modules to each other and routes the external signals to the Timer modules. TEC contains the control registers to configure the routing between the Timer modules, and it also has the enable register bits and the interrupt enable and interrupt flags for external event inputs.

TEC features include:

- Enabling of internal and external clear signals
- Routing of internal signals (between Timer_D instances) and external clear signals
- Support of external fault input signals
- Interrupt vector generation of external fault and clear signals.
- Generating feedback signals to the Timer capture/compare channels to affect the timer outputs

The block diagram of TEC is shown in [Figure 1-1](#).

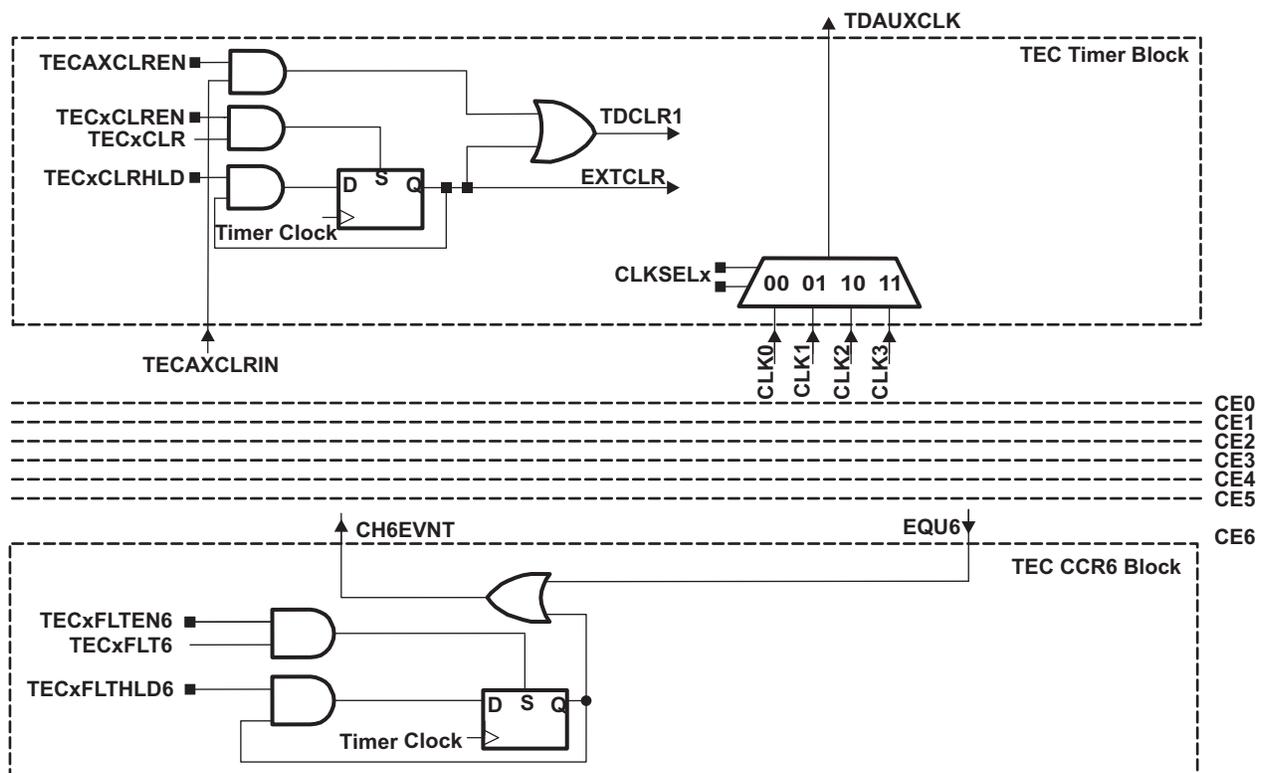


Figure 1-1. Timer Event Control Block Diagram

1.2 TEC Operation

The TEC module contains three sub-blocks:

- AUXCLK Selection sub-block
The AUXCLK Selection sub-block chooses the auxiliary clock source for the timer.
- External Clear sub-block
The External Clear sub-block controls the operation of the timer counter.
- Channel Event sub-block
The Channel Event sub-block controls the operation of a capture/compare channel.

This structure means that one Timer_D3 module, for example, needs a TEC that contains one AUXCLK Selection sub-block, one External Clear sub-block, and three Channel Event sub-blocks.

1.2.1 AUXCLK Selection Sub-Block

The AUXCLK Selection sub-block provides the auxiliary clock to Timer_D. By configuring the CLKSELx bits, one of the four clock sources can be chosen.

1.2.2 External Clear Sub-Block

The External Clear sub-block accepts external signals that can clear the Timer_D and affect the timer output. The TDR register in Timer_D module can be cleared by the following external events:

- External input TECECLR is enabled and is high.
- The auxiliary clear signal TECAXCLRIN is enabled and is high.

1.2.3 Channel Event Sub-Block

The Channel Event sub-block is responsible for timer event control and signaling. One Channel Event sub-block corresponds to one capture/compare channel in Timer_D module. The output unit of a capture/compare channel accepts the external fault input as well as the EQUx signal coming from the CCRx unit of the Timer_D. Both events will affect the PWM output.

When a TECXFLTx event is enabled and occurs, the corresponding status bit TECXFLTxSTA in the TECSTA register is set. This event also sets the TECXFLTIFG interrupt flag. When TECXFLTIFG is set to logical 1, the TECXFLTxSTA status bits show which external fault signal or signals are active. The TECXFLTHLDx control bit holds the external fault signal. Clearing the TECXFLTxSTA status bits also resets the held signal back to zero.

1.2.3.1 External Input Events Affect Timer Output

Figure 1-2 shows how the external signals affect the Timer_D output in a Power Factor Corrector (PFC) application.

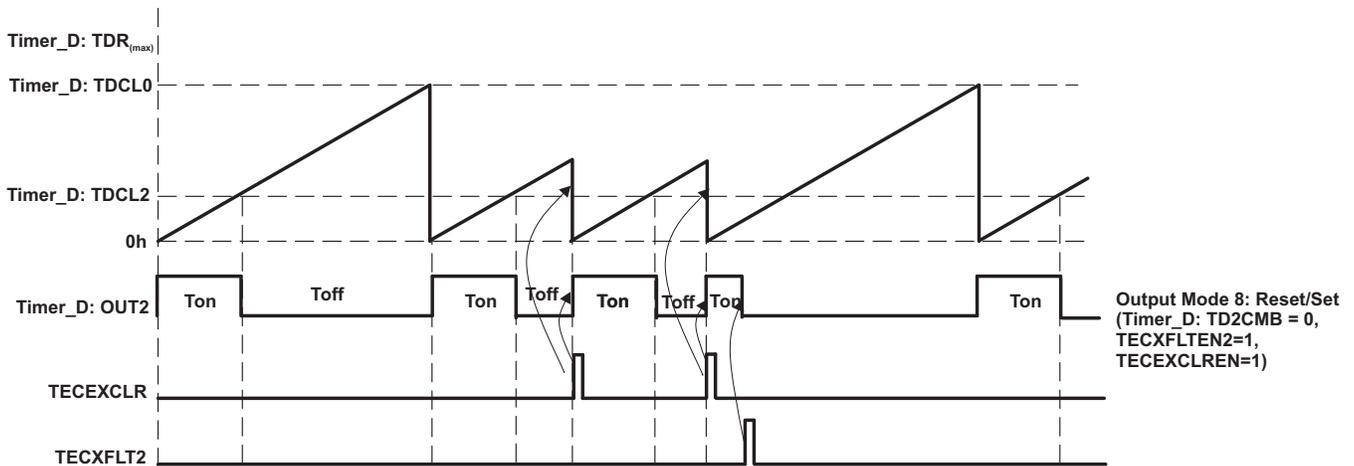


Figure 1-2. External Input Events Affect Timer_D Output

Figure 1-3 shows an example in which channels are combined.

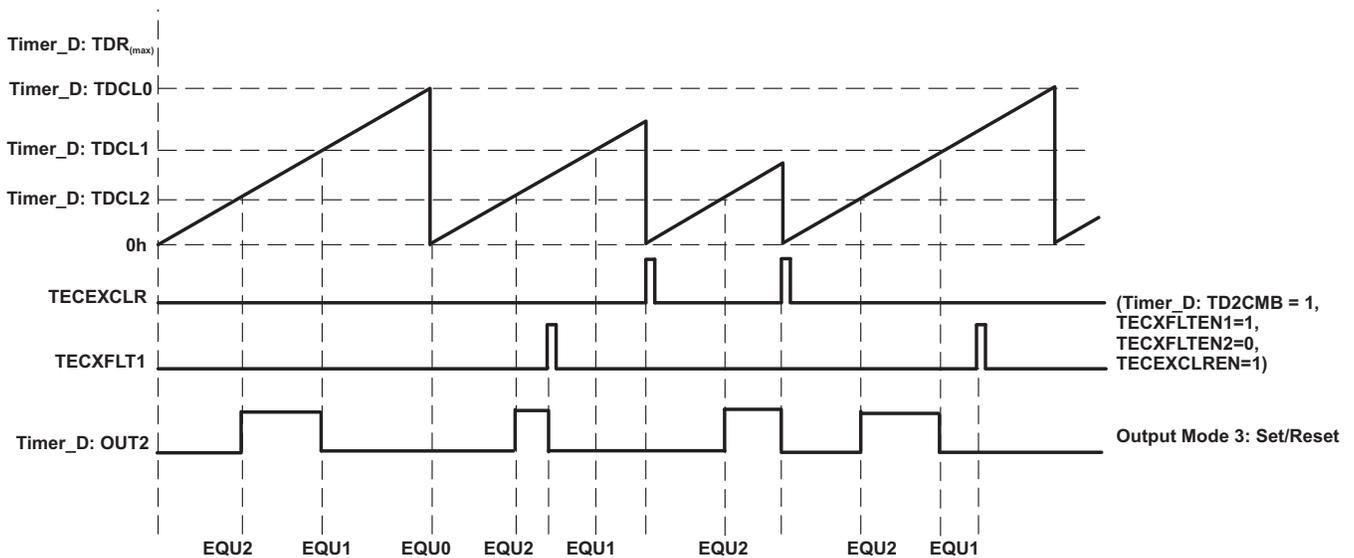


Figure 1-3. Timer_D Output With Channel Combination

1.2.4 Module Level Connection Between TEC and Timer_D

The TEC and Timer_D modules are connected through internal signals. Figure 1-4 shows the interconnection between TEC and Timer_D module. See the [Timer_D chapter](#) for more Timer_D module information.

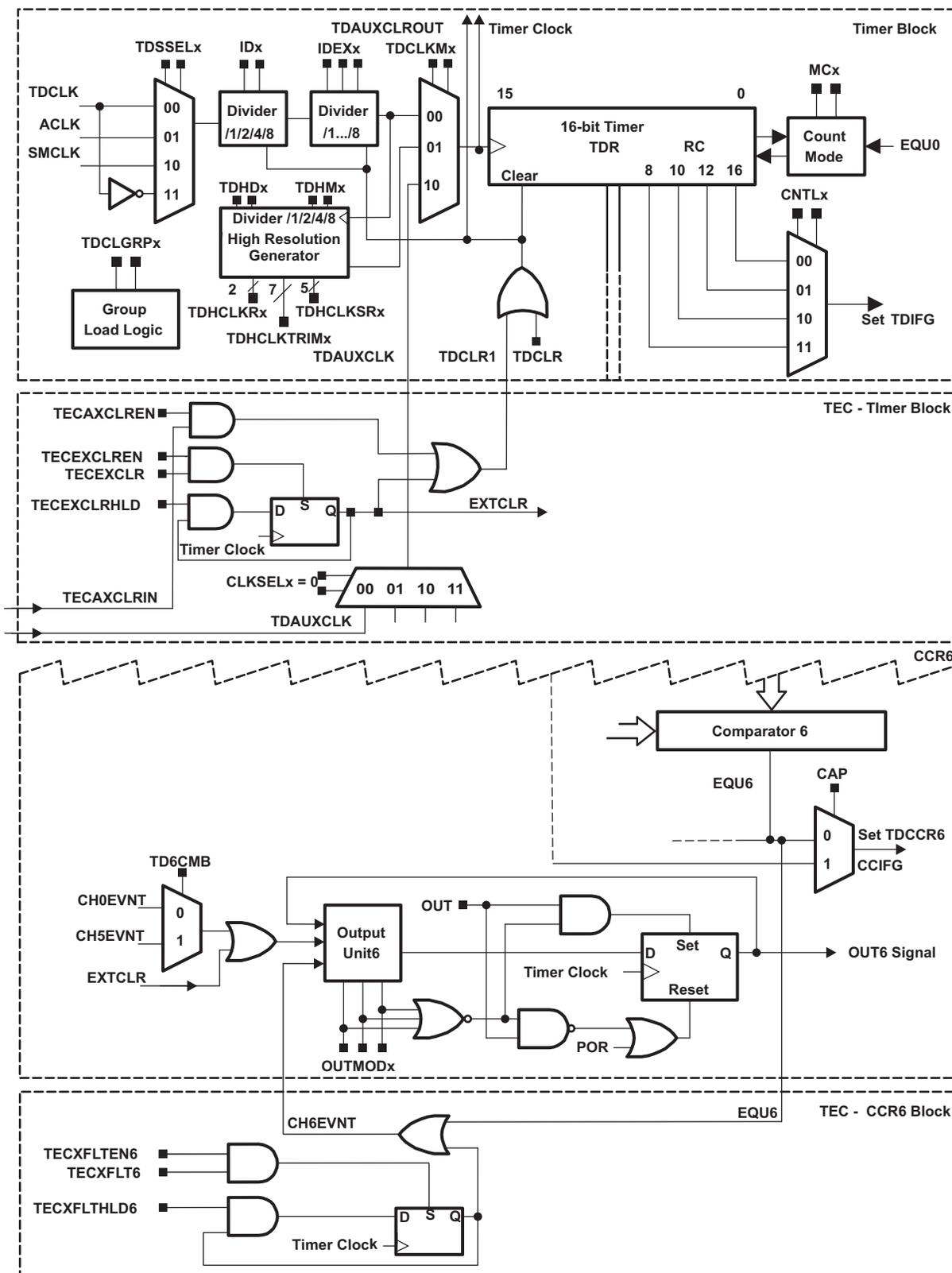


Figure 1-4. Module Level Connection Between TEC and Timer_D

1.2.5 Synchronization Mechanism Between Timer_D Instances

Two or more Timer_D modules can be synchronized to each other. One instance can be the master of the other Timer_D instance (slave). The master is the instance that supplies the clock to the other instance. If two timer instances are synchronized to each other, then there is a device specific order; for example, Timer0_D is the master of Timer1_D. The slave uses the settings of the TDHEN bit, the CNTLx bits, and the MCx bits of the master. The CCR0 registers of the master and the slave must be programmed to equal values. Figure 1-5 shows the combination of a Timer_D master and a Timer_D slave and the control signals routed through the TEC module of the slave. The clock generator of the Timer_D slave is powered down by selecting the TDCLKMx to accept the clock input from the Timer_D master. The TECEXCLR signals of the slave timers do not propagate to the master but the clear events of the master timers are signaled to the slave timers. See Figure Figure 1-5 for the detailed signal routing between master and slave. The divider and clock selector settings of the slave timers are ignored. The high resolution generator of the slave timer is disabled.

The Example 1-1 shows how to program the master timer and the slave timer to synchronize them.

Example 1-1.

```
// Example: TD0 is master timer, TD1 is slave timer
//          Period is 200. TD0 channel 1: 20% duty cycle. TD0 channel 2: 40% duty cycle
//          TD1 channel 1: 60% duty cycle. TD1 channel 2: 80% duty cycle
// Configure Master TD0
    TD0CTL0 = TDSSEL_2;           // TDCLK = SMCLK = Hi-Res input clk
    TD0CTL1 |= TDCLKM_1;        // TD0 clock = Hi-res local clock
    TD0HCTL0 = TDHM_0 + TDHREGEN + TDHEN; // Hi-res clock 8x TDCLK,
//
Regulation and Hi-res mode enable
// TD0HINT |= TDHLKIE;         // Set TDH Lock IFG -
// not used in the example

// Configure Slave TD1
    TD1CTL1 = TDCLKM_2;         // TD1 clock = Auxiliary clock source from
master
//
timer instance
// Configure Slave TEC1
    TEC1XCTL2 |= TECAxCLREN;
// Enable synchronized clear

// Configure TD0 and its PWM outputs
    TD0CTL0 |= TDCLR;          // Clear timer counter master+slave

    TD0CCR0 = 200;              // TD0CCR0
    TD0CCR1 = 40;               // 20% dutycycle
    TD0CCTL1 |= OUTMOD_7;      // TD0CCR1, Reset/Set
    TD0CCR2 = 80;              // 40% dutycycle
    TD0CCTL2 |= OUTMOD_7;      // TD0CCR2, Reset/Set

// Configure TD1 PWM outputs
    TD1CCR0 = 200;              // TD1CCR0
    TD1CCR1 = 120;              // 60% dutycycle
    TD1CCTL1 |= OUTMOD_7;      // TD1CCR1, Reset/Set
    TD1CCR2 = 160;              // 80% dutycycle
    TD1CCTL2 |= OUTMOD_7;      // TD1CCR2, Reset/Set

// Start timers and select Up-mode
    TD0CTL0 |= MC_1 + TDCLR;    // up-mode, start timer
```

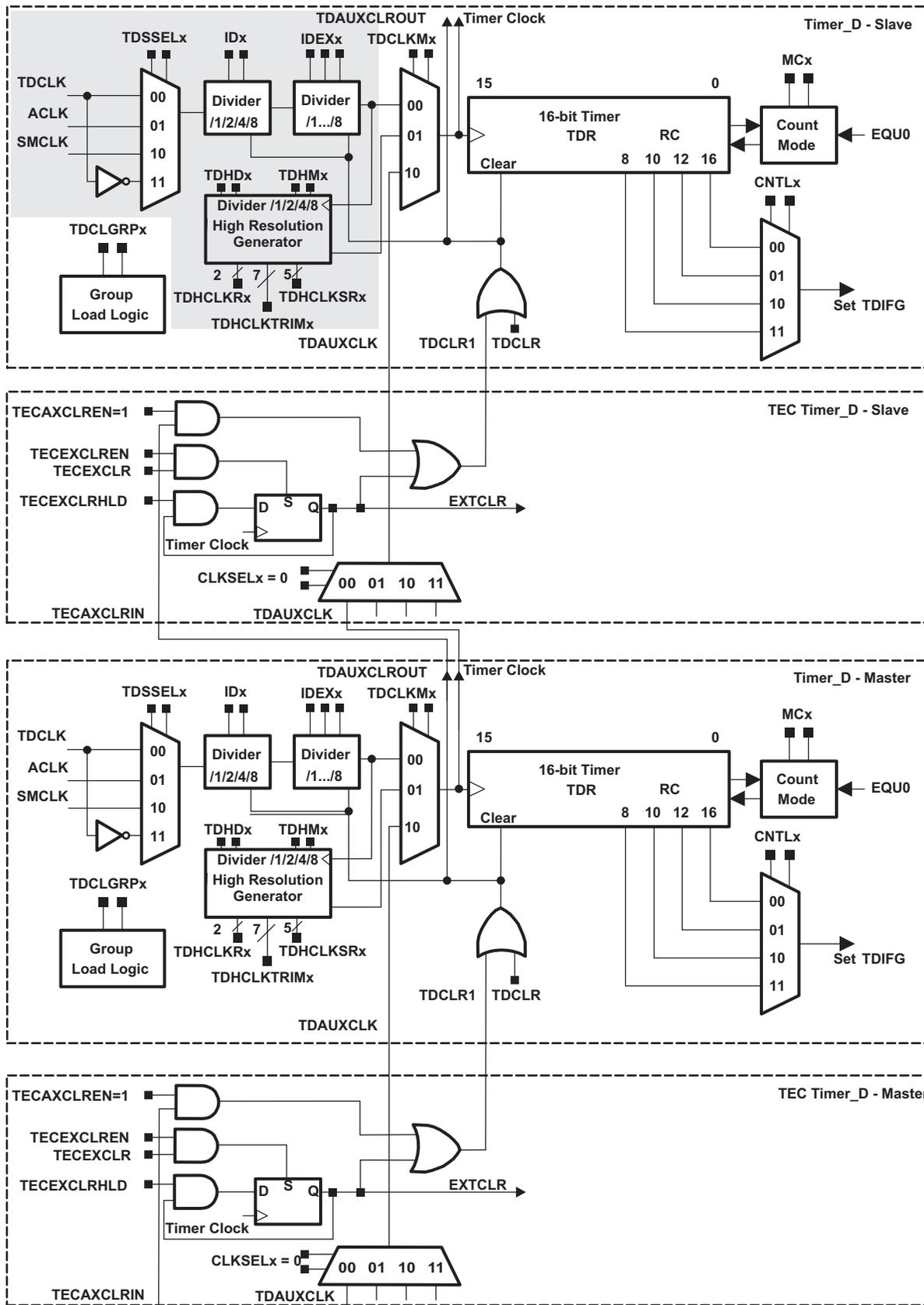


Figure 1-5. Synchronization Between Timer Instances

1.2.6 Timer Event Control Interrupts

The TEC module has only one interrupt vector, TECxIV.

1.2.6.1 TECxIV, Interrupt Vector Generator

The external fault interrupt TECXFLTIFG, the external clear interrupt TECEXCLRIFG, and the auxiliary clear interrupt TECAXCLRIFG are prioritized and combined to source a single interrupt vector. The interrupt vector register TECxIV is used to determine which flag requested an interrupt.

The highest-priority enabled interrupt generates a number in the TECxIV register (see [Section 1.3.6](#)). This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled TEC interrupts do not affect the TECxIV value.

Read access of the TECxIV register automatically resets the highest-pending interrupt flag. If another interrupt flag is set, another interrupt is immediately generated after servicing the initial interrupt.

Write access of the TECxIV register clears all pending interrupt conditions and flags.

1.3 TEC Registers

The Timer Event Control registers are listed in [Table 1-1](#). The base address can be found in the device-specific data sheet. The address offset is listed in [Table 1-1](#).

Table 1-1. TEC Registers

Offset	Acronym	Register Name	Type	Reset	Section
0000h	TECxCTL0	Timer Event Control External Control 0	Read/write	0000h	Section 1.3.1
0002h	TECxCTL1	Timer Event Control External Control 1	Read/write	0000h	Section 1.3.2
0004h	TECxCTL2	Timer Event Control External Control 2	Read/write	0000h	Section 1.3.3
0006h	TECxSTA	Timer Event Control Status	Read/write	0000h	Section 1.3.4
0008h	TECxINT	Timer Event Control External Interrupt	Read/write	0000h	Section 1.3.5
000Ah	TECxIV	Timer Event Control Interrupt Vector	Read only	0000h	Section 1.3.6

1.3.1 TECxCTL0 Register

Timer Event Control External Control Register 0

Figure 1-6. TECxCTL0 Register

15	14	13	12	11	10	9	8
Reserved	TECXFLTEN6	TECXFLTEN5	TECXFLTEN4	TECXFLTEN3	TECXFLTEN2	TECXFLTEN1	TECXFLTEN0
r0	rw-(0)						
7	6	5	4	3	2	1	0
Reserved	TECXFLTHLD6	TECXFLTHLD5	TECXFLTHLD4	TECXFLTHLD3	TECXFLTHLD2	TECXFLTHLD1	TECXFLTHLD0
r0	rw-(0)						

Table 1-2. TECxCTL0 Register Description

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads as 0.
14	TECXFLTEN6	RW	0h	External fault signal enable for channel event block 6 (only available on TEC7) 0b = External fault signal is disabled for CE6 1b = External fault signal is enabled for CE6
13	TECXFLTEN5	RW	0h	External fault signal enable for channel event block 5 (only available on TEC7) 0b = External fault signal is disabled for CE5 1b = External fault signal is enabled for CE5
12	TECXFLTEN4	RW	0h	External fault signal enable for channel event block 4 (only available on TEC5 or TEC7) 0b = External fault signal is disabled for CE4 1b = External fault signal is enabled for CE4
11	TECXFLTEN3	RW	0h	External fault signal enable for channel event block 3 (only available on TEC5 or TEC7) 0b = External fault signal is disabled for CE3 1b = External fault signal is enabled for CE3
10	TECXFLTEN2	RW	0h	External fault signal enable for channel event block 2 0b = External fault signal is disabled for CE2 1b = External fault signal is enabled for CE2
9	TECXFLTEN1	RW	0h	External fault signal enable for channel event block 1 0b = External fault signal is disabled for CE1 1b = External fault signal is enabled for CE1
8	TECXFLTEN0	RW	0h	External fault signal enable for channel event block 0 0b = External fault signal is disabled for CE0 1b = External fault signal is enabled for CE0
7	Reserved	R	0h	Reserved. Always reads as 0.
6	TECXFLTHLD6	RW	0h	External fault signal hold bit for CE6 0b = External fault signal is not held 1b = External fault signal is held
5	TECXFLTHLD5	RW	0h	External fault signal hold bit for CE5 0b = External fault signal is not held 1b = External fault signal is held
4	TECXFLTHLD4	RW	0h	External fault signal hold bit for CE4 0b = External fault signal is not held 1b = External fault signal is held
3	TECXFLTHLD3	RW	0h	External fault signal hold bit for CE3 0b = External fault signal is not held 1b = External fault signal is held

Table 1-2. TECxCTL0 Register Description (continued)

Bit	Field	Type	Reset	Description
2	TECXFLTHLD2	RW	0h	External fault signal hold bit for CE2 0b = External fault signal is not held 1b = External fault signal is held
1	TECXFLTHLD1	RW	0h	External fault signal hold bit for CE1 0b = External fault signal is not held 1b = External fault signal is held
0	TECXFLTHLD0	RW	0h	External fault signal hold bit for CE0 0b = External fault signal is not held 1b = External fault signal is held

1.3.2 TECxCTL1 Register

Timer Event Control External Control Register 1

Figure 1-7. TECxCTL1 Register

15	14	13	12	11	10	9	8
Reserved	TECXFLTLVS6	TECXFLTLVS5	TECXFLTLVS4	TECXFLTLVS3	TECXFLTLVS2	TECXFLTLVS1	TECXFLTLVS0
r0	rw-(0)						
7	6	5	4	3	2	1	0
Reserved	TECXFLTPOL6	TECXFLTPOL5	TECXFLTPOL4	TECXFLTPOL3	TECXFLTPOL2	TECXFLTPOL1	TECXFLTPOL0
r0	rw-(0)						

Table 1-3. TECxCTL1 Register Description

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads as 0.
14	TECXFLTLVS6	RW	0h	Signal type of external fault 6 0b = Edge sensitive 1b = Level sensitive
13	TECXFLTLVS5	RW	0h	Signal type of external fault 5 0b = Edge sensitive 1b = Level sensitive
12	TECXFLTLVS4	RW	0h	Signal type of external fault 4 0b = Edge sensitive 1b = Level sensitive
11	TECXFLTLVS3	RW	0h	Signal type of external fault 3 0b = Edge sensitive 1b = Level sensitive
10	TECXFLTLVS2	RW	0h	Signal type of external fault 2 0b = Edge sensitive 1b = Level sensitive
9	TECXFLTLVS1	RW	0h	Signal type of external fault 1 0b = Edge sensitive 1b = Level sensitive
8	TECXFLTLVS0	RW	0h	Signal type of external fault 0 0b = Edge sensitive 1b = Level sensitive
7	Reserved	R	0h	Reserved. Always reads as 0.
6	TECXFLTPOL6	RW	0h	Polarity bit of external fault 6 0b = Selects falling edge in edge sensitive or low level in level sensitive 1b = Selects rising edge in edge sensitive or high level in level sensitive
5	TECXFLTPOL5	RW	0h	Polarity bit of external fault 5 0b = Selects falling edge in edge sensitive or low level in level sensitive 1b = Selects rising edge in edge sensitive or high level in level sensitive
4	TECXFLTPOL4	RW	0h	Polarity bit of external fault 4 0b = Selects falling edge in edge sensitive or low level in level sensitive 1b = Selects rising edge in edge sensitive or high level in level sensitive
3	TECXFLTPOL3	RW	0h	Polarity bit of external fault 3 0b = Selects falling edge in edge sensitive or low level in level sensitive 1b = Selects rising edge in edge sensitive or high level in level sensitive
2	TECXFLTPOL2	RW	0h	Polarity bit of external fault 2 0b = Selects falling edge in edge sensitive or low level in level sensitive 1b = Selects rising edge in edge sensitive or high level in level sensitive

Table 1-3. TECxCTL1 Register Description (continued)

Bit	Field	Type	Reset	Description
1	TECXFLTPOL1	RW	0h	Polarity bit of external fault 1 0b = Selects falling edge in edge sensitive or low level in level sensitive 1b = Selects rising edge in edge sensitive or high level in level sensitive
0	TECXFLTPOL0	RW	0h	Polarity bit of external fault 0 0b = Selects falling edge in edge sensitive or low level in level sensitive 1b = Selects rising edge in edge sensitive or high level in level sensitive

1.3.3 TECxCTL2 Register

Timer Event Control External Control Register 2

Figure 1-8. TECxCTL2 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved	TECEXCLRLVS	TECEXCLRPOL	TECEXCLRHLDD	TECEXCLREN	TECAXCLREN	CLKSELx	
r0	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Table 1-4. TECxCTL2 Register Description

Bit	Field	Type	Reset	Description
15-7	Reserved	R	0h	Reserved. Always reads as 0.
6	TECEXCLRLVS	RW	0h	Signal type of external clear 0b = Edge sensitive 1b = Level sensitive
5	TECEXCLRPOL	RW	0h	Polarity bit of external clear 0b = Selects falling edge in edge sensitive or low level in level sensitive 1b = Selects rising edge in edge sensitive or high level in level sensitive
4	TECEXCLRHLDD	RW	0h	External clear signal hold bit 0b = External clear signal is not held 1b = External clear signal is held
3	TECEXCLREN	RW	0h	External clear signal control bit 0b = External clear signal disabled 1b = External clear signal enabled
2	TECAXCLREN	RW	0h	Auxiliary clear signal control bit 0b = Auxiliary clear signal disabled 1b = Auxiliary clear signal enabled
1-0	CLKSELx	RW	0h	Auxiliary clock source selection bits 00b = Clock input from a Timer_D master instance 01b = Reserved 10b = Reserved 11b = Reserved

1.3.4 TECxSTA Register

Timer Event Control Status Register

Figure 1-9. TECxSTA Register

15	14	13	12	11	10	9	8
Reserved							TECXCLRSTA
r0	r0	r0	r0	r0	r0	r0	rw-(0)
7	6	5	4	3	2	1	0
Reserved	TECXFLT6STA	TECXFLT5STA	TECXFLT4STA	TECXFLT3STA	TECXFLT2STA	TECXFLT1STA	TECXFLT0STA
r0	rw-(0)						

Table 1-5. TECxSTA Register Description

Bit	Field	Type	Reset	Description
15-9	Reserved	R	0h	Reserved. Always reads as 0.
8	TECXCLRSTA	RW	0h	External clear status flag. This bit is set if the external clear input is detected. If the bit is set it remains set until cleared by writing 0 to it. 0b = No external clear detected 1b = External clear detected
7	Reserved	R	0h	Reserved. Always reads as 0.
6	TECXFLT6STA	RW	0h	External fault status flag. This bit is set if the external fault signal in CE6 is detected. If the bit is set it remains set until cleared by writing 0 to it. 0b = No external fault detected 1b = External fault detected
5	TECXFLT5STA	RW	0h	External fault status flag. This bit is set if the external fault signal in CE5 is detected. If the bit is set it remains set until cleared by writing 0 to it. 0b = No external fault detected 1b = External fault detected
4	TECXFLT4STA	RW	0h	External fault status flag. This bit is set if the external fault signal in CE4 is detected. If the bit is set it remains set until cleared by writing 0 to it. 0b = No external fault detected 1b = External fault detected
3	TECXFLT3STA	RW	0h	External fault status flag. This bit is set if the external fault signal in CE3 is detected. If the bit is set it remains set until cleared by writing 0 to it. 0b = No external fault detected 1b = External fault detected
2	TECXFLT2STA	RW	0h	External fault status flag. This bit is set if the external fault signal in CE2 is detected. If the bit is set it remains set until cleared by writing 0 to it. 0b = No external fault detected 1b = External fault detected
1	TECXFLT1STA	RW	0h	External fault status flag. This bit is set if the external fault signal in CE1 is detected. If the bit is set it remains set until cleared by writing 0 to it. 0b = No external fault detected 1b = External fault detected
0	TECXFLT0STA	RW	0h	External fault status flag. This bit is set if the external fault signal in CE0 is detected. If the bit is set it remains set until cleared by writing 0 to it. 0b = No external fault detected 1b = External fault detected

1.3.5 TECxINT Register

Timer Event Control External Interrupt Register

Figure 1-10. TECxINT Register

15	14	13	12	11	10	9	8
Reserved					TECXFLTIE	TECEXCLRIE	TECAXCLRIE
r0	r0	r0	r0	r0	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
Reserved					TECXFLTIFG	TECEXCLRIFG	TECAXCLRIFG
r0	r0	r0	r0	r0	rw-(0)	rw-(0)	rw-(0)

Table 1-6. TECxINT Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10	TECXFLTIE	RW	0h	External fault interrupt enable. This bit enables the TECXFLTIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled
9	TECEXCLRIE	RW	0h	External clear interrupt enable. This bit enables the TECEXCLRIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled
8	TECAXCLRIE	RW	0h	Auxiliary interrupt enable. This bit enables the TECAXCLRIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled
7-3	Reserved	R	0h	Reserved. Always reads as 0.
2	TECXFLTIFG	RW	0h	External fault interrupt flag. This bit is set if one of the external fault signal TECXFLTx is detected. Software has to look into the control register TECSTA to find out which one it is. If the bit is set it remains set until cleared by reading it or writing a 0 to it. 0b = No interrupt pending 1b = Interrupt pending
1	TECEXCLRIFG	RW	0h	External clear interrupt flag. This bit is set if the external clear signal is detected. If the bit is set it remains set until cleared by reading it or writing a 0 to it. 0b = No interrupt pending 1b = Interrupt pending
0	TECAXCLRIFG	RW	0h	Auxiliary clear interrupt flag. This bit is set if the auxiliary clear signal is detected. If the bit is set it remains set until cleared by reading it or writing a 0 to it. 0b = No interrupt pending 1b = Interrupt pending

1.3.6 TECxIV Register

Timer Event Control Interrupt Vector Register

Figure 1-11. TECxIV Register

15	14	13	12	11	10	9	8
TECxIVx							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
TECxIVx							
r0	r0	r0	r0	r0	r-(0)	r-(0)	r0

Table 1-7. TECxIV Register Description

Bit	Field	Type	Reset	Description
15-0	TECxIVx	R	0h	TEC external interrupt vector value 00h = No interrupt pending 02h = Interrupt Source: External fault; Interrupt Flag: TECXFLTIFG; Interrupt Priority: Highest 04h = Interrupt Source: External clear; Interrupt Flag: TECEXCLRIFG 06h = Interrupt Source: Auxiliary clear; Interrupt Flag: TECAXCLRIFG; Interrupt Priority: Lowest

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