LDO-PWR Module

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. Click here to download the latest version of the full user's guide: SLAU208.

This chapter describes the LDO-PWR module that is available in some devices.

Topic **Page**

1.1 LDO-PWR Introduction

The features of the LDO-PWR module include:

- Integrated 3.3-V LDO regulator with sufficient output to power the entire MSP430™ microcontroller and system circuitry from 5-V external supply
- Current-limiting capability on 3.3-V LDO output with detection flag and interrupt generation
- LDO input voltage detection flag and interrupt generation

Figure 1-1 shows a block diagram of the LDO-PWR module.

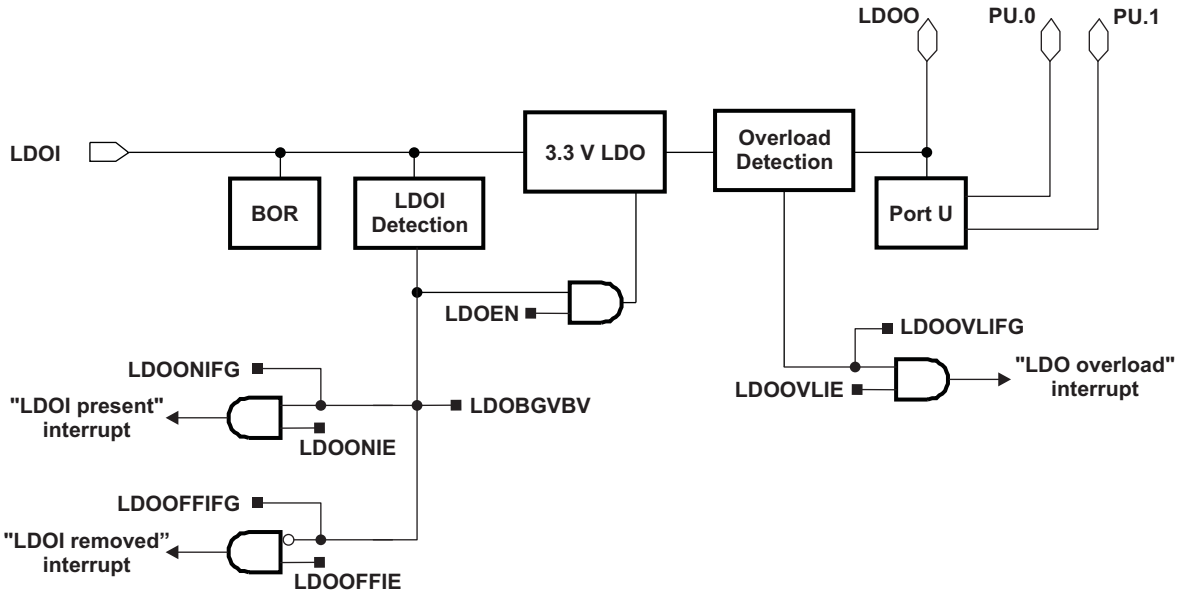

Figure 1-1. LDO Block Diagram

1.2 LDO-PWR Operation

The LDO-PWR power system incorporates an integrated 3.3-V LDO regulator that allows the entire MSP430 microcontroller to be powered from nominal 5-V LDOI when it is made available from the system. Alternatively, the power system can supply power only to other components within the system, or it can be unused altogether. The LDO-PWR, when enabled, also supplies power to Port U.

1.2.1 Enabling/Disabling

The 3.3-V LDO is enabled/disabled by setting/clearing LDOEN (LDOEN = 1 by default). If the voltage on LDOI is detected to be low or nonexistent, the LDO is suspended even if enabled by LDOEN = 1. No additional current is consumed while the LDO is suspended. When the voltage on LDOI rises above the LDO power brownout level, the LDO reference and low voltage detection become enabled. When the voltage on LDOI rises further above the launch voltage V_{LAUNCH}, the 3.3-V LDO becomes enabled (see Figure 1-2). See device-specific data sheet for value of V_{LAUNCH}.

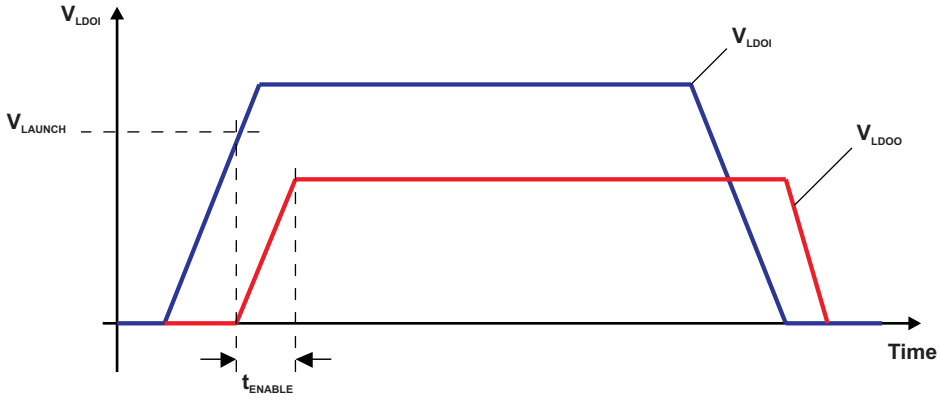

Figure 1-2. 3.3-V LDO Power Up/Down Profile

1.2.2 Powering the Rest of the MSP430 from the LDO-PWR

The output of the 3.3-V LDO (LDOO) can be used to power the entire MSP430 device, sourcing the DVCC rail. If this is desired, LDOO and DVCC should be connected externally. Power from the 3.3-V LDO is sourced into DVCC (see Figure 1-3).

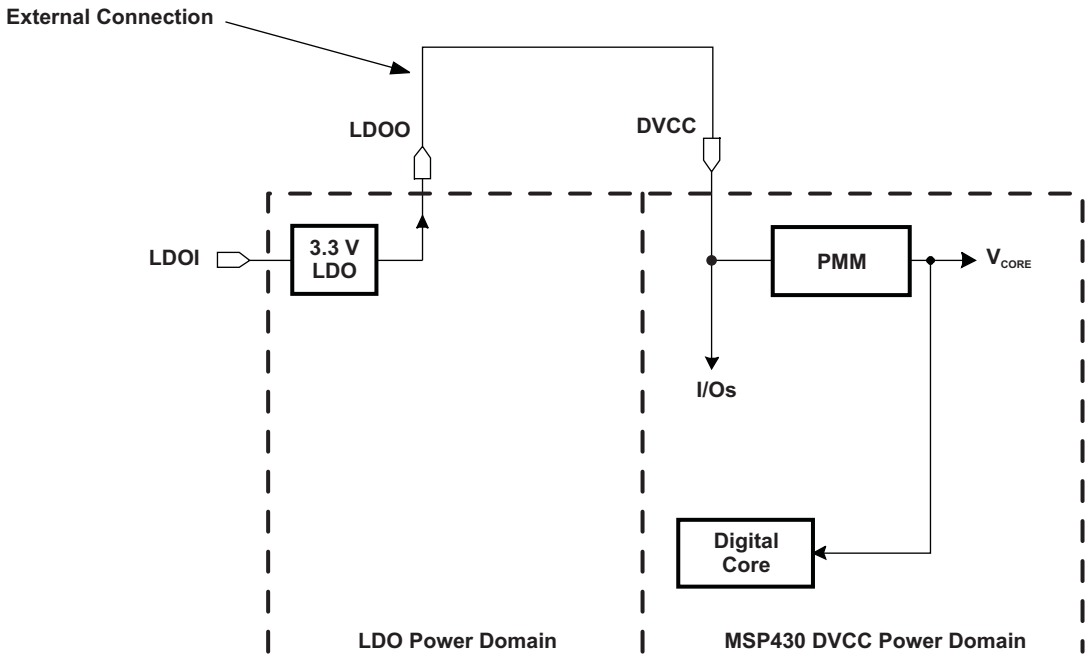

Figure 1-3. Powering Entire MSP430 From LDOI

With this connection made, the MSP430 allows for autonomous power up of the device when the voltage on LDOI rises above V_{LAUNCH}. If no voltage is present on V_{CORE} – meaning the device is unpowered (or, in LPMx.5 mode) – then the 3.3-V LDO automatically turns on when the voltage on LDOI rises above V_{LAUNCH}.

Note that if DVCC is being driven from the 3.3-V LDO in this manner, and if power is available from LDOI, attempting to place the device into LPMx.5 results in the device immediately re-powering. This is because it recreates the conditions of the autonomous feature described above (no V_{CORE} but power available on LDOI). The resulting drop of V_{CORE} would cause the system to immediately power up again.

When DVCC is being powered from LDOI, it is up to the user to ensure that the total current being drawn from LDOI stays below the current overload detection, I_{DET}.

1.2.3 Powering Other Components in the System from LDO-PWR

There is sufficient current capacity available from the 3.3-V LDO to power not only the entire MSP430 but also other components in the system, via the LDOO pin. It is also possible to use the 3.3-V LDO only to power other components in the system.

1.2.4 Applications That Do Not Require LDO-PWR

There may be applications where the 3.3-V LDO is not required. In these cases, keep LDOI tied low to prevent the 3.3-V LDO from turning on and drawing any current even if LDOEN = 1. If Port U operation is desired, since the 3.3-V LDO is not enabled, an external voltage to the LDOO pin is required.

1.2.5 Current Limitation and Overload Protection

The 3.3-V LDO features current limitation to protect itself from an overload condition; that is, when the output of the LDO becomes current-limited to I_{DET}. This is reported to software via the VUOVLIFG flag. See device-specific data sheet for value of I_{DET}.

During overload conditions, LDOO drops below its nominal output voltage. In power scenarios where DVCC is exclusively supplied from LDOO, repetitive system restarts may be triggered as long the overload condition exists. For this reason, firmware should avoid re-enabling high current draw modules after detection of an overload on the previous power session, until the cause of failure can be identified and corrected. Ultimately, it is the user's responsibility to ensure that the current drawn from LDOI does not exceed I_{DET}.

The LDO-PWR power system brownout circuit is supplied from LDOI or DVCC, whichever carries the higher voltage.

1.2.6 LDO-PWR Interrupts

The LDO-PWR module shares a single interrupt vector to handle multiple LDO-PWR interrupts.

The LDOONIFG flag can be used to indicate that the voltage on LDOI has risen above the launch voltage. In addition to the LDOONIFG being set, an interrupt is also generated when LDOONIE = 1. Similarly, the LDOOFFIFG flag can be used to indicate that the voltage on LDOI has fallen below the launch voltage. In addition to the LDOOFFIFG being set, an interrupt is also generated when LDOOFFIE = 1.The LDOBGVBV bit can also be polled to indicate the level of LDOI; that is, above or below the launch voltage.

The LDOOVLIFG flag can be used to indicate an overcurrent condition on the 3.3-V LDO. When an overcurrent condition is detected, LDOOVLIFG = 1. In addition to the LDOOVLIFG being set, an interrupt is also generated when LDOOVLIE = 1.

1.2.7 Port U Control

The Port U pins (PU.0/PU.1) function as general-purpose high-current I/O pins. These pins can only be configured together as either both inputs or both outputs. Port U is supplied by the LDOO rail. If the 3.3-V LDO is not being used in the system (disabled), the LDOO pin can be supplied externally.

PUOPE controls the enable of both outputs residing on the Port U pins. Setting PUIPE = 1 causes both input buffers to be enabled. When Port U outputs are enabled (PUOPE = 1), the PUIN0 and PUIN1 pins mirror what is present on the outputs assuming PUIPE = 1. To use the Port U pins as inputs, the outputs should be disabled by setting PUOPE = 0, and enabling the input buffers by setting PUIPE = 1. Once configured as inputs (PUIPE = 1), the PUIN0 and PUIN1 bits can be read to determine the respective input values.

When PUOPE is set, both Port U pins function as outputs, controlled by PUOUT0/PUOUT1. When driven high, they use the LDOO rail, and they are capable of a drive current higher than other I/O pins on the device. See the device-specific datasheet for parameters.

By default, PUOPE and PUIPE are cleared. PU.0/PU.1 are high-impedance (input buffers are disabled and outputs are disabled).

1.3 LDO-PWR Registers

Write access to the configuration registers is allowed or disallowed using the LDOKEYPID register. Writing the proper value (9628h) unlocks the configuration registers and enables write access. Writing any other value disables access while leaving the values of the registers intact. Locking should be done intentionally after the configuration is finished. Read access is available without the need to write to the LDOKEYPID register.

The configuration registers are listed in Table 1-1. All addresses are expressed as offsets; the base address can be found in the device-specific data sheet.

All registers are byte and word accessible.

Table 1-1. LDO-PWR Registers

Offset	Acronym	Register Name	Type	Reset	Section
00h	LDOKEYPID	LDO key and ID register	Read/Write	0000h	Section 1.3.1
04h	PUCTL	Port U control register	Read/Write	0000h	Section 1.3.2
08h	LDOPWRCTL	LDO-PWR control register	Read/Write	0810h	Section 1.3.3

1.3.1 LDOKEYPID Register

LDO Key Register

Figure 1-4. LDOKEYPID Register

15	14	13	12	11	10	9	8
LDOKEY							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
LDOKEY							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-2. LDOKEYPID Register Description

Bit	Field	Type	Reset	Description
15-0	LDOKEY	RW	0h	Key register. Must be written with a value of 9628h in order to be recognized as a valid key. This "unlocks" the configuration registers. If written with any other value, the registers become "locked". Reads back as A528h if the registers are unlocked.

1.3.2 PUCTL Register

Port U Control Register

Figure 1-5. PUCTL Register

15	14	13	12	11	10	9	8
Reserved						Reserved	PUIPE
r0	r0	r0	r0	r0	r0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved		PUOPE	Reserved	PUIN1	PUIN0	PUOUT1	PUOUT0
r0	r0	rw-0	rw-0	r	r	rw-0	rw-0

Can be modified only when LDOKEYPID is unlocked.

Table 1-3. PUCTL Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	R	0h	Reserved. Always reads as 0.
9	Reserved	RW	0h	Reserved. Always write as 0.
8	PUIPE	RW	0h	PU input enable 0b = PU.0 and PU.1 inputs are disabled 1b = PU.0 and PU.1 inputs are enabled
7-6	Reserved	R	0h	Reserved. Always reads as 0.
5	PUOPE	RW	0h	PU output enable 0b = PU.0 and PU.1 outputs are disabled 1b = PU.0 and PU.1 outputs are enabled
4	Reserved	R	0h	Reserved. Always write as 0.
3	PUIN1	R	0h	PU.1 input data, This bit reflects the logic value on the PU.1 terminal when PUIPE = 1.
2	PUIN0	R	0h	PU.0 input data, This bit reflects the logic value on the PU.0 terminal when PUIPE = 1.
1	PUOUT1	RW	0h	PU.1 output data. This bits defines the value of the PU.1 pin when PUOPE = 1.
0	PUOUT0	RW	0h	PU.0 output data. This bits defines the value of the PU.0 pin when PUOPE = 1.

1.3.3 LDOPWRCTL Register

LDO-Power Control Register

Figure 1-6. LDOPWRCTL Register

15	14	13	12	11	10	9	8
Reserved			Reserved	LDOEN	LDOOFFIE	LDOONIE	LDOOVLIE
r0	r0	r0	rw-0	rw-1	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved		OVLAOFF	Reserved	LDOBGVBV	LDOOFFIFG	LDOONIFG	LDOOVLIFG
r0	r0	rw-0	rw-1	r	rw-0	rw-0	rw-0

Can be modified only when LDOKEYPID is unlocked.

Table 1-4. LDOPWRCTL Register Description

Bit	Field	Type	Reset	Description
15-13	Reserved	R	0h	Reserved. Always reads as 0.
12	Reserved	RW	0h	Reserved. Always reads as 0.
11	LDOEN	RW	1h	3.3V LDO enable. When set, the LDO is enabled. 0b = LDO disabled 1b = LDO enabled
10	LDOOFFIE	RW	0h	LDOI voltage "going OFF" interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
9	LDOONIE	RW	0h	LDOI voltage "coming ON" interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
8	LDOOVLIE	RW	0h	LDO overload indication interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
7-6	Reserved	R	0h	Reserved. Always reads as 0.
5	OVLAOFF	RW	0h	LDO overload auto-off enable 0b = During an overload on the 3.3-V LDO, the LDO automatically enters current-limiting mode and stays there until the condition stops. 1b = An overload indication clears the LDOEN bit.
4	Reserved	RW	1h	Reserved
3	LDOBGVBV	RW	0h	LDOI valid 0b = LDOI is not valid yet 1b = LDOI is valid and within bounds
2	LDOOFFIFG	RW	0h	LDOI "going OFF" interrupt flag. This bit indicates that LDOI fell below the launch voltage. 0b = LDOI did not fall below the launch voltage. 1b = LDOI fell below the launch voltage.
1	LDOONIFG	RW	0h	LDOI "coming ON" interrupt flag. This bit indicates that LDOI rose above the launch voltage. 0b = LDOI did not rise above the launch voltage. 1b = LDOI rose above the launch voltage.
0	LDOOVLIFG	RW	0h	LDO overload interrupt flag. This bit indicates that the 3.3-V LDO entered an overload condition. 0b = No overload condition detected. 1b = Overload condition detected.

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