User's Guide
SLAU554A–March 2014–Revised July 2014

AFE5401-Q1, 4-Channel, Integrated Analog Front-end Evaluation Module

This user's guide gives a general overview of the AFE5401-Q1 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the AFE5401-Q1 integrated analog front-end. The AFE5401-Q1 EVM provides a platform for evaluating the integrated signal chain under various signal, clock, reference, and ADC output formats.

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1 AFE5401-Q1 EVM Kit Contents

The AFE5401-Q1 EVM is a compact, USB-based evaluation kit for evaluating the AFE5401-Q1, a 4-channel analog front-end. The kit consists of (1) AFE5401-Q1EVM, (2) a USB cable for SPI communication to the software GUI, and (3) a +5-V AC/DC adaptor with plug adaptors for powering the EVM. Figure 1 shows an overview of the evaluation setup which includes the TSW1400 Data Capture Card (not included with this kit).

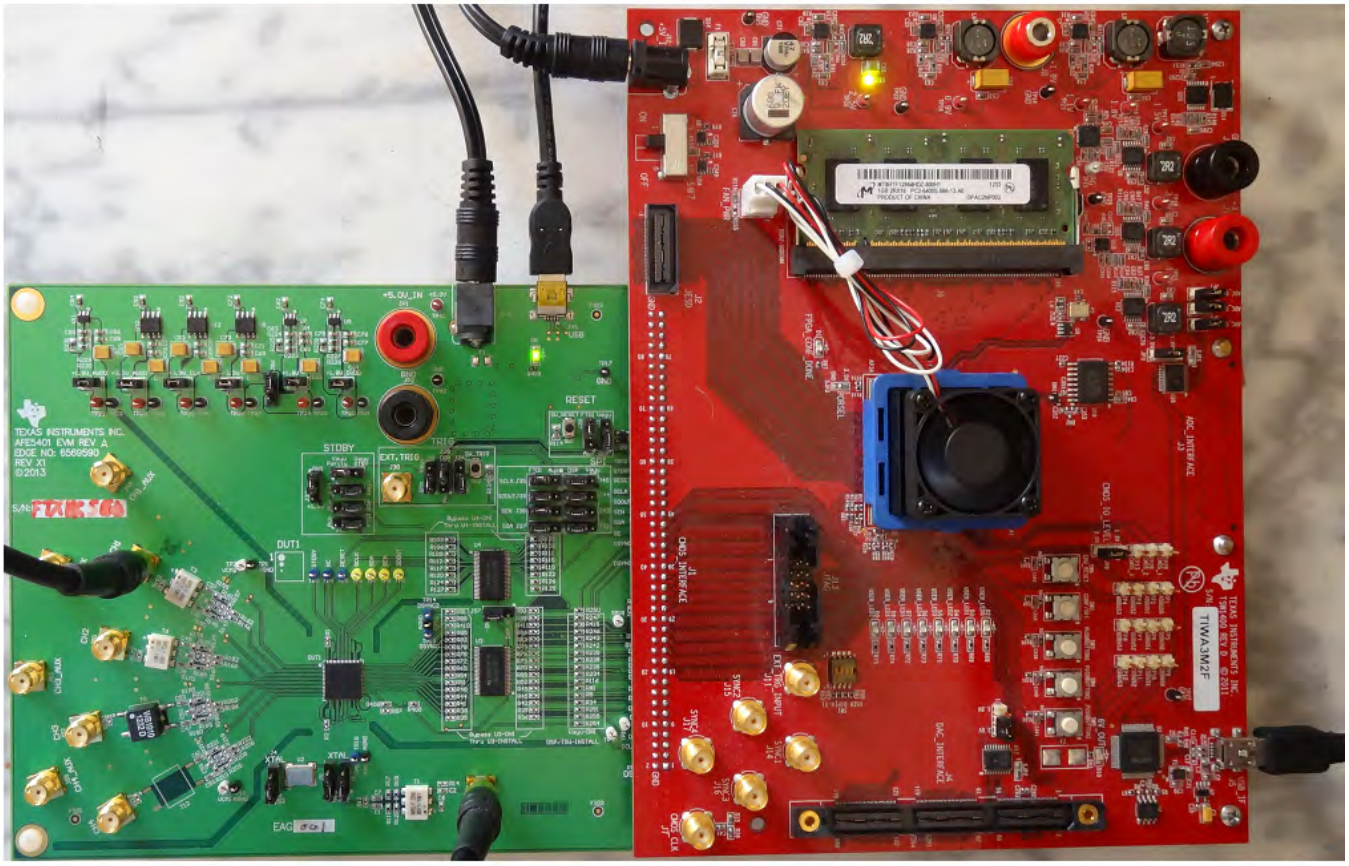


Figure 1. AFE5401-Q1 EVM (Green) with TSW1400 Capture Card (Red)

TSW1400 EVM: The high-speed LVDS de-serializer board is required for capturing data from the AFE5401-Q1EVM. The graphical user interface (GUI) software that is available with the EVM, called *High Speed Data Converter Pro*, includes many data analysis features for processing and plotting captured data. The TSW1400 EVM and software can be used to test many of TI's ADCs, DACs, and AFEs. (*NOTE: the TSW1400 capture card is not included with the AFE5401-Q1 EVM Kit and must be ordered separately*). For more information pertaining to be TSW1400EVM, see: http://focus.ti.com/docs/toolsw/folders/print/tsw1400evm.html.

Equipment: No external equipment is required to test functionality of the setup. Using the on-EVM crystal oscillator for the input clock and an internally generated RAMP test mode, the CMOS interface can be verified. When signal capture is desired, signal generators, preferably with low-phase noise and harmonic distortion, must be used as source of input signal and input clock in order to get the desired performance. Additionally, band-pass filters (BPF) are required in signal and clock paths to attenuate the harmonics and noise from the generators.

AFE5401-Q1 EVM: The AFE5401-Q1 EVM is a compact USB 2.0 based evaluation kit for the AFE5401-Q1, Quad Channel Analog Front-End. This EVM provides versatility to begin evaluation quickly and with no external equipment required as a +5-V AC/DC power supply and an on-board crystal oscillator eliminate the need for these instruments. The EVM supplies a provision for interfacing I/Os via additional external buffering or a secondary Flexible Flat Cable (FFC) connector allowing users to evaluate with their

own DSP platform (in lieu of the TSW1400 capture card). In addition, monitoring the power consumption the individual power supply pins of the AFE5401-Q1 is possible via headers. Finally, the EVM allows for three unique AFE analog input configurations including (1) a transformer with input bandwidth from 1 MHz to 400 MHz, (2) a transformer with input bandwidth from 5 kHz to 100 MHz for low frequency applications and (3) a single-ended AC coupled input drive.

USB Interface to PC: USB connections from the AFE5401-Q1EVM and TSW1400EVM to the personal computer (PC) are used for communication from the GUIs to the boards. Section 2 explains the TSW1400 and AFE5401-Q1 GUI installation procedures.

2 GUI Software Installation

The AFE5401-Q1 GUI Software provides an easy interface in which to evaluate the AFE5401-Q1. As a plug-in to the *High Speed Data Convertor Pro GUI (HSDCpro)*, control of the AFE5401-Q1 EVM and the TSW1400 Capture Card (available in separate kit from the TI estore) is done with one GUI. The GUI allows for one-click auto configuration of the AFE5401-Q1 using one of several configuration files provided with the installer. Data capture and analysis are performed by *HSDCpro* including fast-Fourier transform (FFT) analysis providing SNR, SFDR, and Harmonic Distortion.

The AFE5401-Q1 EVM and the TSW1400 EVM both require software installations. The following two sections explain where to find and how to install the software properly. Ensure that no USB connections are made to the EVMs until after the installations are complete.

2.1 High Speed Data Converter Pro (HSDCpro) GUI Installation (TSW1400 GUI)

From the Texas Instruments website, www.ti.com, search for TSW1400. Under **Technical Documents**, find the **Software** section from which **High Speed Data Converter Pro GUI Installer** can be downloaded and saved (SLWC107). Revision J (Rev J) or higher of HSDCpro is required as earlier versions are not compatible with the AFE5401-Q1 GUI.

Instructions for installing *HSDCpro* follow:

- Unzip the saved folder and run the installer executable to obtain the menu shown in Figure 2.
- Click the *Install* button.

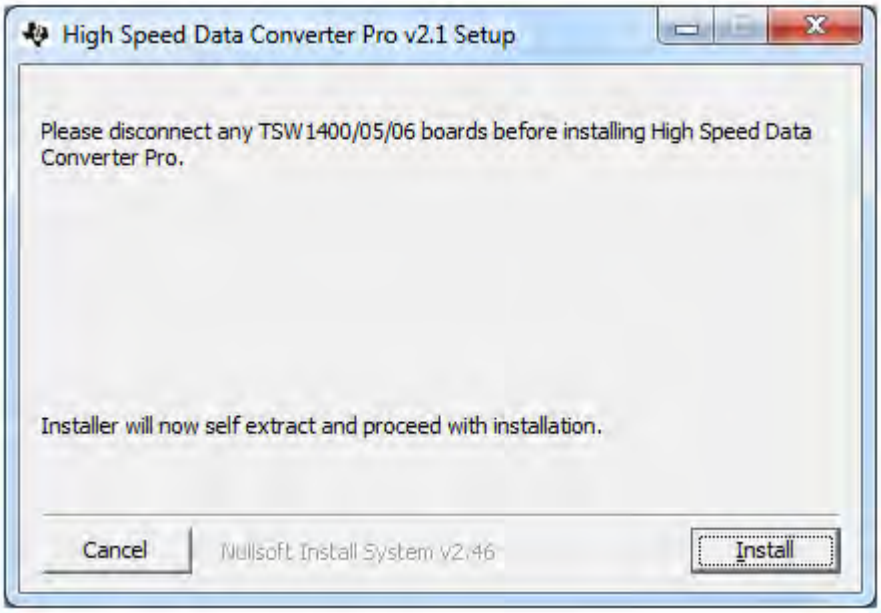


Figure 2. *HSDCpro* **Install (a)**

- Leave the destination directories as the default and press the *Next* button as shown in Figure 3.

NOTE: If a destination directory other than the default directory is used, the AFE5401-Q1 GUI is not found, therefore, it is not invoked as a plug-in tab to HSDCpro.

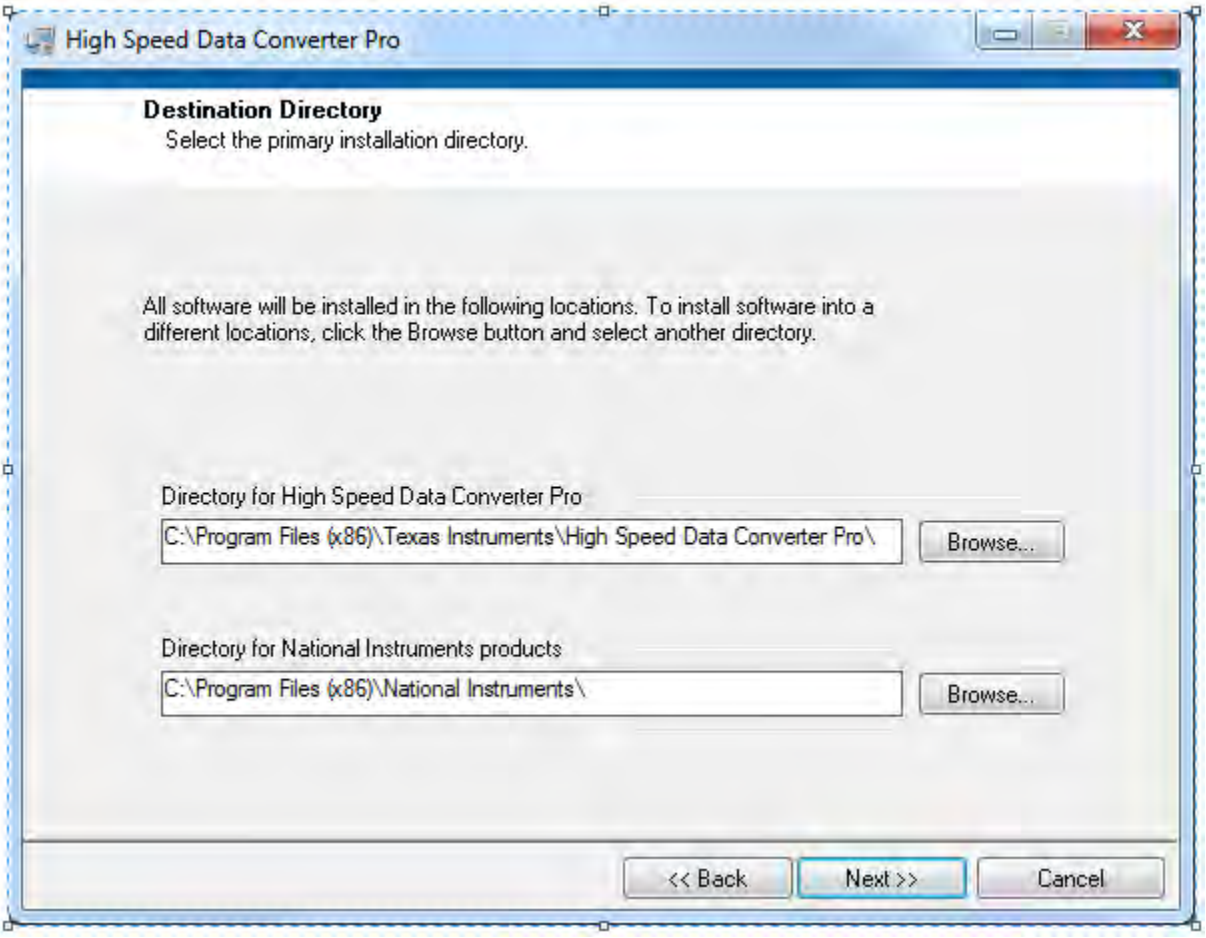


Figure 3. *HSDCpro* **Install (b)**

1. Read the License Agreement from Texas Instruments and select *I accept the License Agreement* and press the *Next* button as shown in Figure 4.

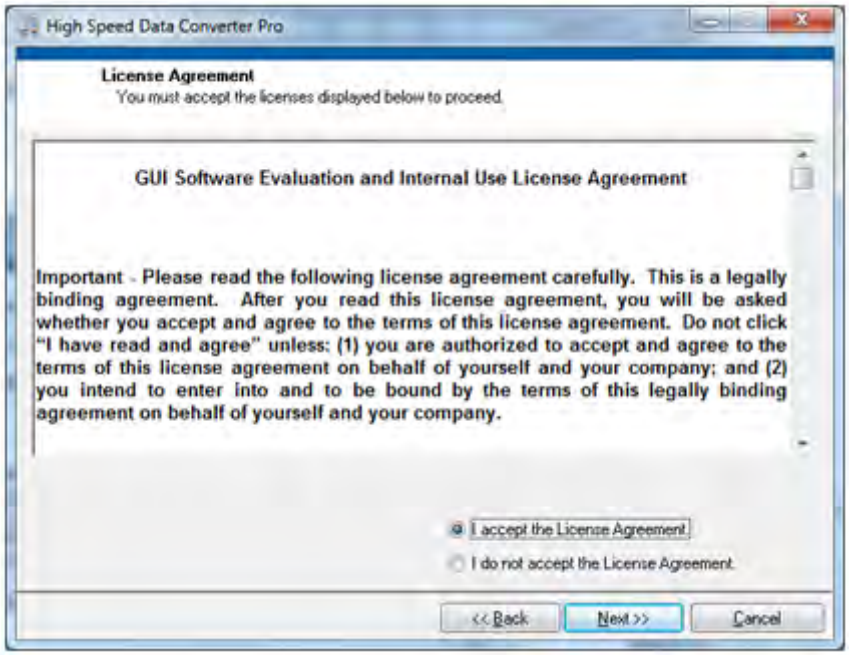


Figure 4. *HSDCpro* **Install (c)**

(b) Read the License Agreement from National Instruments and *I accept the License Agreement* and press the *Next* button as in Figure 5.

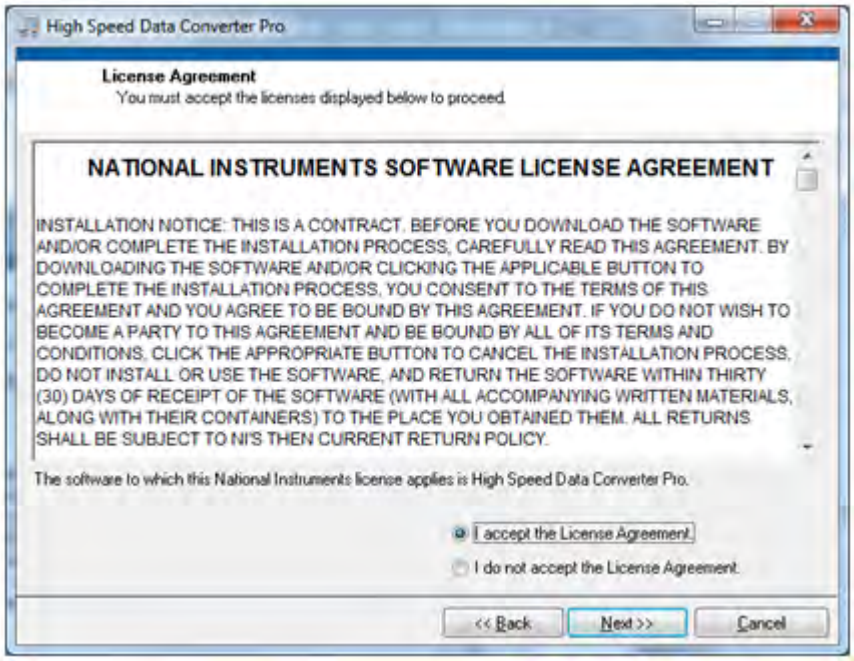


Figure 5. *HSDCpro* **Install (d)**

3. Press the *Next* button as in Figure 6.

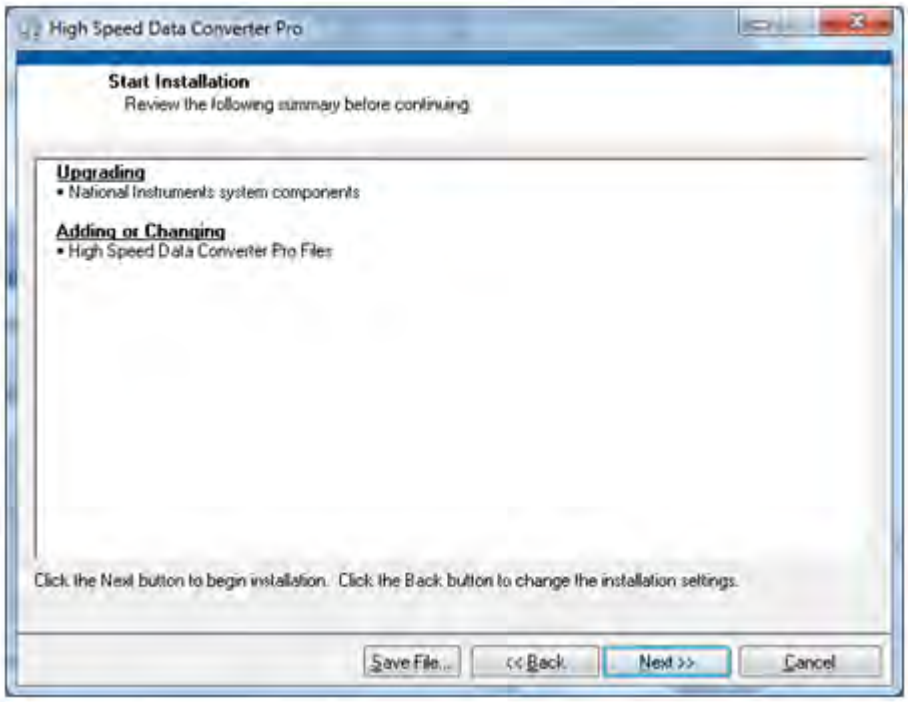


Figure 6. *HSDCpro* **Install (e)**

(d) The window in Figure 7 should appear, indicating that the installation is in progress.

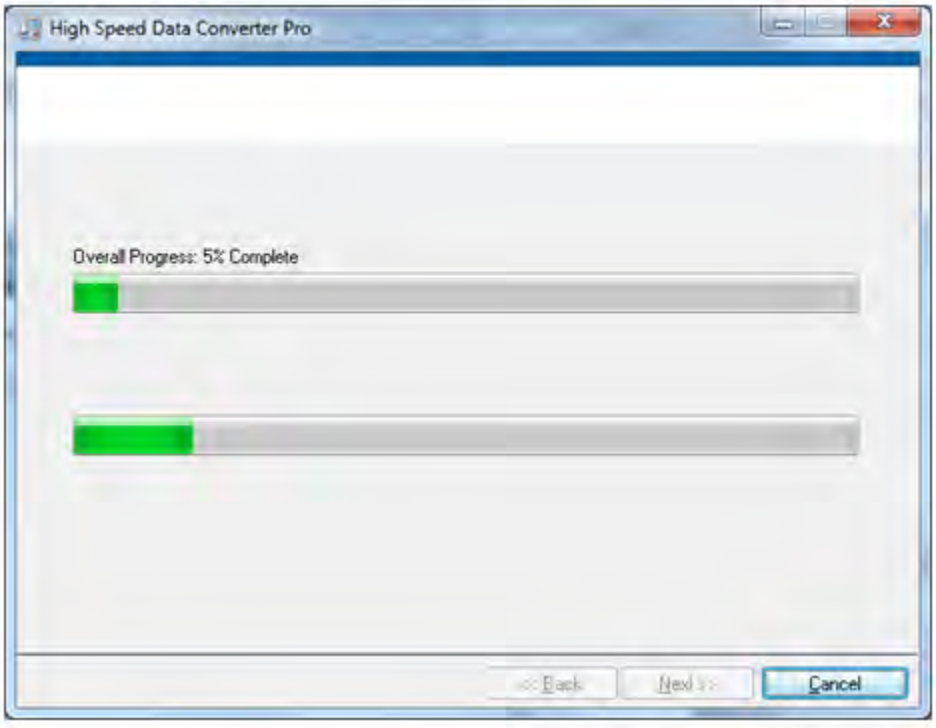


Figure 7. *HSDCpro* **Install (f)**

5. The window shown in Figure 8 appears, indicating *Installation Complete*. Press the *Next* button.

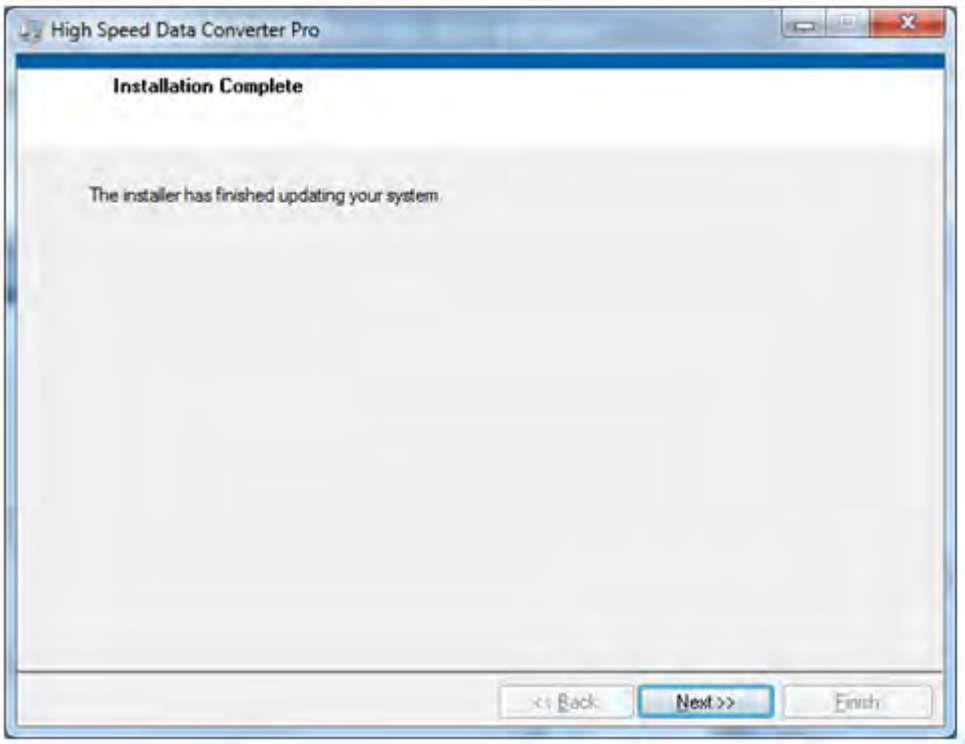


Figure 8. *HSDCpro* **Install (g)**

(f) The window in Figure 9 appears briefly to complete the process.

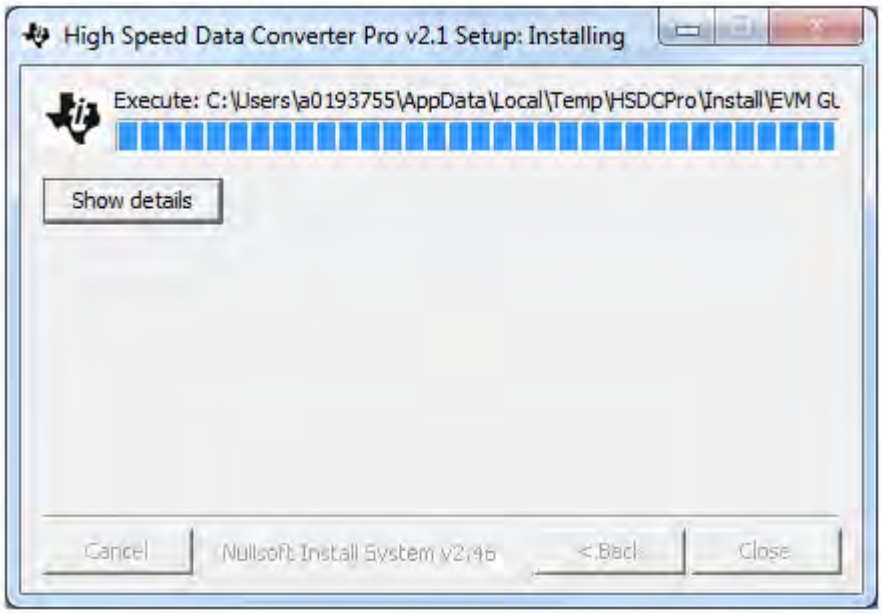


Figure 9. *HSDCpro* **Install (h)**

7. As shown in Figure 10, a computer restart might be requested depending on whether or not the PC already has the National Instruments' MCR installer. If requested, hit the *Restart* button to complete the installation.

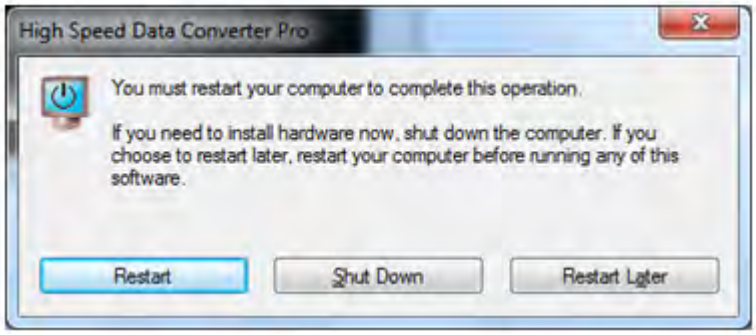


Figure 10. *HSDCpro* **Install (i)**

2.2 AFE5401-Q1 EVM GUI Installation

The AFE5401-Q1 GUI software can be obtained from TI's local supporting FAE. A zipped file containing the installer shall be provided.

(a) Unzip the folder and run the setup.exe file as administrator by right clicking on it and selecting *Run as administrator* as shown in Figure 11.

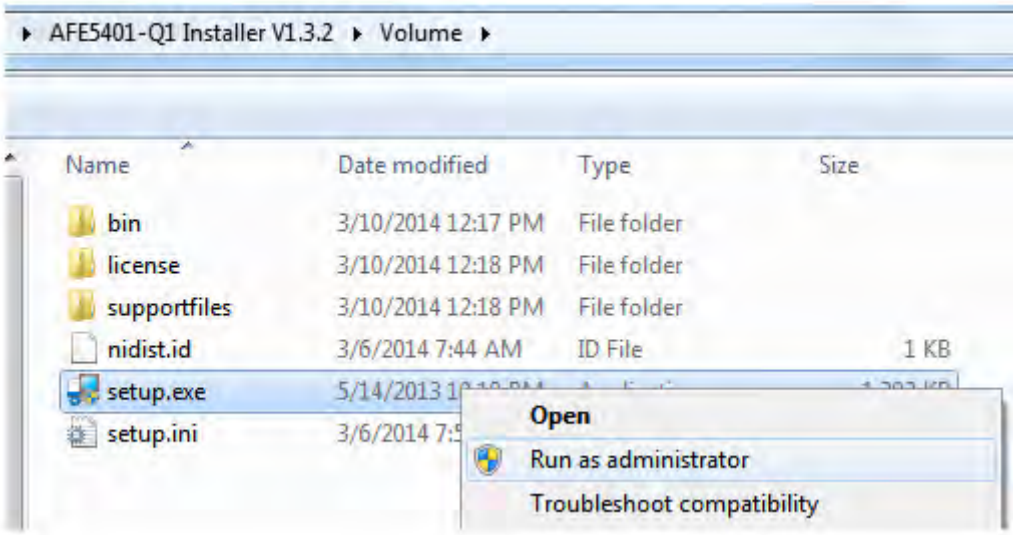


Figure 11. AFE5401-Q1 GUI Install (a)

2. Leave the destination directory as the default and press the *Next* button as shown in Figure 12.

NOTE: If a destination directory other than the default directory is used, the AFE5401-Q1 GUI is not found, therefore, it is not invoked as a plug-in tab to HSDCpro.

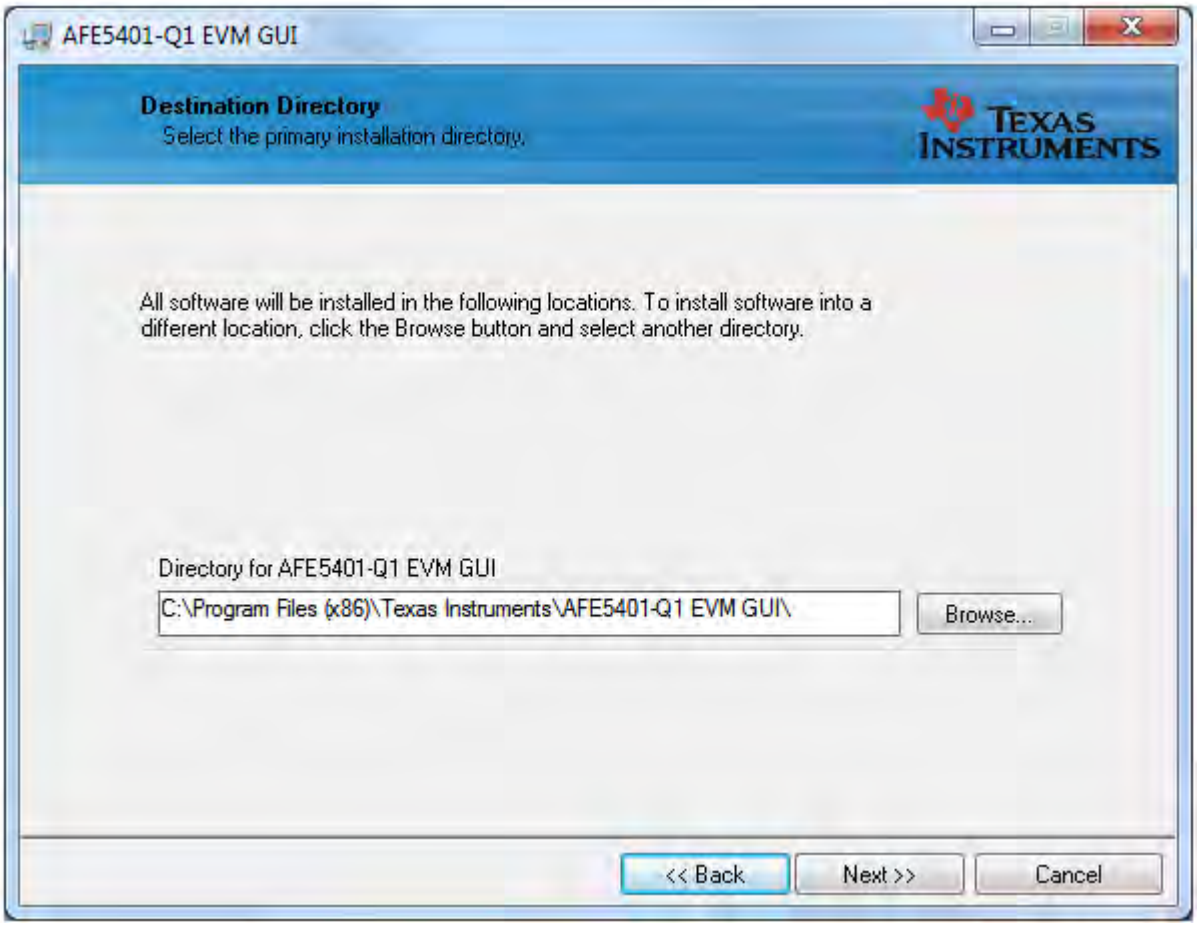


Figure 12. AFE5401-Q1 GUI Install (b)

3. Read the License Agreement from Texas Instruments, select the *I accept the License Agreement* button, and then press the *Next* button, as shown in Figure 13.

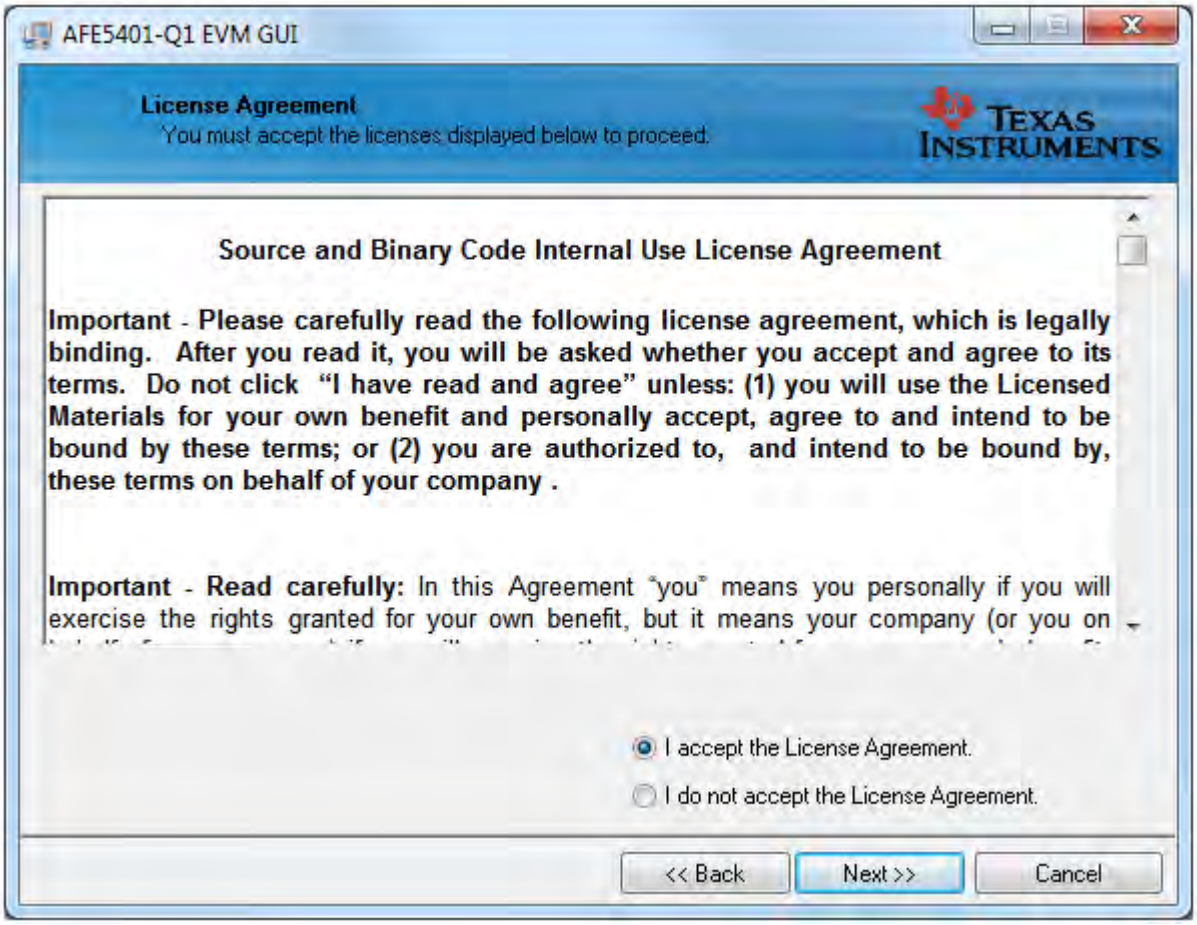


Figure 13. AFE5401-Q1 GUI Install (c)

4. Read the Texas Instruments Software Manifest, select the *I accept the License Agreement* check box, and then press the *Next* button, as shown in Figure 14.

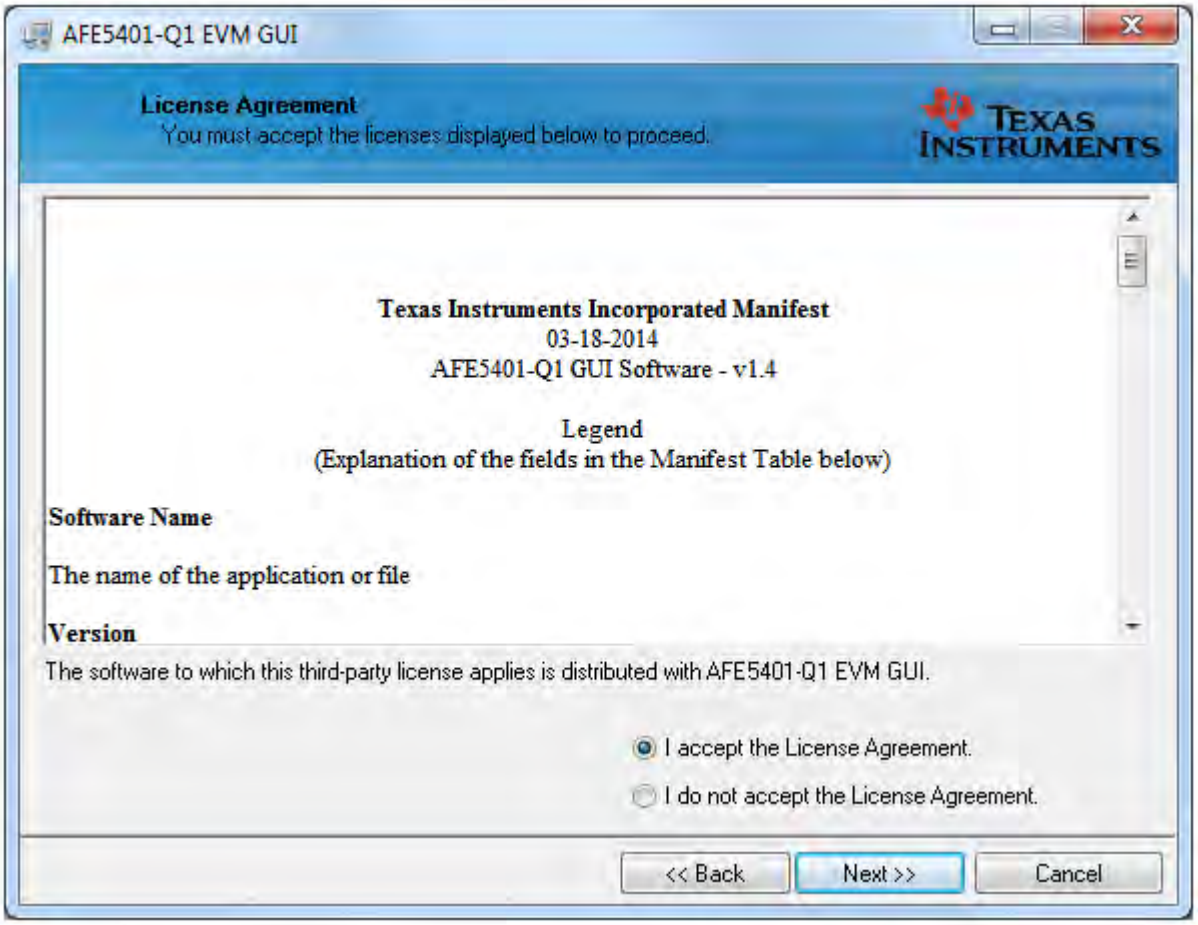


Figure 14. AFE5401-Q1 GUI Install (c)

5. Begin the installation by pressing the *Next* button, as illustrated in Figure 15.

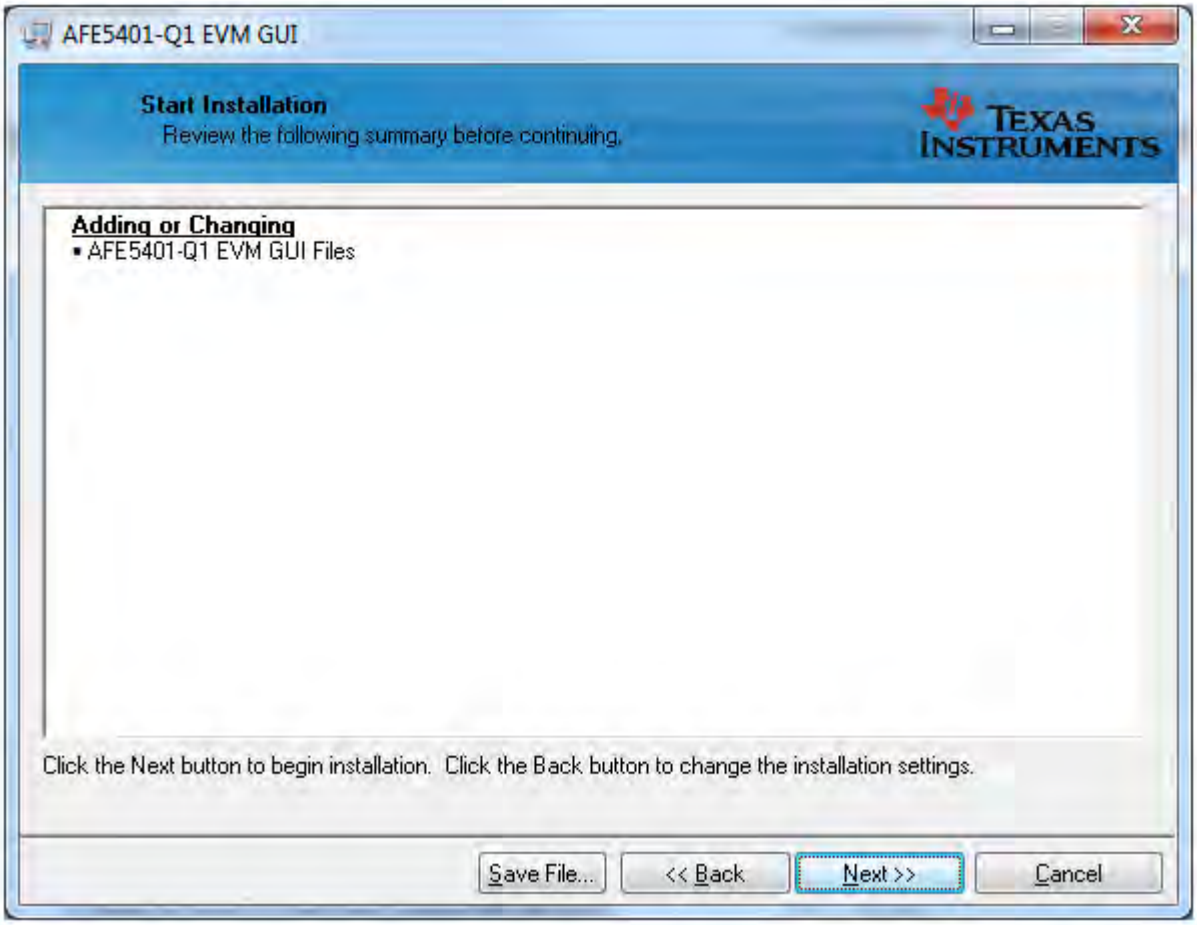


Figure 15. AFE5401-Q1 GUI Install (d)

6. The window shown in Figure 16 should appear showing that installation is in progress.

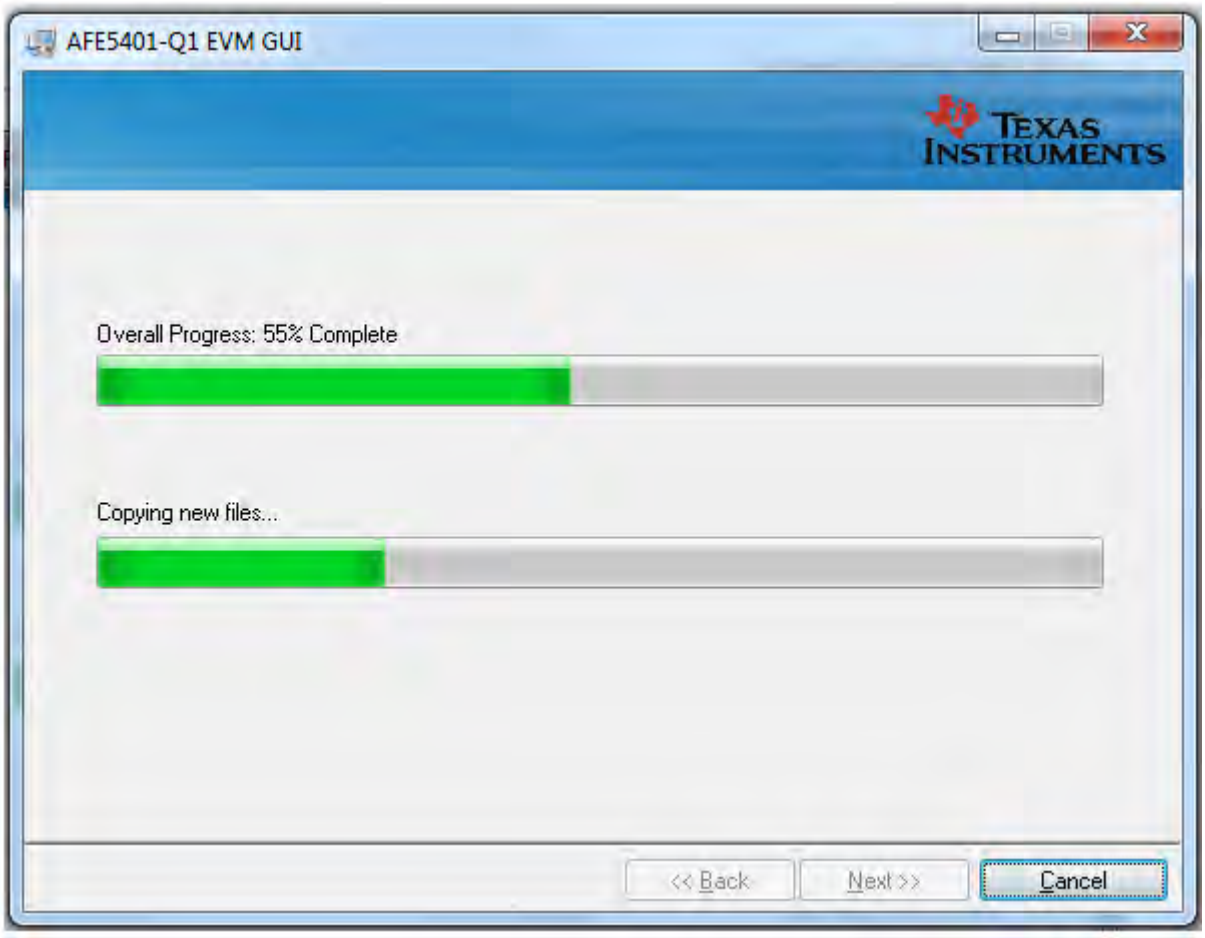


Figure 16. AFE5401-Q1 GUI Install (e)

7. Upon complete of installation, the window in Figure 17 appears. Press the *Finish* button to continue.

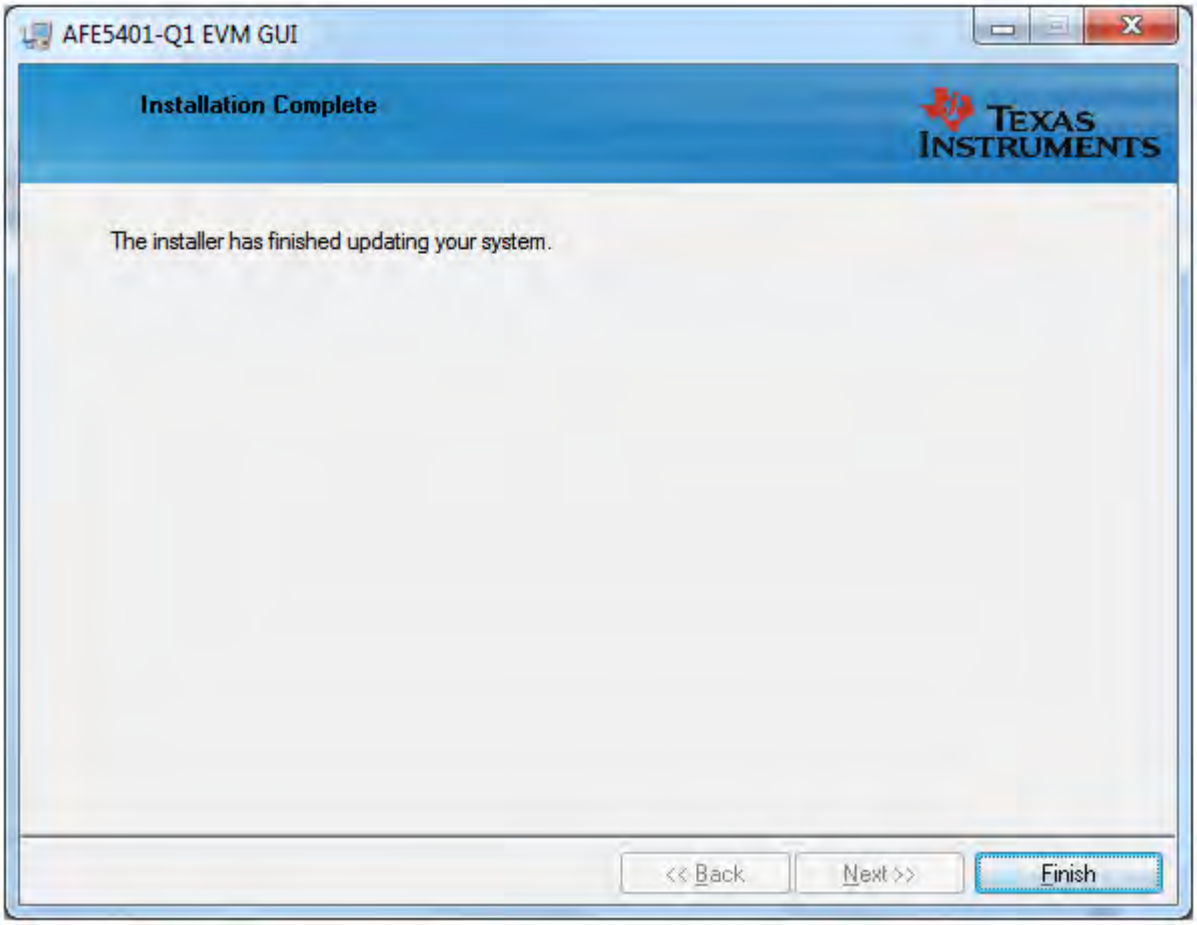


Figure 17. AFE5401-Q1 GUI Install (f)

3 AFE5401-Q1 EVM Header and Test Points

This section describes the functions of the headers on the EVM. It also provides a list of test points on the EVM that are useful for debug and general-use purposes.

3.1 AFE5401-Q1 EVM Header Configuration

The AFE5401-Q1 EVM is flexible in its configurability through the use of 2- and 3-pin headers. The default configuration of the EVM is set to facilitate initial testing by requiring no changes. Table 1 describes the purpose of all headers with the default position highlighted in red or yellow, while Figure 18 shows the default positions on the EVM.

Table 1. AFE5401-Q1 Header Configuration

Jumpe #	Default Config	Pin 1 Silkscreen	Pin 3 Silkscreen	Circuit	Description
JP22	Short pins 1-2	+1.8V_AVDD		Power Supply	Power Supply to DUT pins 19, 24, 62 (AVDD18)
JP28	Short pins 1-2	+3.3V_AVDD		Power Supply	Power Supply to DUT pin 18 (AVDD3)
JP20	Short pins 1-2	+1.8V_DVDD		Power Supply	Power Supply to DUT pins 28, 30, 51 (DVDD18)
JP26	Short pins 1-2	+3.3V		Power Supply	+3.3V Supply to J56
JP24	Short pins 1-2	+1.8V		Power Supply	+1.8V Supply to J56
J56	Short pins 1-2	+3.3V	+1.8V	Power Supply	Power supply to DUT pins 32, 33, 50 (DRVDD); selects output of (1) JP26, +3.3V or (2) output of JP24, +1.8V
JP30	Short pins 1-2	+3.3V_CLK		Power Supply	Power Supply to XTAL at U2
J33	Short pins 1-2	GND	+1.8V	Standby Circuit	Selects Voltage level of STDBY signal (1) GND or (3) +3.3V
J27	short pins 2-3	AUX	FTDI	Standby Circuit	Selects STDBY control source: (1) AUX determined by J29 or (3) Device GUI thru FTDI
J29	Short pins 1-2	AUX	DSP	Standby Circuit	Selects STDBY control source: (1) AUX determined by J32 or (3) CMOS connector P1
J32	Short pins 1-2	EVM	Vayu	Standby Circuit	Selects STDBY control source: (1) EVM determined by J33 or (3) Vayu connector J47
J34	Short pins 1-2	Vayu_Parity	Vayu_STDBY	Standby Circuit	For Vayu control only, selects (1) outputs parity from AFE5401-Q1 or (3) inputs STDBY from Vayu connector J47
J26	Short pins 1-2	Aux	FTDI	Trigger	Selects DUT Trigger signal source: (1) AUX determined by J28 or (3) Device GUI thru FTDI
J28	short pins 2-3	Aux	DSP	Trigger	Selects DUT Trigger signal source: (1) AUX determined by J31 or (3) CMOS connector P1
J31	Short pins 1-2	SMA	Vayu	Trigger	Selects DUT Trigger signal source: (1) SMA J30, EXT. TRIG or (3) Vayu connector J47
J41	Short pins 1-2	DSP	Vayu	Reset	Selects RESET control source when sma J36 is set to Aux (1) from DSP or (3) from Vayu
J36	short pins 2-3	Aux	FTDI	Reset	Selects DUT RESET signal source: (1) Aux determined by J41 or (3) Device GUI thru FTDI
J35	short pins 2-3	Aux	FTDI	Reset	Selects DUT SCLK signal source: (1) Aux determined by J40 (3) Device GUI thru FTDI
J40	short pins 1-2	DSP	Vayu	SPI	Selects SCLK signal source: (1) CMOS connector P1 (3) Vayu connector J47
J39	short pins 2-3	Aux	FTDI	SPI	Selects DUT SDOUT signal path: (1) Aux determined by J44 (3) Device GUI thru FTDI
J44	short pins 1-2	DSP	Vayu	SPI	Selects SDOUT signal path: (1) CMOS connector P1 (3) Vayu connector J47

Table 1. AFE5401-Q1 Header Configuration (continued)

Jumpe #	Default Config	Pin 1 Silkscreen	Pin 3 Silkscreen	Circuit	Description
J38	short pins 2-3	Aux	FTDI	SPI	Selects DUT SEN signal source: (1) Aux determined by J43 (3) Device GUI thru FTDI
J43	short pins 1-2	DSP	Vayu	SPI	Selects SEN signal source: (1) CMOS connector P1 (3) Vayu connector J47
J37	short pins 2-3	Aux	FTDI	SPI	Selects DUT SDA signal source: (1) Aux determined by J42 (3) Device GUI thru FTDI
J42	short pins 1-2	DSP	Vayu	SPI	Selects SDA signal source: (1) CMOS connector P1 (3) Vayu connector J47
J57	short pins 2-3	DSP_OE	GND	SPI	Selects enablebar source for flip flop at U4 between (1)FPGA via P1 or (2) GND
J4	short pins 2-3	XFMR	XTAL	CLOCK	Power Supply for on-board 25MHz XTAL oscillator
J5	short pins 2-3	XFMR	XTAL	CLOCK	Selects clock input configuration to (1) differential signal input to SMA J3, CLK_IN, thru transformer or (3) single-ended on-board XTAL oscillator
J8	short pins 2-3	XFMR	XTAL	CLOCK	Selects clock input configuration to (1) differential signal input to SMA J3, CLK_IN, thru transformer or (3) single-ended on-board XTAL oscillator

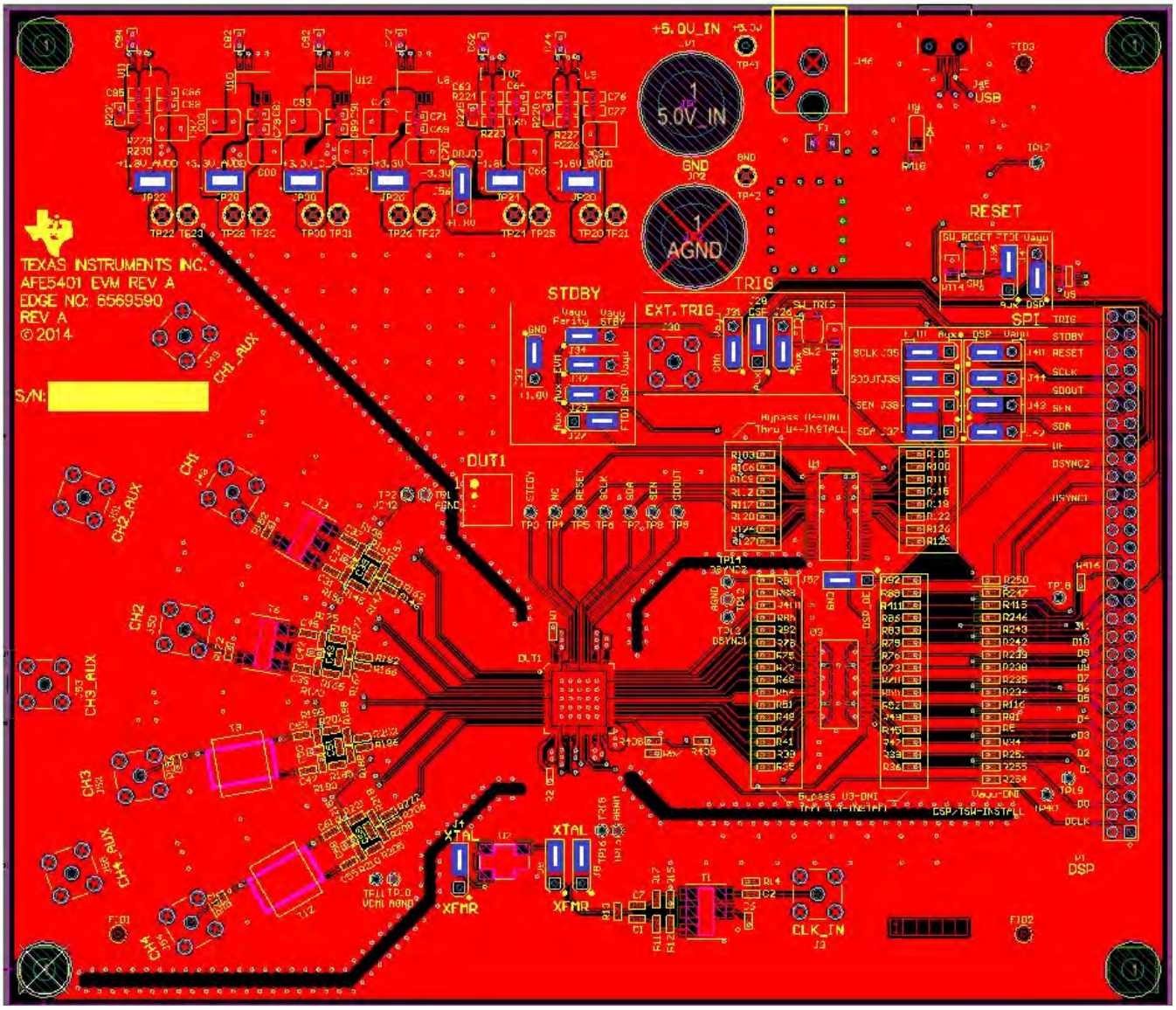


Figure 18. AFE5401-Q1 EVM Default Header Configuration

3.2 AFE5401-Q1 EVM Test Points

Table 2 lists all the test points on the AFE5401-Q1-Q1 EVM and the purpose of each test point.

Table 2. AFE5401-Q1 Header Configuration

Testpoint	Silkscreen	Circuit	Description
TP2	VCM2	Analog Inputs VCM	Common Mode Voltage Node for Analog Inputs 1-2
TP1	AGND	Analog Inputs VCM	Analog Ground
TP11	VCM1	Analog Inputs VCM	Common Mode Voltage Node for Analog Inputs 3-4
TP10	AGND	Analog Inputs VCM	Analog Ground
TP3	STDBY	Digital Input	Input to STBY pin 59
TP4	NC	n/a	
TP5	RESET	Digital Input	Input to RESET pin 57

Table 2. AFE5401-Q1 Header Configuration (continued)

Testpoint	Silkscreen	Circuit	Description
TP6	SCLK	Digital Input	Input to SCLK pin 56
TP7	SDA	Digital Input	Input to SDATA pin 55
TP8	SEN	Digital Input	Input to SEN pin 55
TP9	SDOUT	Digital Output	Input to SDOUT pin 53
TP14	DSYNC2	Frame Clock	Output from DSYCN2 pin 27
TP12	AGND	Frame Clock	Analog Ground
TP13	DSYNC1	Frame Clock	Output from DSYCN2 pin 26
TP16	TRIG	Frame Clock	Input to TRIG pin 25
TP15	AGND	Frame Clock	Analog Ground
TP21	REFOUT	CDC Cock Device	Output from REFOUT pin 29 of CDC device
TP17	n/a	not used	
TP18	n/a	not used	
TP19	n/a	not used	
TP20	n/a	not used	

4 Setup for Testing AFE5401-Q1 EVM

This section outlines (1) the external connections required to test the AFE5401-Q1 EVM using the CMOS interface and (2) how to set up the GUIs for testing.

Only the minimal GUI software settings required to achieve the previously mentioned tests are described. For a detailed explanation of the AFE5401-Q1 GUI software and all its features, please see Section 6. For a detailed explanation of the *High Speed Data Converter Pro* GUI software, please consult the GUI User's Guide, (SLWU087). The TSW140x EVM User's Guide (SLWU079C) is available on www.ti.com.

4.1 External Connections

Figure 19 shows the connections for proper hardware setup (*Note: Testing the parallel CMOS interface between the AFE5401-Q1 EVM and the TSW1400 EVM can be performed using a RAMP function generated within the AFE5401-Q1 device in lieu of the signal source listed in item 7. Also, an on-board 25-MHz crystal oscillator (XTAL) can provide the ADC sampling clock in lieu of the signal source listed in item 6. This configuration is only recommended for testing the RAMP function as low phase noise filtered signal sources must be provided to both the ADC clock input and the ADC analog inputs for measuring device performance*).

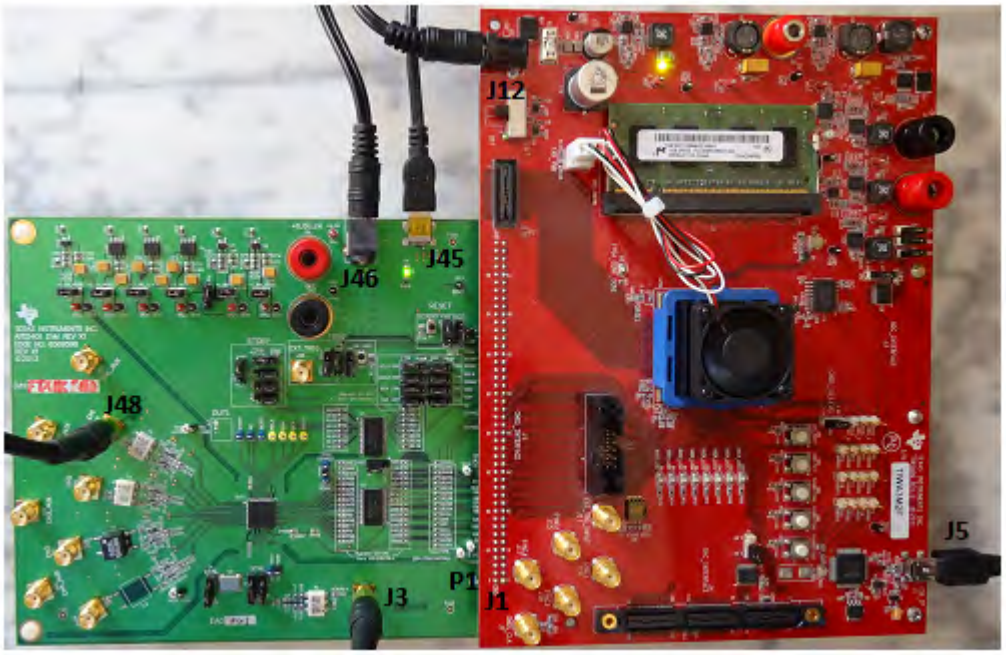


Figure 19. TSW1400 and AFE5401-Q1 Setup

1. Mate the TSW1400 EVM at connector **J1 (CMOS_INTERFACE)** to the AFE5401-Q1 EVM at connector **P1 (DSP)** through the CMOS header connector. The connection should be right justified looking from the CMOS outputs of the AFE5401-Q1 to the TSW1400 EVM as shown in Figure 20.

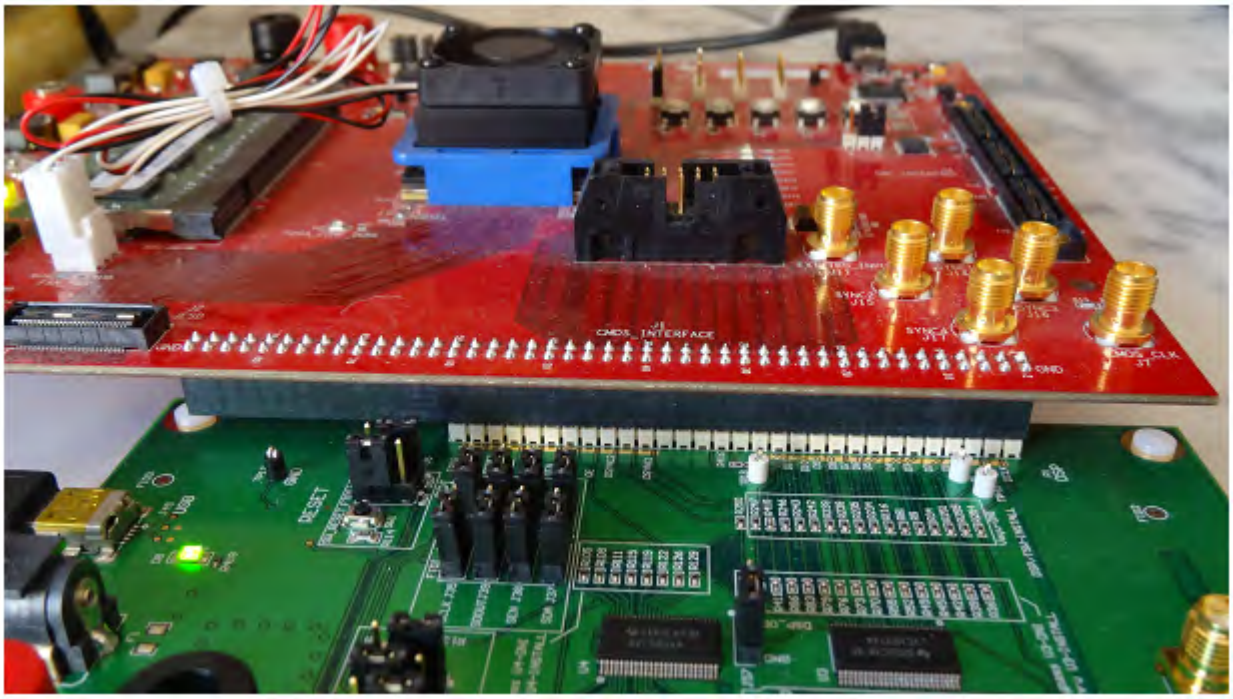


Figure 20. TSW1400 Mated to AFE5401-Q1

2. Connect the DC +5-V output of the provided AC-to-DC power supply to **J12 (+5V_IN)** of the TSW1400 EVM and the input of the power supply cable to a 110-230 VAC source.
3. Connect the DC +5 V output of the provided AC-to-DC power supply to connector **JP46** of the

AFE5401-Q1 EVM.

4. Connect the USB cable from the PC to **J45** (**USB**) of AFE5401-Q1 EVM.
5. Connect the USB cable from the PC to **J5** (**USB_IF**) of the TSW1400 EVM.
   [*NOTE: it is recommended that the PC USB port be able to support USB2.0. If unsure, always chose the USB ports at the back of the PC chassis over ones located on the front or sides.*]
6. Supply an ADC clock signal through a bandpass filter to sma **J3** (**CLK_IN**) of the AFE5401-Q1 EVM (that is, +5 dBm, 25 MHz).
   [*NOTE: Not required if only testing the CMOS interface with a RAMP test pattern or for non-coherent sampling as 25MHz XTAL clock provided on the EVM.*]
7. Supply an analog input signal through a bandpass filter to sma **J48** (**CH1**) of the AFE5401-Q1 EVM (that is, +4 dBm, 3.5 MHz).
   [*NOTE: Not required if only testing the CMOS interface with a test pattern.*]

4.2 TSW1400 and AFE5401-Q1 GUI Software Setups

With the setup outlined in Figure 19 established, launch the *High Speed Data Converter Pro* GUI. The GUI should automatically detect the serial number of the TSW1400 EVM connected as shown in Figure 21. Click on *OK*.

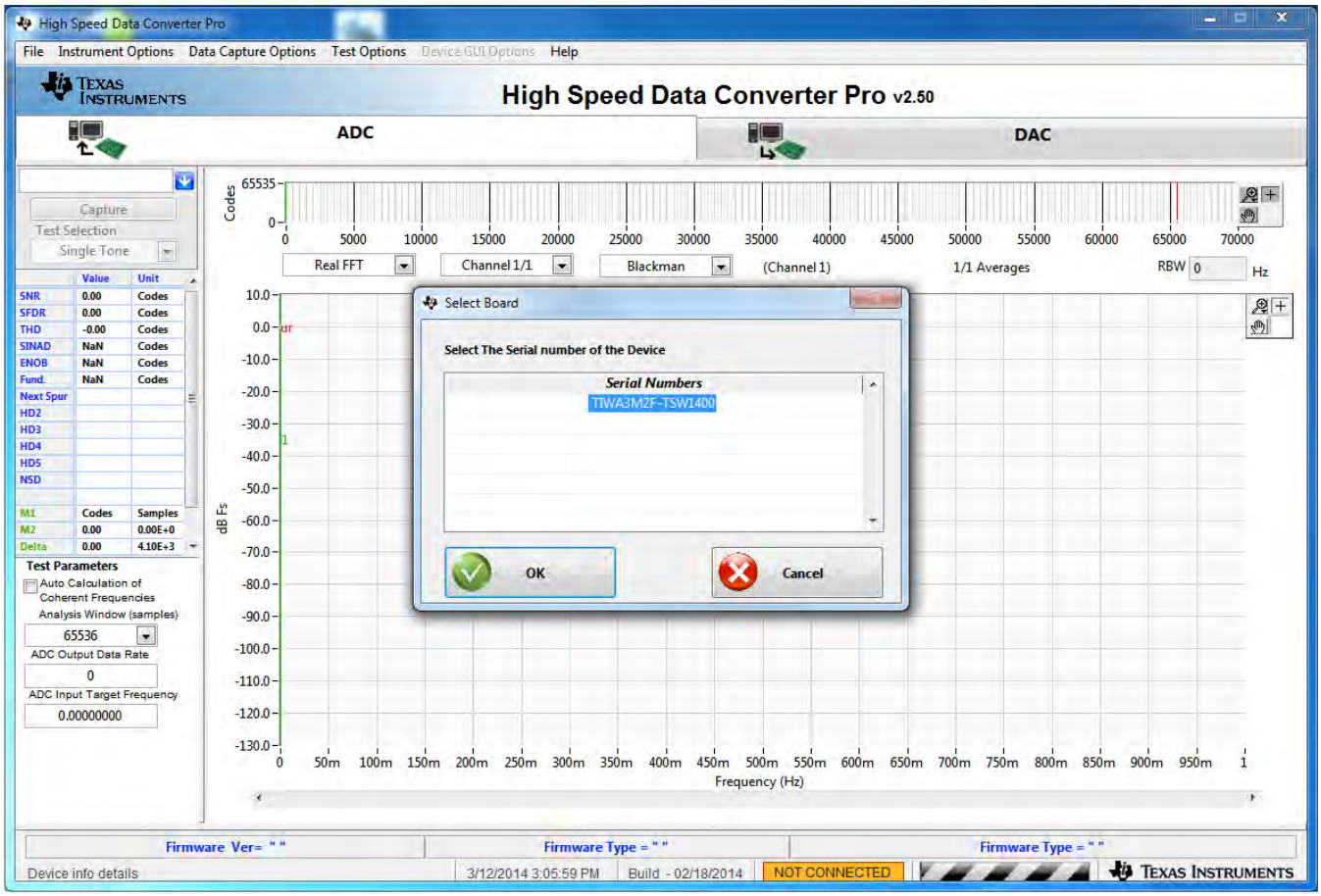


Figure 21. TSW1400 GUI Setup (a)

Figure 22 shows the message that appears. Click *OK*.

Figure 22. TSW1400 GUI Setup (b)

If instead, the message in Figure 23 appears, it indicates that the USB connection to the TSW1400 EVM is not present. Click *OK*, then establish a USB connection and repeat step 1.

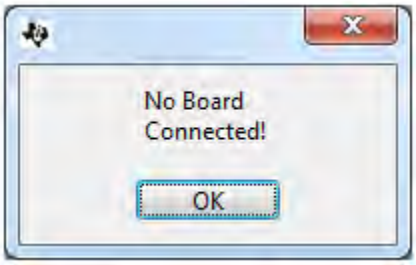


Figure 23. TSW1400 GUI Setup (c)

Select a device by clicking on the blue arrow in the upper left corner of the *HSDCpro* GUI. Scroll down and select *AFE5401-Q1* as shown in Figure 24.

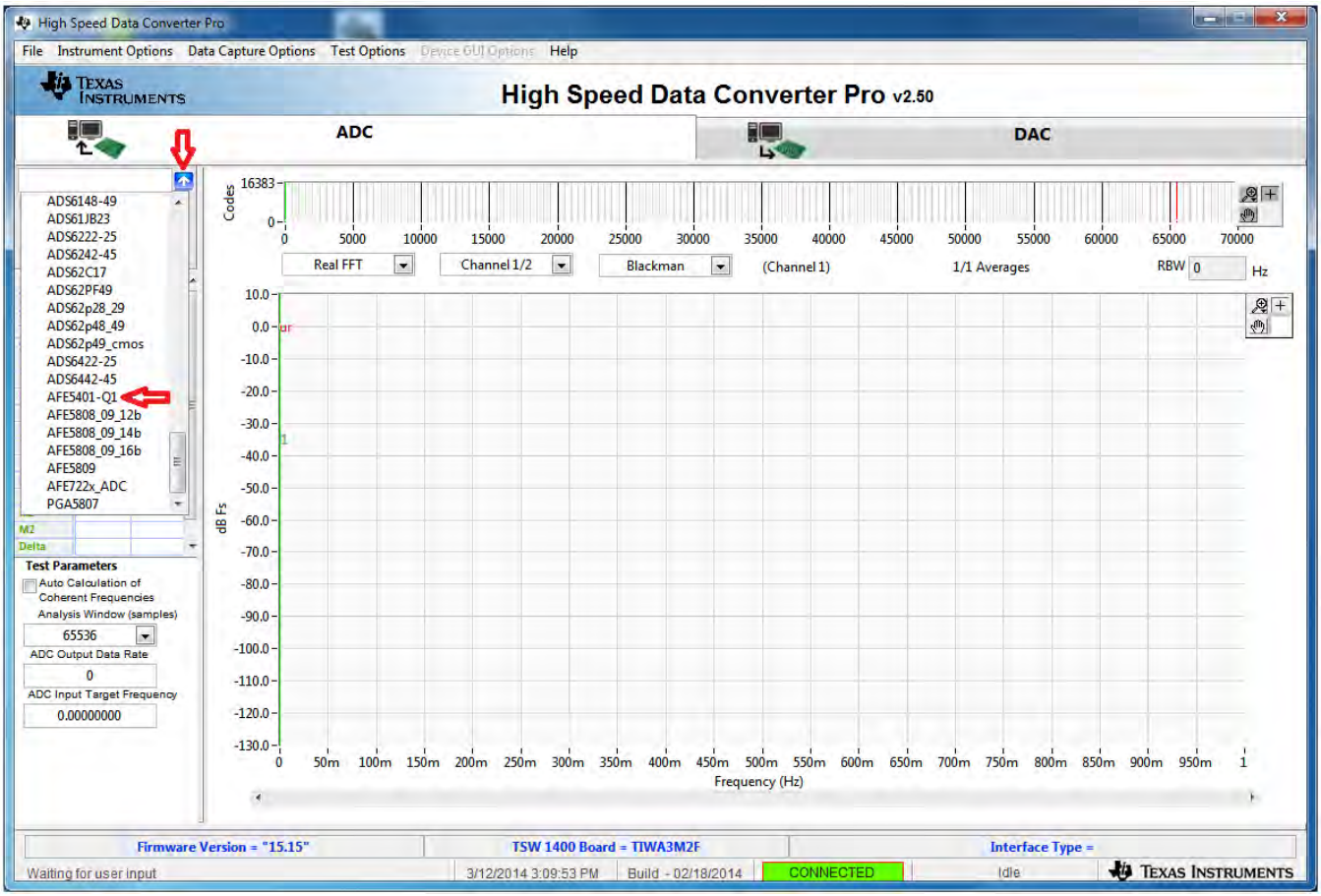


Figure 24. TSW1400 GUI Setup (d)

Click the *Yes* button to update the ADC firmware on the TSW1400 FPGA as depicted in Figure 25.

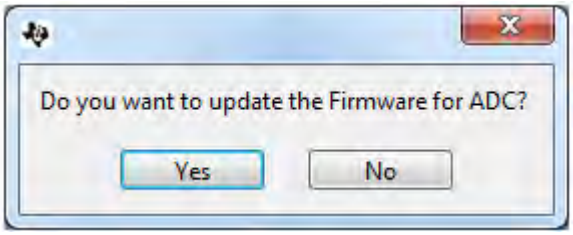


Figure 25. TSW1400 GUI Setup (e)

While the firmware is being loaded into the TSW1400 FPGA, the menu shown in Figure 26 appears.

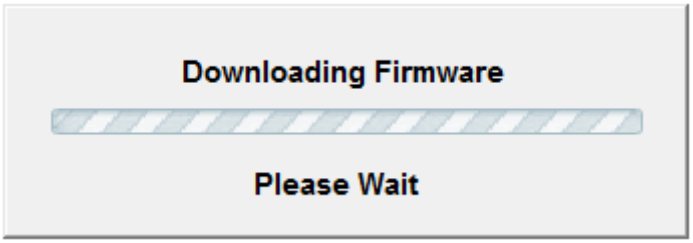


Figure 26. TSW1400 GUI Setup (f)

Once loaded, the plug-in AFE5401-Q1 GUI appears as a new tab within the *HSDCpro* GUI, as shown in Figure 27.

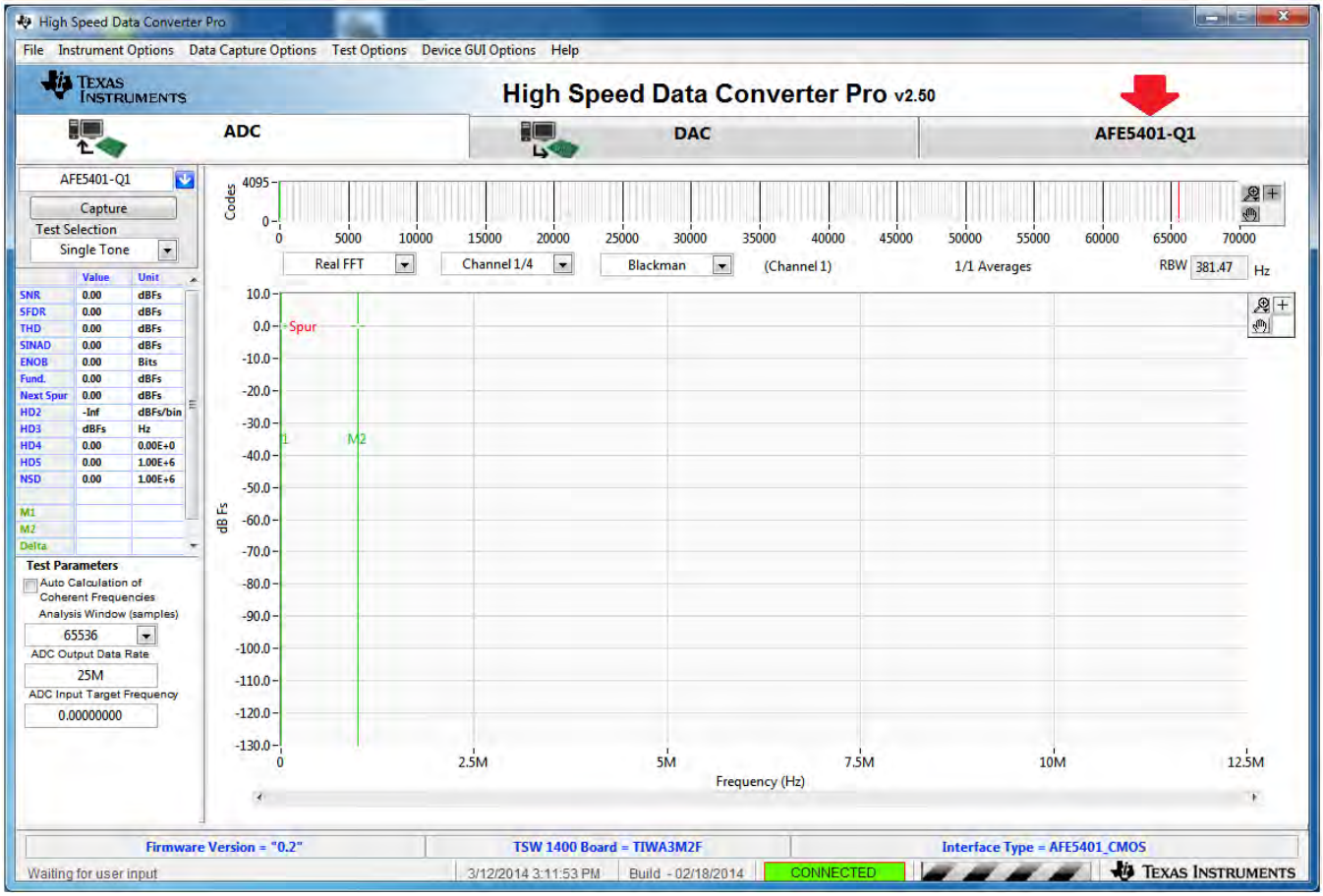


Figure 27. AFE5401-Q1 Plug-in GUI Setup (g)

Click on the tab *AFE5401-Q1 GUII* to view the GUI software for the AFE5401-Q1. The GUI consists of four tabs: *Read Me First*, *TOP LEVEL SETTINGS*, *DIAGNOSTICS & TEST MODES*, and *Low Level View*. The *Read Me First* tab is presented initially as shown in Figure 28.

The easiest way to configure the AFE5401-Q1 EVM for testing is by using the pre-loaded configurations provided with the AFE5401-Q1 GUI software installation. The bottom of the *Read Me First* tab provides a way to load these configurations. Figure 28 shows there are 12 configurations, each with the possibility to capture *Normal ADC Data* (sampling signal at the analog inputs) or a *Full Scale Ramp* test pattern generated internal to the AFE5401-Q1.

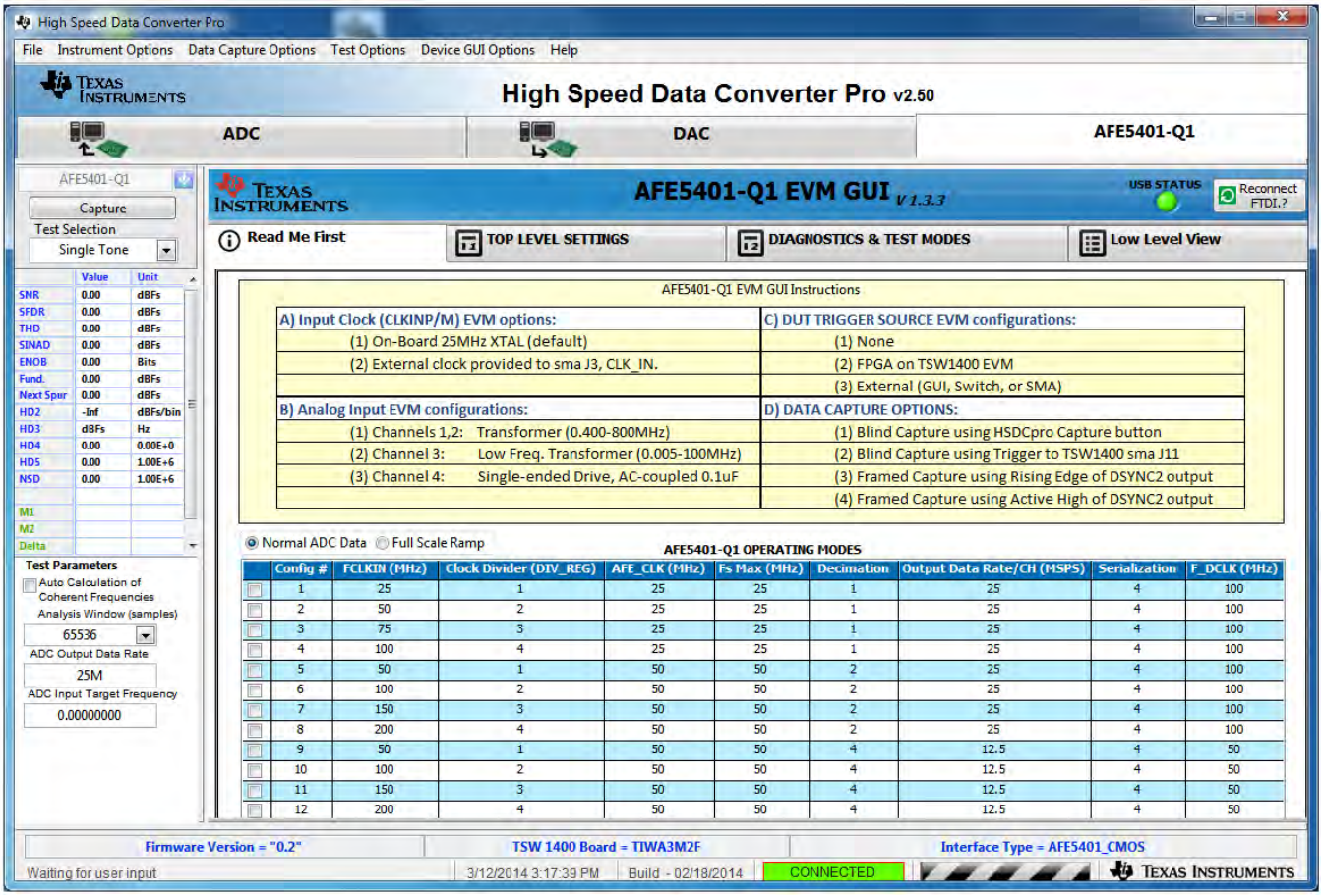


Figure 28. AFE5401-Q1 Plug-in GUI Setup (h)

5 Capturing a RAMP Test Pattern

Program the AFE5401-Q1 device for a *Full Scale Ramp* test pattern by selecting the *Full Scale Ramp* radio button on the *Read Me First* tab as shown in Figure 29.

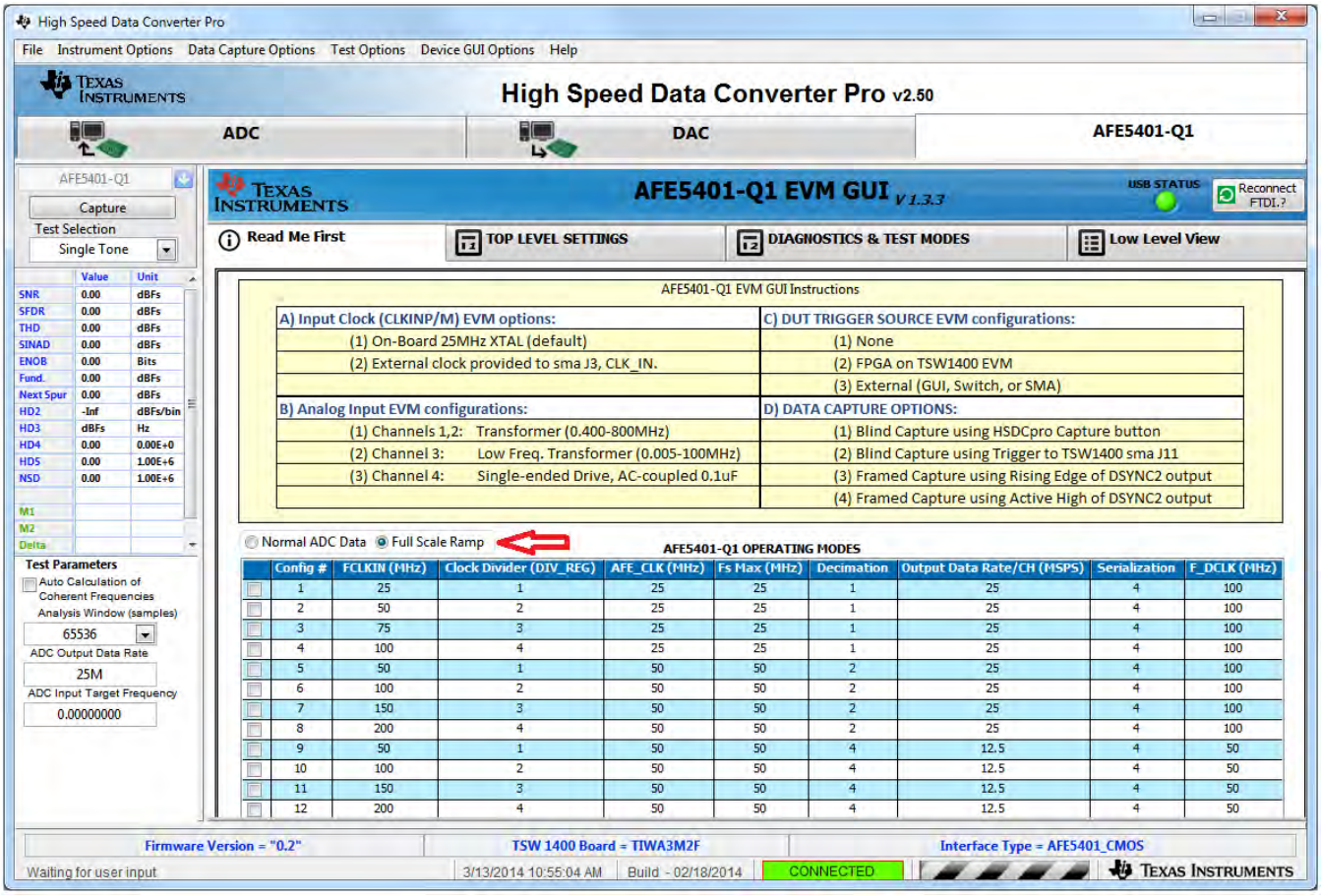


Figure 29. AFE5401-Q1 Ramp Capture (a)

The message in Figure 30 indicates one of the twelve pre-defined configurations described in the table must be selected. Click *OK* and select the desired configuration.

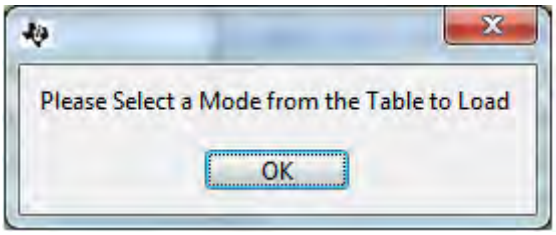


Figure 30. AFE5401-Q1 Ramp Capture (b)

If the on-board 25-MHz crystal oscillator is being utilized (default jumper configuration), the config # 1 is the only viable option as the required FCLKIN is 25 MHz as described in the table.
[*NOTE: To use configs 2-12, move jumpers **J4**, **J5**, and **J8** from the **XTAL** position to the **XFMR** position and provide the appropriate clock frequency to sma **J3**, **CLK_IN**.*]

For this example, *Config #1* is selected as shown in Figure 31.

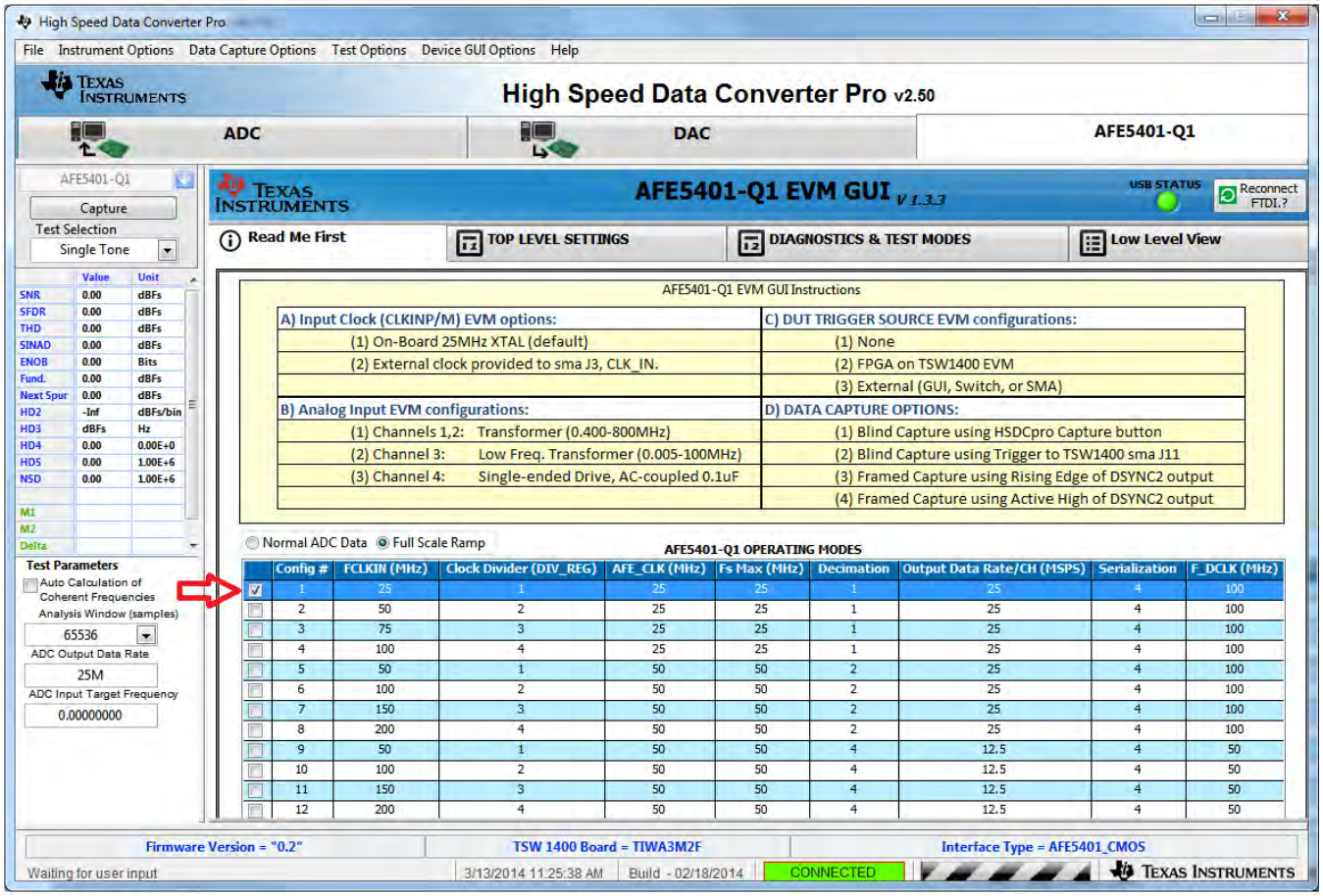


Figure 31. AFE5401-Q1 Ramp Capture (c)

Upon selecting a configuration, the message in Figure 32 appears while the EVM is being configured.

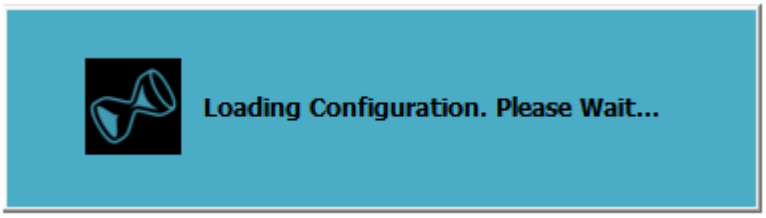


Figure 32. AFE5401-Q1 Ramp Capture (d)

Perform the following steps shown in Figure 33 to capture a Full Scale RAMP test pattern:

(a) Press the **ADC** tab of the GUI

(b) Select ***Codes***

(c) Press the ***Capture*** button

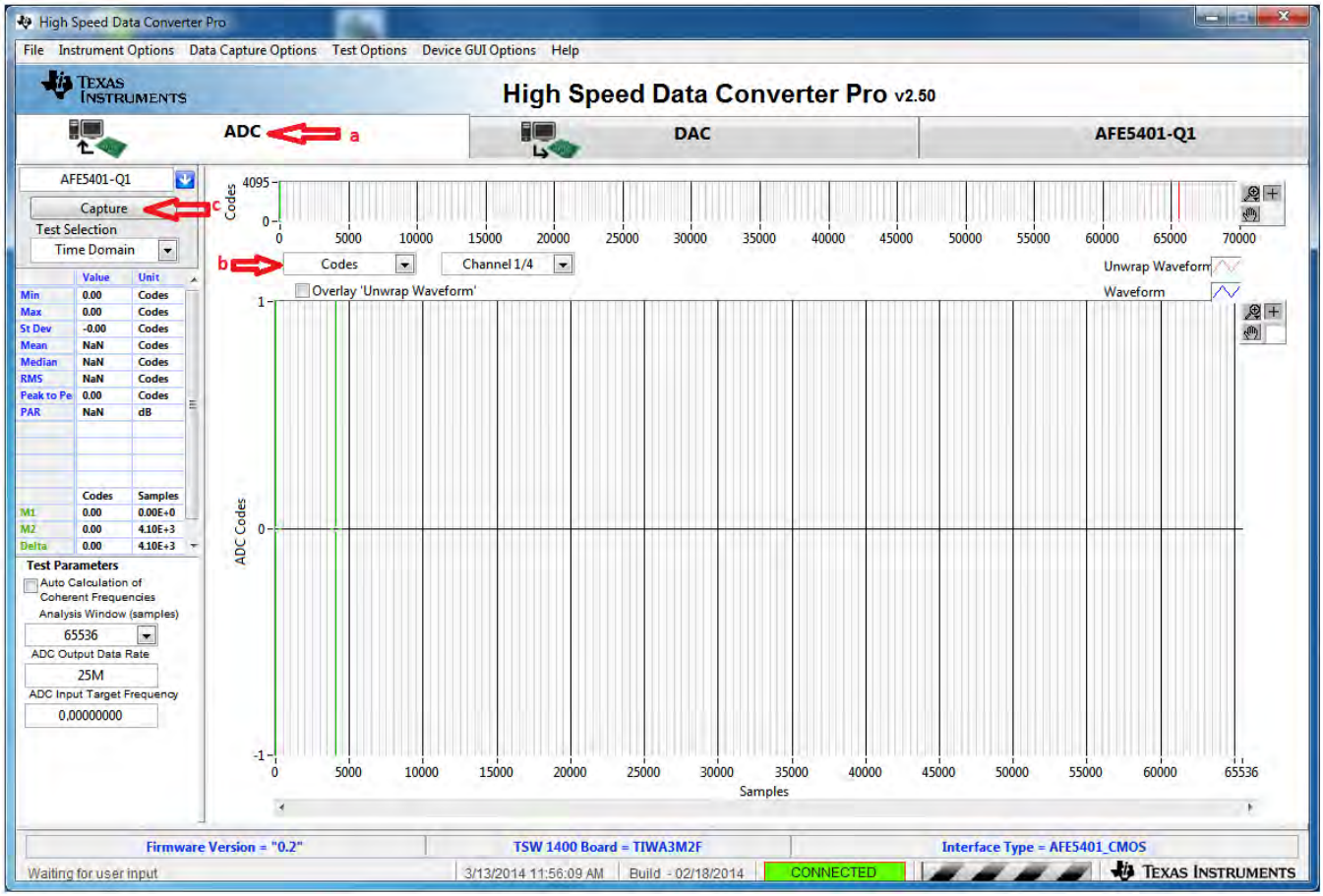


Figure 33. AFE5401-Q1 Ramp Capture (e)

A sawtooth RAMP waveform (Figure 34) is captured.

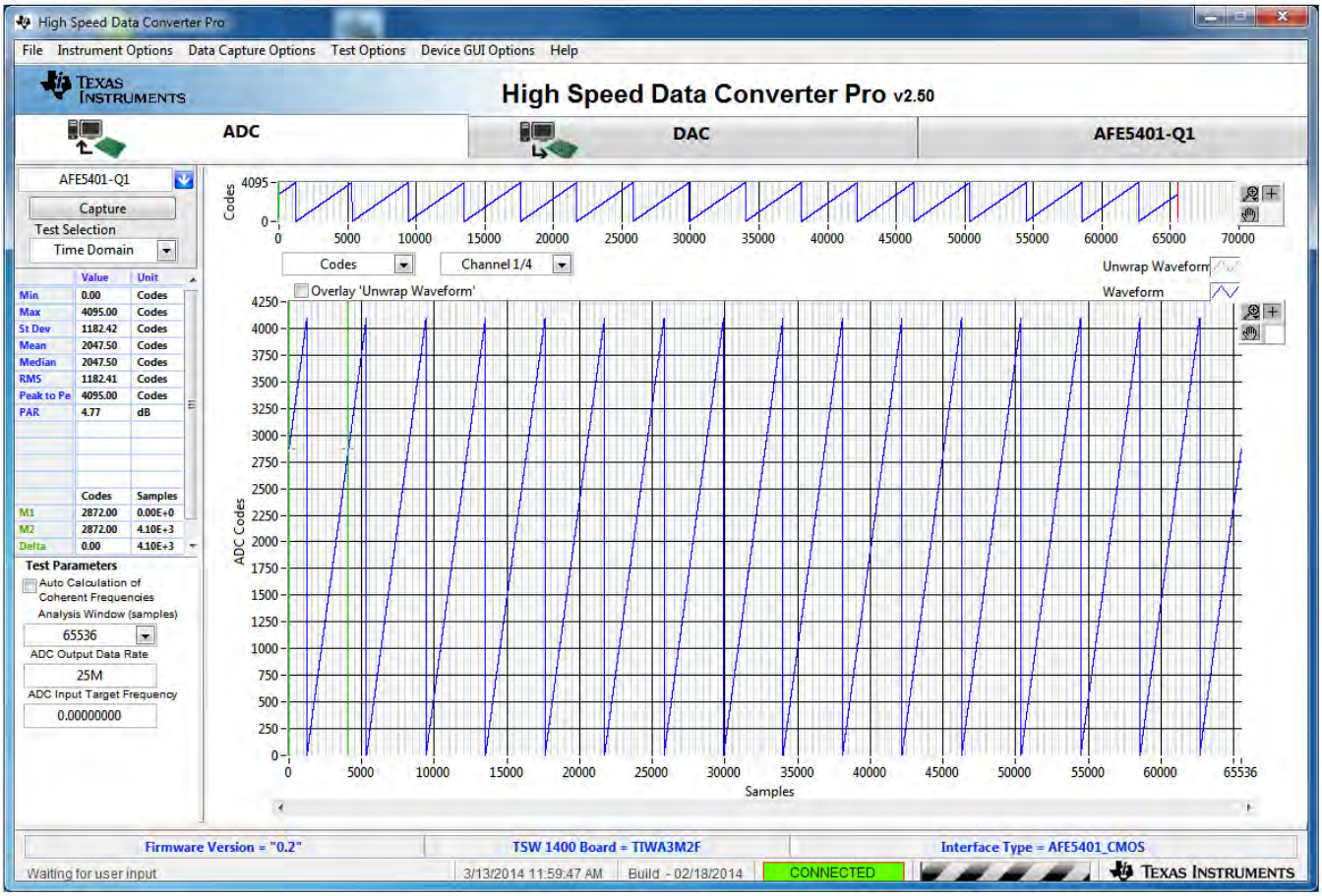


Figure 34. AFE5401-Q1 Ramp Capture (f)

By default, *Channel 1/4* is the first channel displayed in *HSDCpro*. Use the drop-down menu shown in Figure 35 to view any one of four channels and confirm that a sawtooth waveform has been captured. Also confirm, in the menu to the left side, that the Min code is 0 and the Max code is 4095, corresponding to a 12-bit ADC.

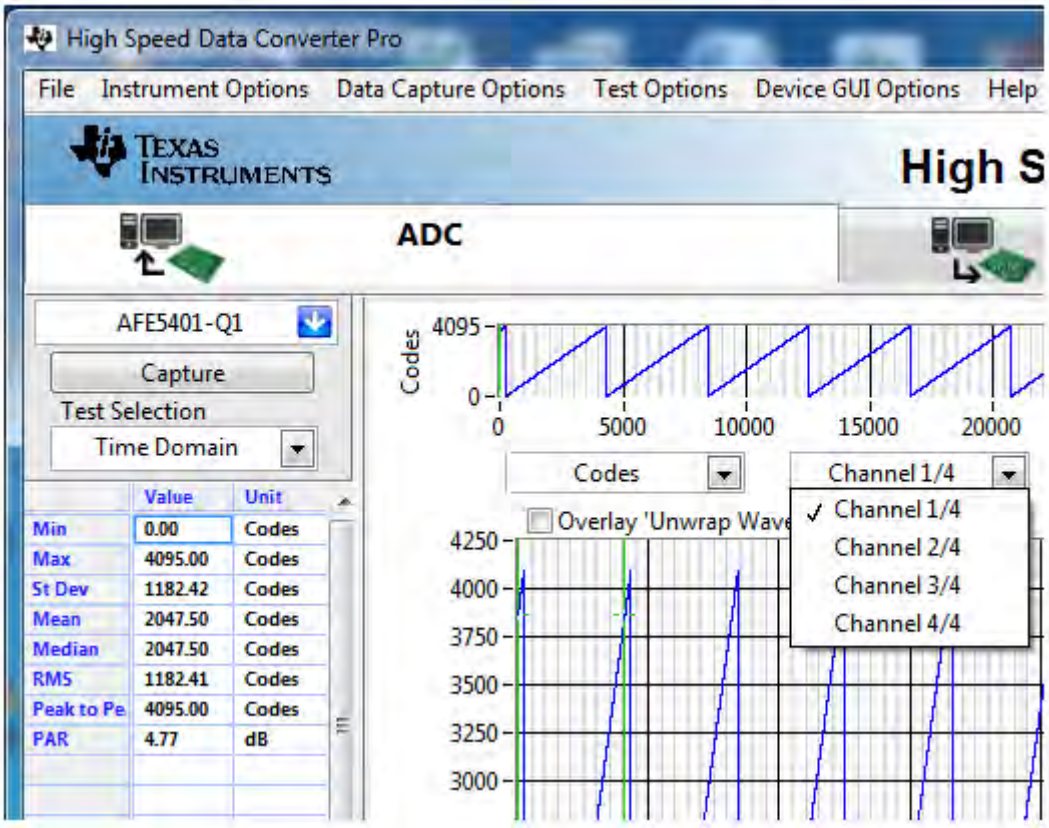


Figure 35. AFE5401-Q1 Ramp Capture (g)

Zooming into the waveform, as shown in Figure 36, is recommended to ensure that the RAMP waveform increments one ADC code for each subsequent sample (when decimation by 1 is selected).

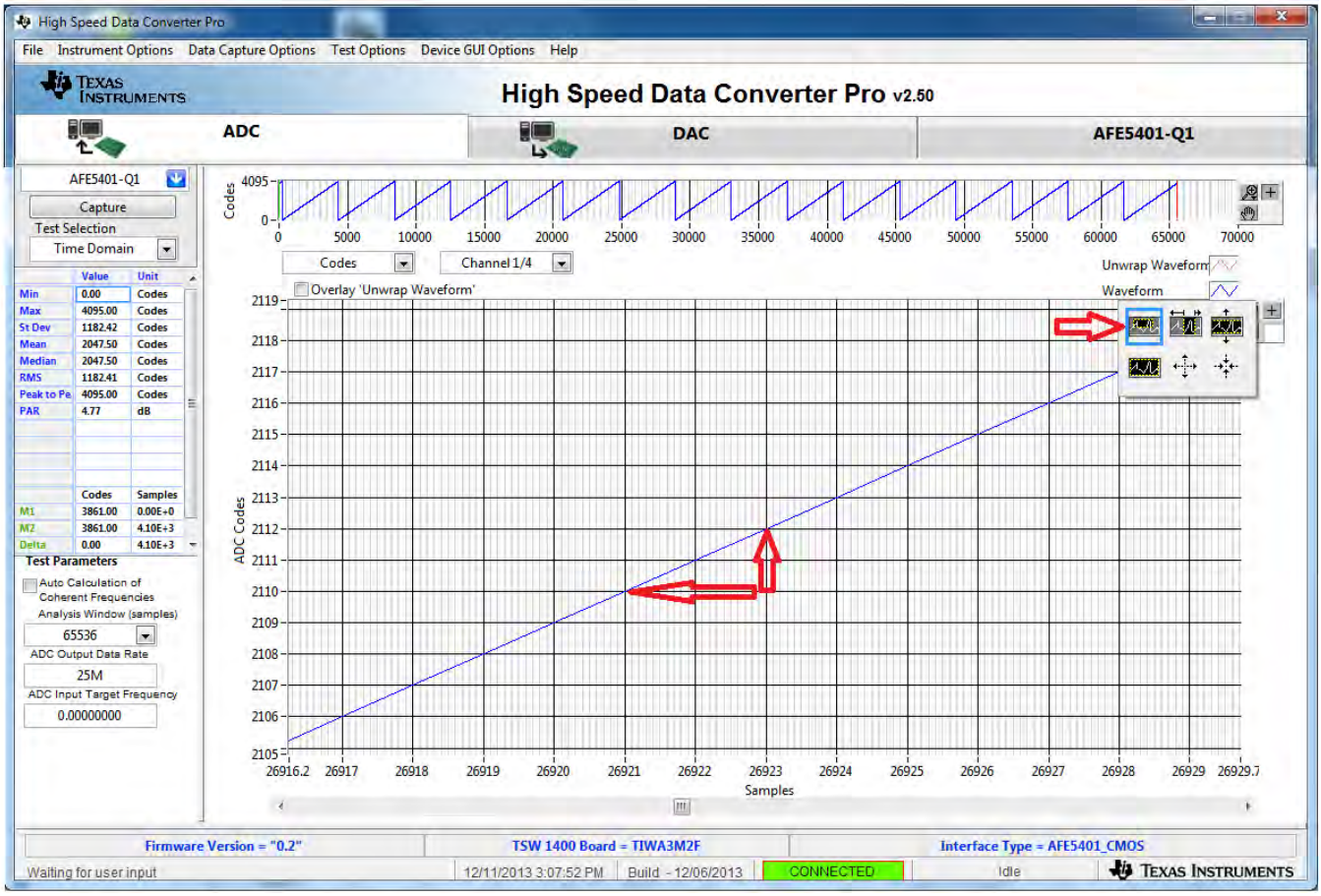


Figure 36. AFE5401-Q1 Ramp Capture (h)

6 Capturing a Sinusoidal Input

Program the AFE5401-Q1 device to sample a sinusoidal input by selecting the *Normal ADC Data* radio button on the *Read Me First* tab as shown in Figure 37.

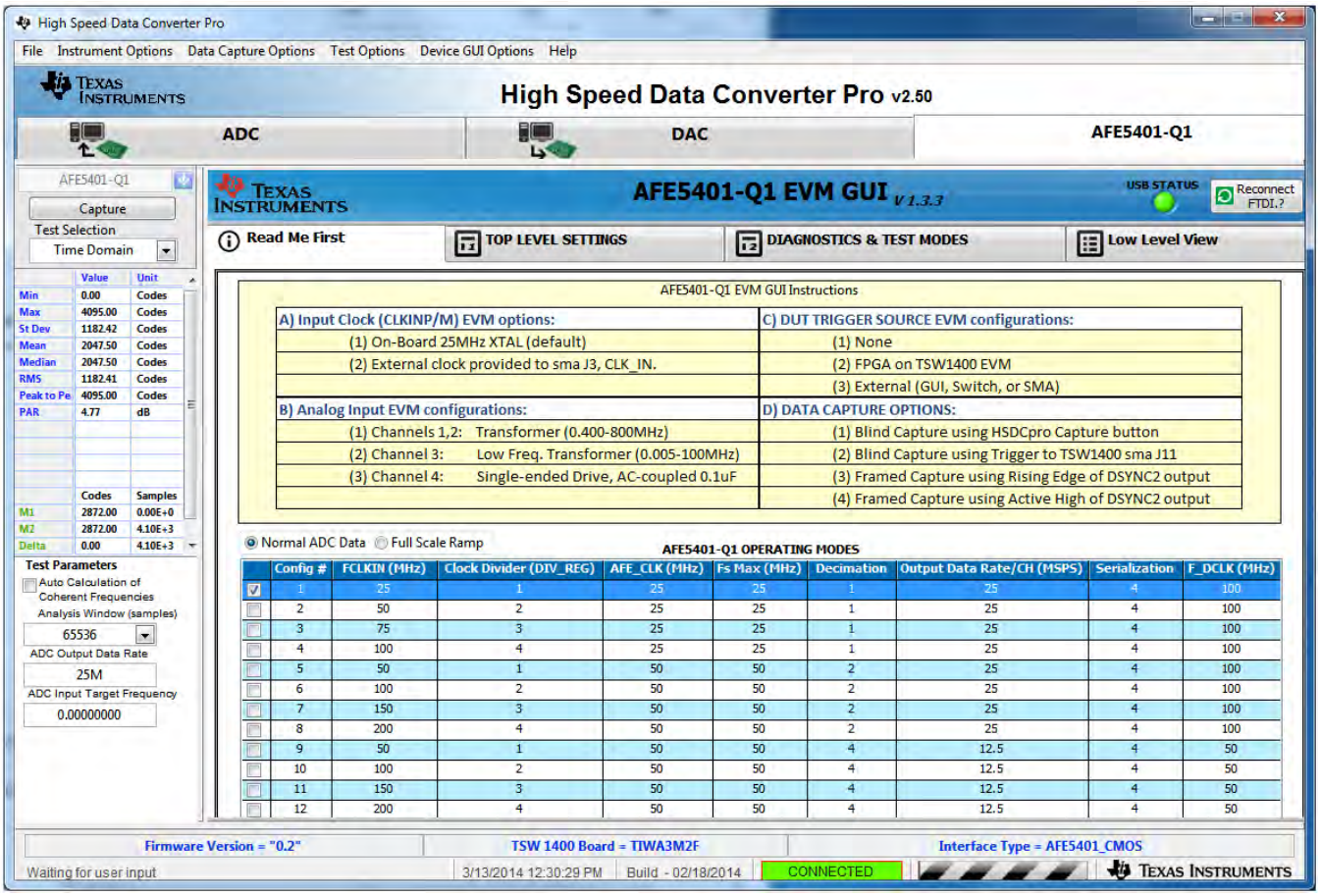


Figure 37. AFE5401-Q1 Sine Capture (a)

Upon selecting a new configuration, the message in Figure 38 appears while the EVM is being configured.

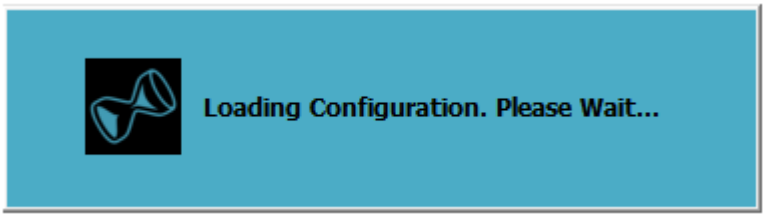


Figure 38. AFE5401-Q1 Sine Capture (b)

To measure device performance using a continuous sinusoidal input, it is necessary to use signal sources that have excellent phase noise for the sampling clock and the analog input. Further, the two supplies should be bandpass filtered and phase locked to one another for coherent sampling. Recall, for the RAMP capture in Section 5, the on-board crystal oscillator was used for the input clock. This cannot be used for coherent sampling. Move jumpers **J4**, **J5**, and **J8** from the **XTAL** position to the **XFMR** position and provide the appropriate clock frequency, 25 MHz in this example, to sma **J3**, **CLK_IN**.

(a) Press the **ADC** tab of the GUI

(b) Select ***Real FFT***

(c) Select ***Rectangular*** windowing

(d) Input the *ADC Input Target Frequency* (***4MHz*** in this example)

(e) Click the box *Auto Calculation of Coherent Frequencies*

(f) Reset the signal generator providing analog input signal to sma **J48**, **CH1**, to the newly calculated coherent frequency (***4.00047302MHz*** in this example)

(g) Press the ***Capture*** button

A capture similar to that shown in Figure 39 should appear. The SNR value of 67.55 dBFS is reported on the left panel which is very close to the datasheet typical of 67.7 dBFS.

Figure 39. AFE5401-Q1 Sine Capture (c)

High pass filtering in post processing can be invoked to remove the DC contribution. This can be achieved in the *HSDCpro* GUI by using the *Notch frequency bins* option as shown in Figure 40.

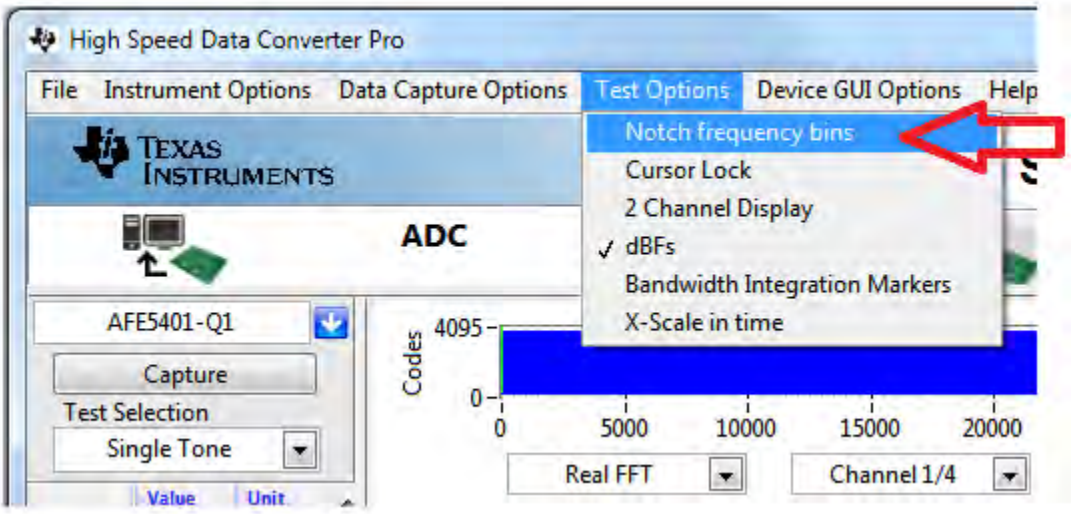


Figure 40. AFE5401-Q1 Sine Capture (d)

Change the ***Number of bins to remove after DC*** from *0* to *250* and press *OK* as shown in Figure 41.

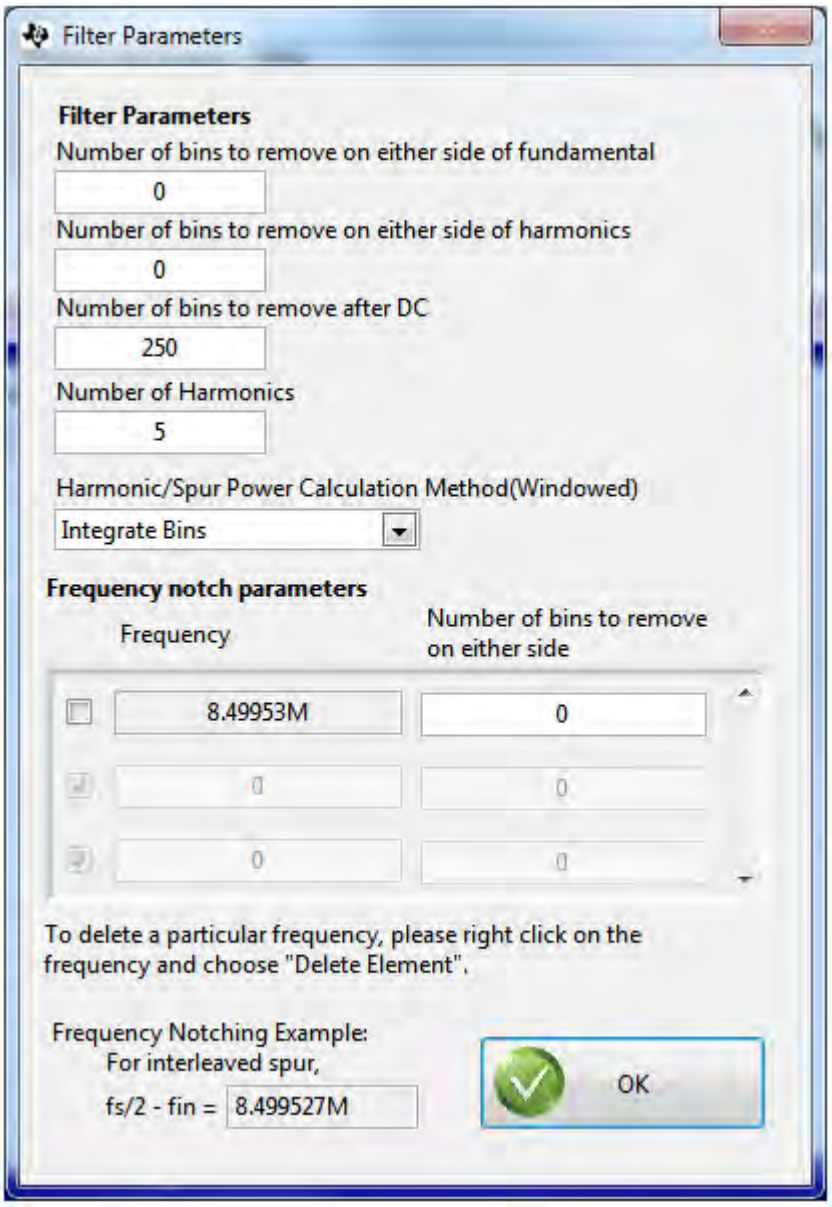


Figure 41. AFE5401-Q1 Sine Capture (e)

The FFT plot and the calculated parameters will update appropriately as shown in Figure 42. The SNR reported is now 68.13 dBFS.

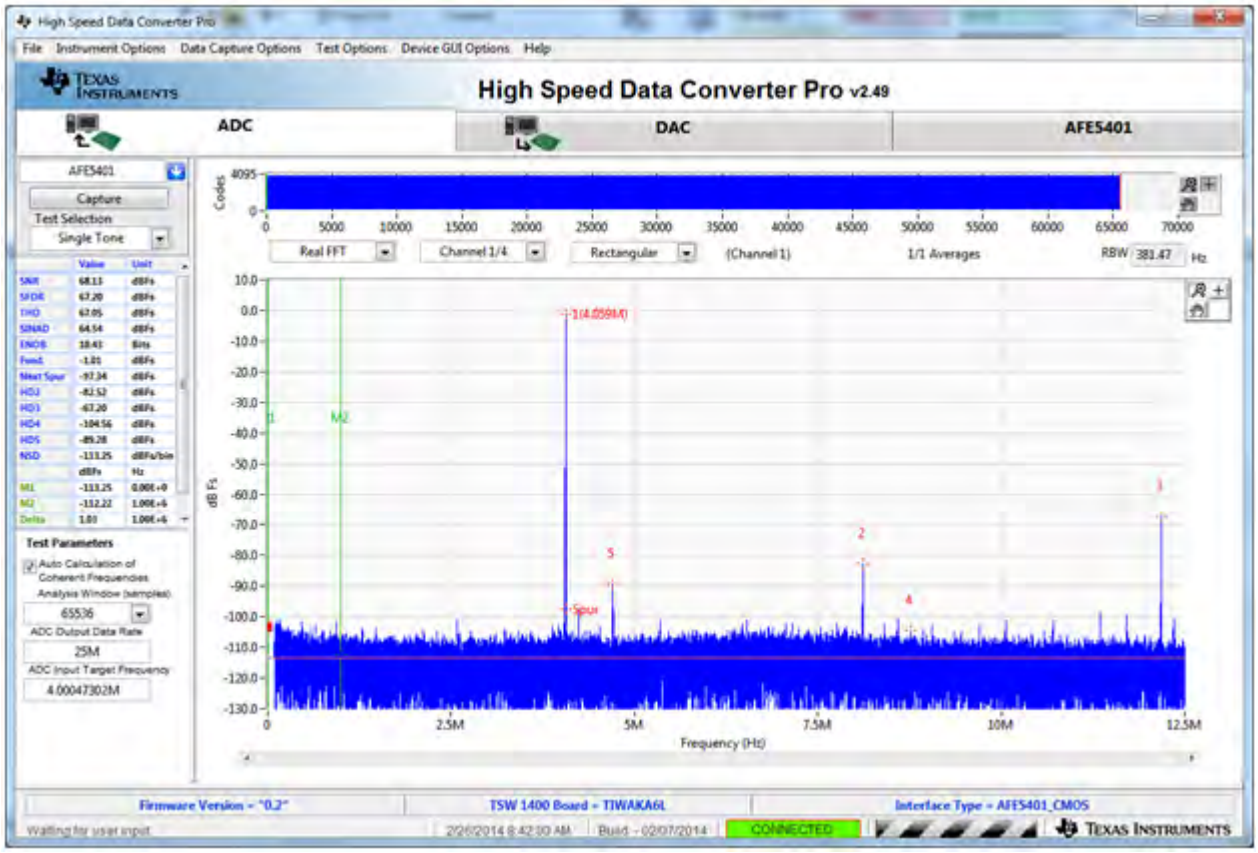


Figure 42. AFE5401-Q1 Sine Capture (f)

As mentioned throughout this user's guide, in order to achieve the SNR performance previously shown, signal sources with very good phase noise must be used. The above FFT was achieved using a Rhode & Schwarz SMA 100A signal generator for both the clock and analog input signals. By comparison, using an Agilent E4438C signal generator for the analog input signal with the rest of the setup remaining unchanged, including the input filter, the SNR degrades 3.7 dB to 64.44 dBFS as shown in Figure 43. From the spectrum, it is apparent that the phase noise and the harmonic distortion is inferior for this instrument. If high quality signal generators are not available, using windowing functions is necessary to get good results. Simply change the drop-down menu in *HSDCpro* from *Rectangular to Hamming*, *Hanning*, or *Blackman* to see the effect of windowing.

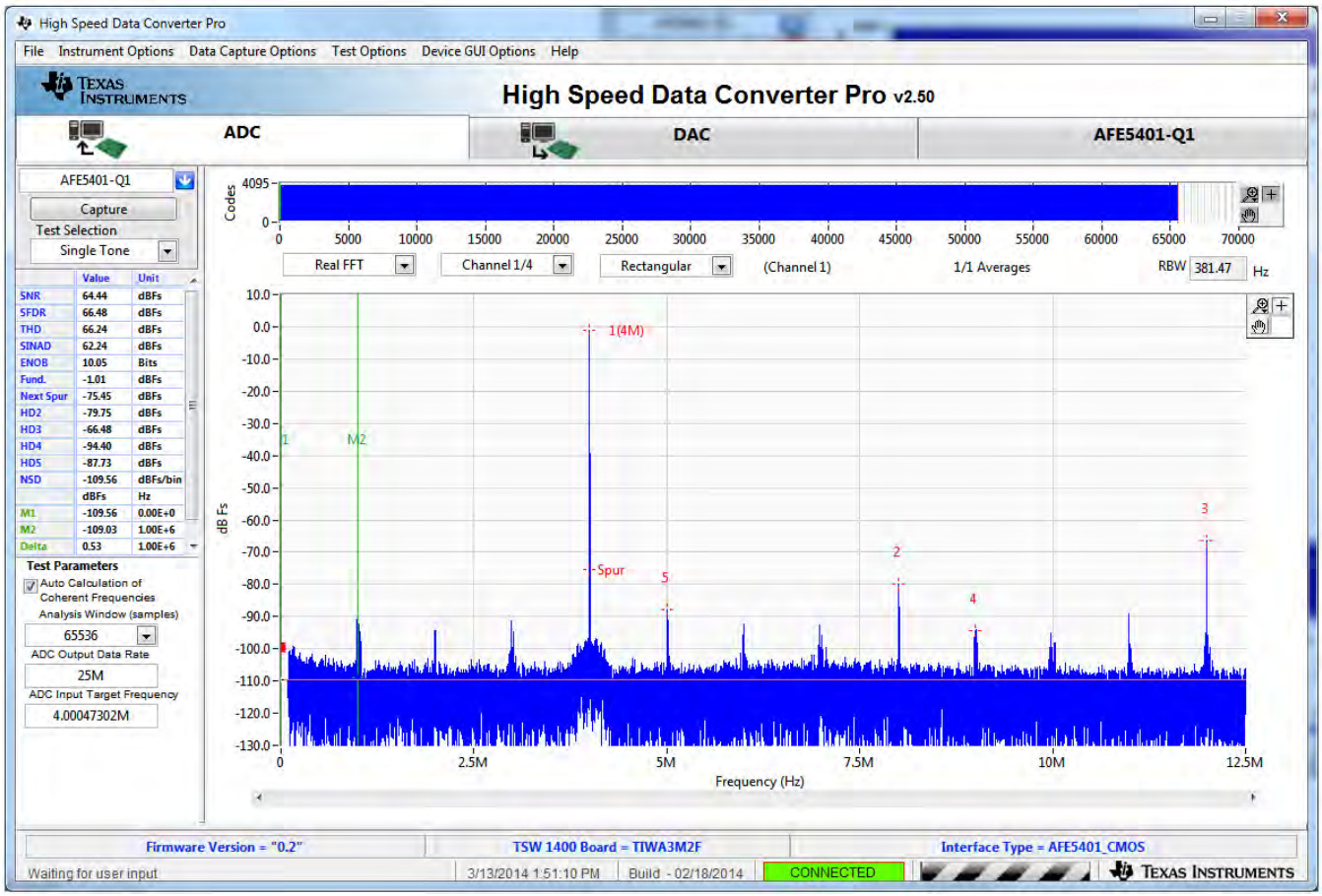


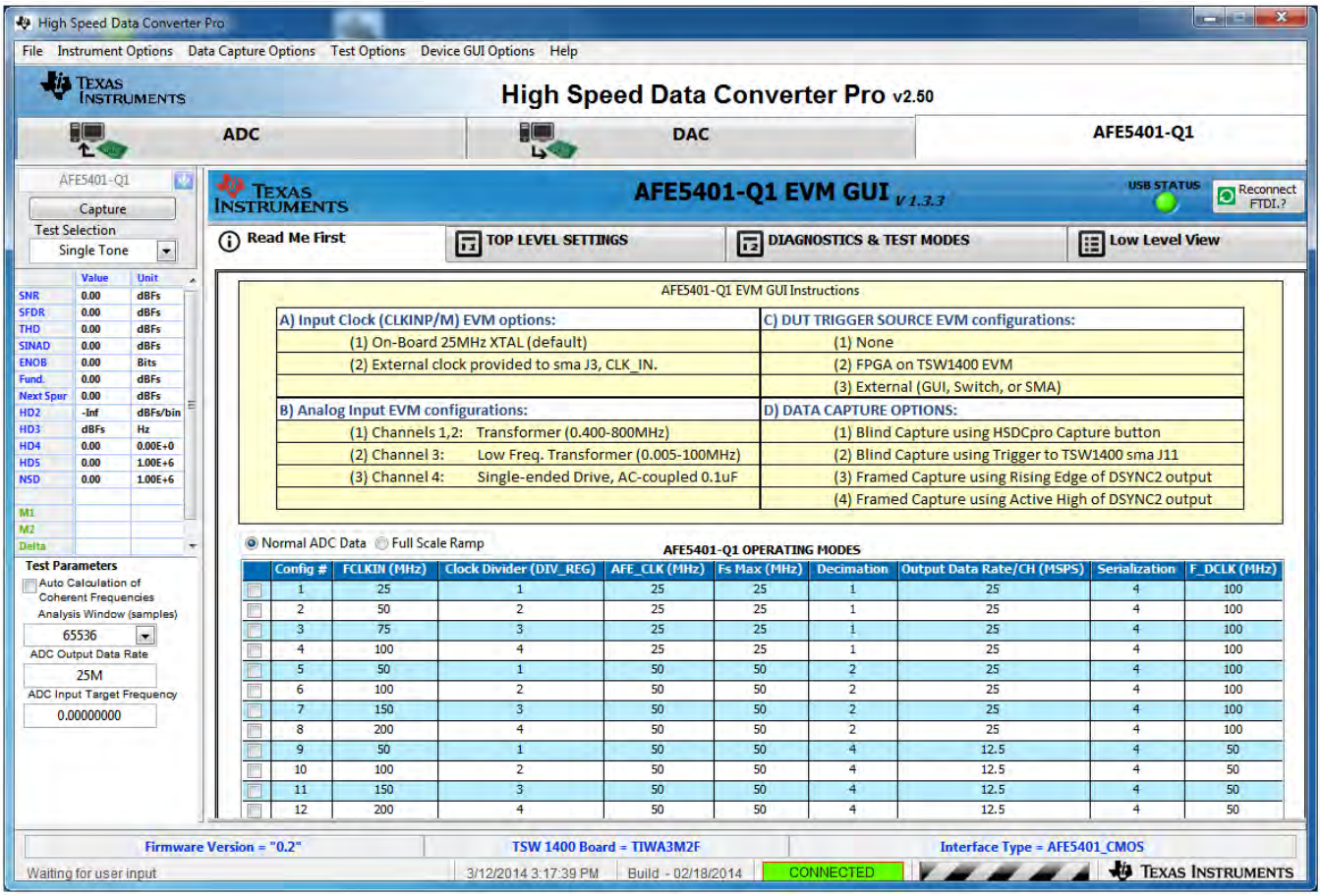
Figure 43. AFE5401-Q1 Sine Capture (g)

7 AFE5401-Q1 GUI Software in Detail

The AFE5401-Q1 GUI software comprises four tabs: (1) *Read Me First*, (2) *TOP LEVEL SETTINGS*, (3) *DIAGNOSTICS & TEST MODES*, and (4) *Low Level View*. A section is dedicated to describing each tab in detail.

7.1 Read Me First Tab

The *Read Me First* tab is the starting point for the GUI when launched and appears as shown in Figure 44. If an AFE5401-Q1 EVM is connected and detected, the USB STATUS indicator located in the upper right hand corner will be green.



Config #	FCLKIN (MHz)	Clock Divider (DIV_REG)	AFE_CLK (MHz)	Fs Max (MHz)	Decimation	Output Data Rate/CH (MSPS)	Serialization	F_DCLK (MHz)
1	25	1	25	25	1	25	4	100
2	50	2	25	25	1	25	4	100
3	75	3	25	25	1	25	4	100
4	100	4	25	25	1	25	4	100
5	50	1	50	50	2	25	4	100
6	100	2	50	50	2	25	4	100
7	150	3	50	50	2	25	4	100
8	200	4	50	50	2	25	4	100
9	50	1	50	50	4	12.5	4	50
10	100	2	50	50	4	12.5	4	50
11	150	3	50	50	4	12.5	4	50
12	200	4	50	50	4	12.5	4	50

Figure 44. AFE5401-Q1 Read Me First GUI Tab (a)

If at any time the USB connection is disrupted and an action is attempted, the USB STATUS indicator turns dark and the error message shown in Figure 45 appears. ***Continue in Simulation*** mode by pressing the appropriate button. In this mode, all GUI controls appear to be working normally without actually writing to the device.

Figure 45. AFE5401-Q1 Read Me First GUI Tab (b)

To exit simulation mode and reestablish connection with the EVM, ensure the USB connection is made and press the ***Reconnect FTDI.?*** button in top right corner of the GUI. Upon reconnecting, the indicator should return to the green color.

The upper half of the *Read Me First* tab provides descriptions of the various EVM configurations available for clock and analog inputs, the various DUT trigger configurations available, and the different data capture options available.

The lower half of the page provides a table describing the various operating modes supported by the device as they relate to input clock, AFE_CLK, and decimation factor. These modes describe the upper specification for clock speeds. Of course, the device can support slower speeds so long at the minimum specifications in the datasheet are respected. By clicking the appropriate checkbox to the left side of each config#, the device can be automatically configured. Further, for each configuration, either *Normal ADC Data*, (sampling the analog input), or a *Full Scale Ramp* (generated within the device at the CMOS output) can be selected.

7.2 TOP LEVEL SETTINGS Tab

The *TOP LEVEL SETTINGS* tab contains all the controls for configuring the device for normal operation. As shown in Figure 46, the tab is divided into six sub-sections with each titled in blue: *TRIGGER & CAPTURE CONFIGURATION*, *CLOCK CONFIGURATION & PDN*, *ANALOG CONFIG*, *DIGITAL CONFIGURATION*, *PIN CTRL*, and *LAST WRITE*.

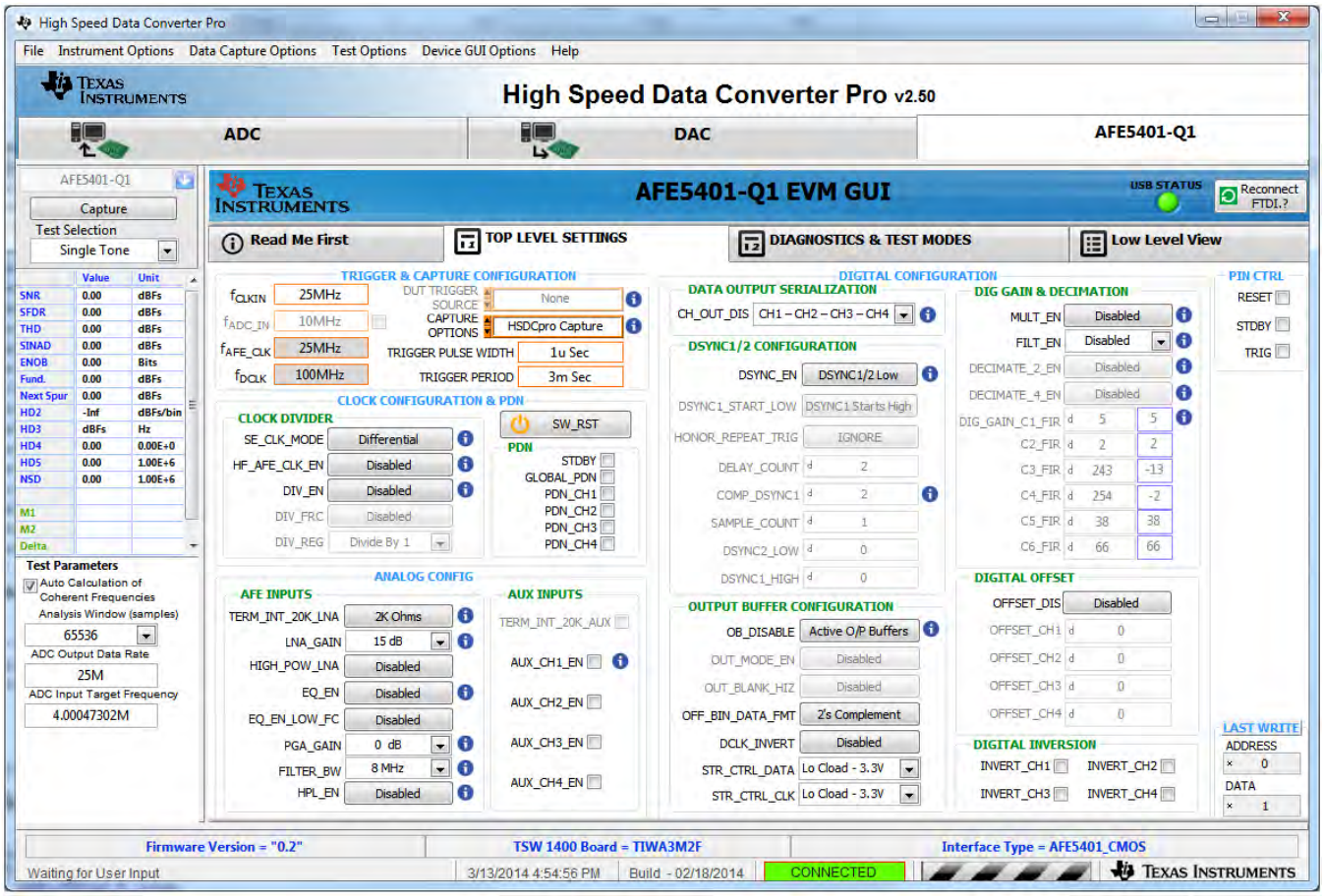


Figure 46. AFE5401-Q1 TOP LEVEL SETTINGS Tab

7.2.1 TRIGGER & CAPTURE CONFIGURATION

The *TRIGGER & CAPTURE CONFIGURATION* sub-section is the only section that does not write directly to the AFE5401-Q1. This sub-section is used to display and control the EVM setup including the input clock frequency, data capture method, and device trigger method. As shown in Figure 47, the input clock to the AFE5401-Q1 should be entered in the f_{CLKIN} box. With this input, the GUI calculates what the ***ADC Output Data Rate*** will be for the current device configuration and updates this parameter in fixed left

panel of the GUI. This value is a function of the decimation factor set. Also calculated are the frequencies of the AFE_CLK, f_{AFE_CLK}, and of the DCLK, f_{DCLK}. As shown in the functional block diagram in the datasheet, the AFE_CLK is the rate at which the ADCs are sampling and is a function of the input clock divider. DCLK is the CMOS output clock and is a function of the AFE_CLK as well as the serialization factor.

NOTE: ADC input signal frequency, f_{ADC_IN}, is another control shown. However, this control is greyed and disabled as this feature will be provided in a future release of the software. Once enabled, providing a value here will automatically update the same control in HSDCpro.

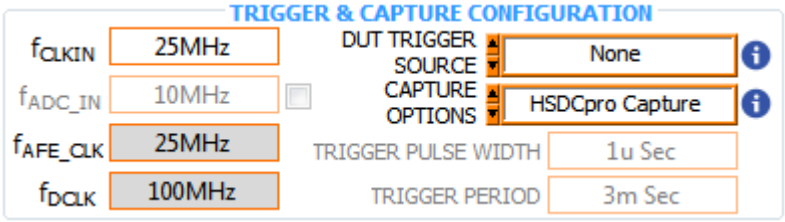


Figure 47. AFE5401-Q1 TRIGGER & CAPTURE CONFIGURATION Section (a)

The AFE5401-Q1 EVM allows for several options for providing a trigger to the **TRIG** pin of the device. These options are listed in the control called **DUT TRIGGER SOURCE** as shown in Figure 48. When the ***DSYNC_EN*** control is disabled (*DSYNC1/2 Low*), DSYNC1 and DSYNC2 output signals are disabled regardless of whether or not a trigger is provided to the device. Therefore, in this case, the ***DUT TRIGGER SOURCE*** control automatically sets to *None*. Once ***DSYNC_EN*** is enabled by the user, the remaining four trigger options become available for selection. The option ***FPGA on TSW1400*** enables the trigger pulse generation in the Stratix IV FPGA on the TSW1400 capture card.

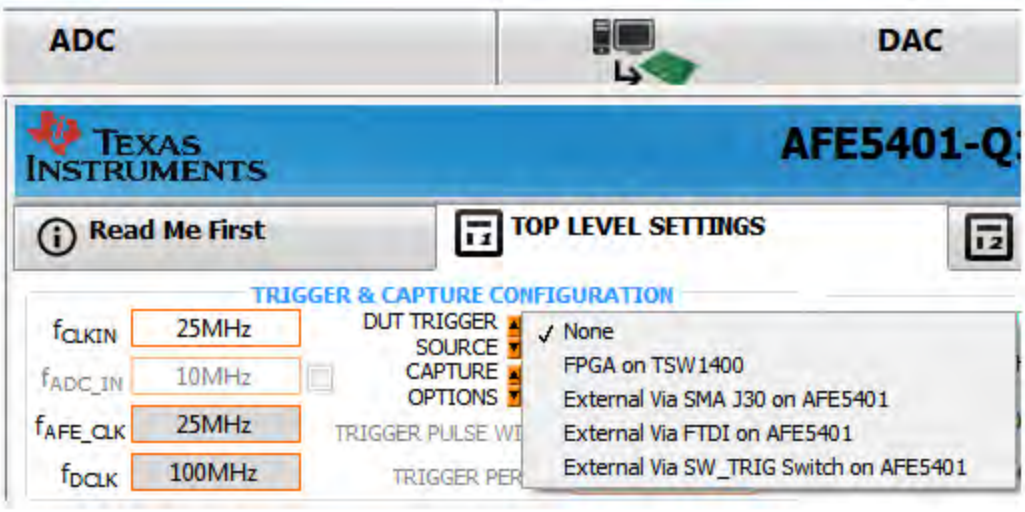


Figure 48. AFE5401-Q1 TRIGGER & CAPTURE CONFIGURATION Section (b)

As shown in Figure 49, when ***FPGA on TSW1400*** is selected for the trigger source, the controls ***TRIGGER PULSE WIDTH*** and ***TRIGGER PERIOD*** become active, allowing the user flexibility in configuring the trigger pulse repetition frequency (PRF).

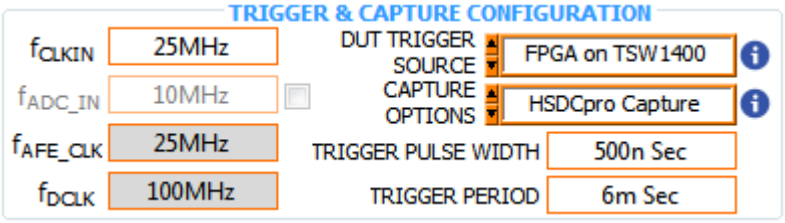


Figure 49. AFE5401-Q1 TOP LEVEL SETTINGS Tab (c)

The remaining three options for providing a trigger to the device include ***External Via SMA J30 on AFE5401***, ***External Via FTDI on AFE5401***, and ***External Via SW_TRIG Switch on AFE5401***. Each trigger option requires a unique jumper configuration in the section of the EVM labeled *TRIG*. Press the information button to the right of the ***DUT TRIGGER SOURCE*** control to see the jumper configurations as shown in Figure 50.

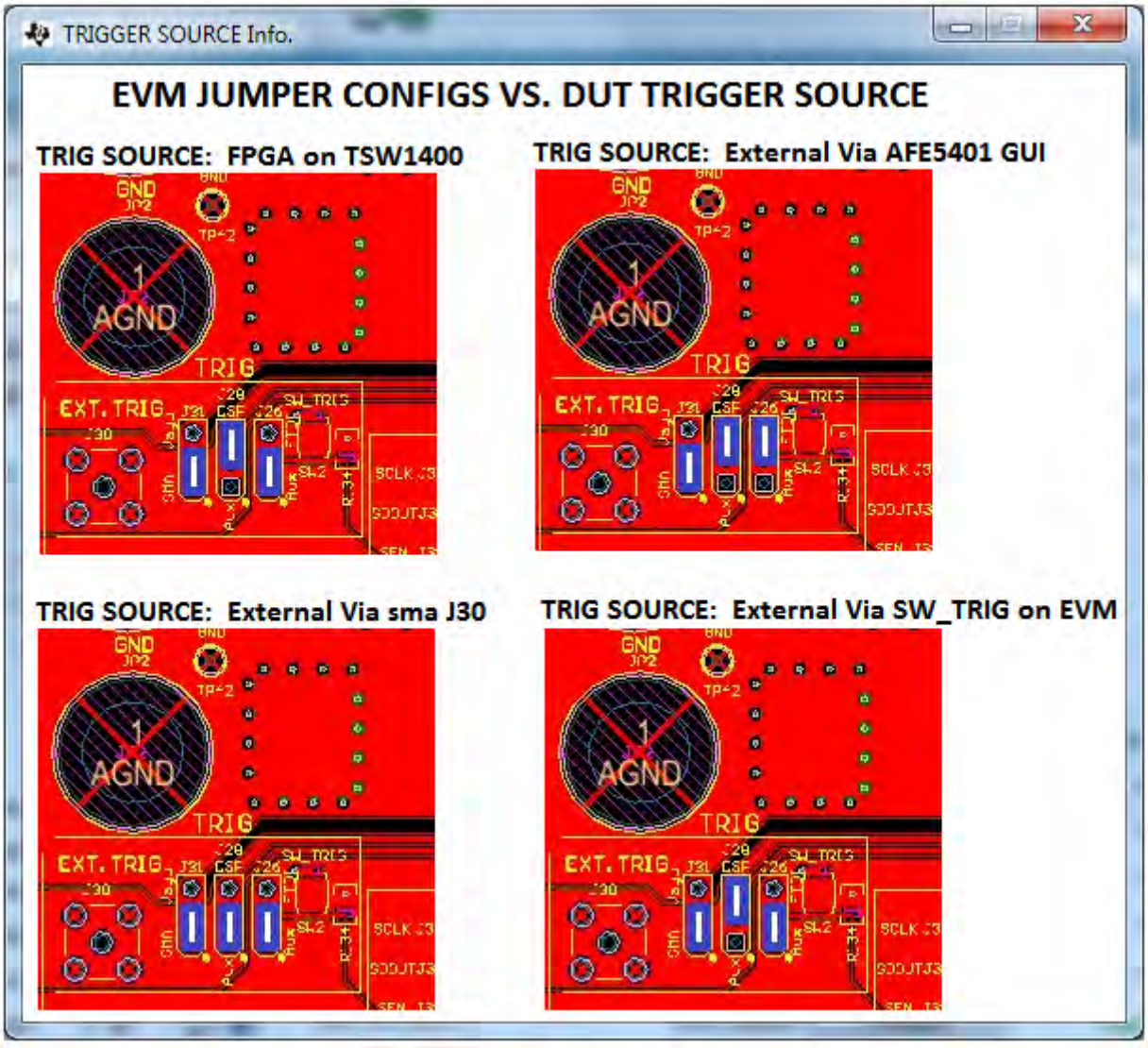


Figure 50. AFE5401-Q1 TRIGGER & CAPTURE CONFIGURATION Section (e)

The AFE5401-Q1 evaluation kit allows for several options for capturing data using the TSW1400 capture card. The GUI control ***CAPTURE OPTIONS*** lists these options as shown in Figure 51. As shown, when the ***DUT TRIGGER SOURCE*** is set to *None*, only *HSDCpro Capture Button (Blind Capture)* and *Trigger to TSW1400 SMA J11 (Blind Capture)* options are available, both of which are 'blind' captures.

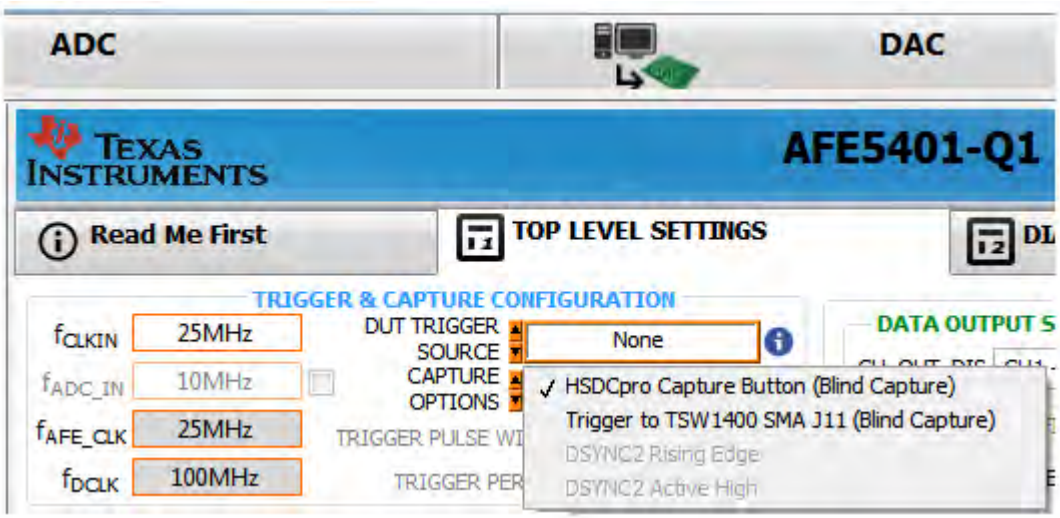


Figure 51. AFE5401-Q1 TRIGGER & CAPTURE CONFIGURATION Section (f)

Blind Capture means that channelization is impossible to determine as the output framing signals DSYNC1 and DSYNC2 are disabled. Appendix A provides an overview of blind captures. When ***DUT TRIGGER SOURCE*** is set to anything other than *None*, the remaining two ***CAPTURE OPTIONS***, *DSYNC2 Rising Edge* and *DSYNC2 Active High*, become active. As the name implies, when *DSYNC2 Rising Edge* is selected, the FPGA receiver begins capture on the first detected rising edge of the DSYNC2 output signal. Similarly, if *DSYNC2 Active High* is selected, only samples corresponding to when the DSYNC2 output signal is high will be captured in the receiver. With these two options, correct channelization is guaranteed. These two receivers implementations are explored more in Appendix B.

7.2.2 CLOCK CONFIGURATION & PDN

The *CLOCK CONFIGURATION & PDN* section, as shown in Figure 52, provides controls for the device input clock, power down controls, and a software reset button (***SW_RST***). Pressing ***SW_RST*** resets all registers to a known power-on reset value, and these changes are reflected in all controls of the GUI. The information buttons next to some controls contain pertinent information to the EVM configuration or the datasheet.

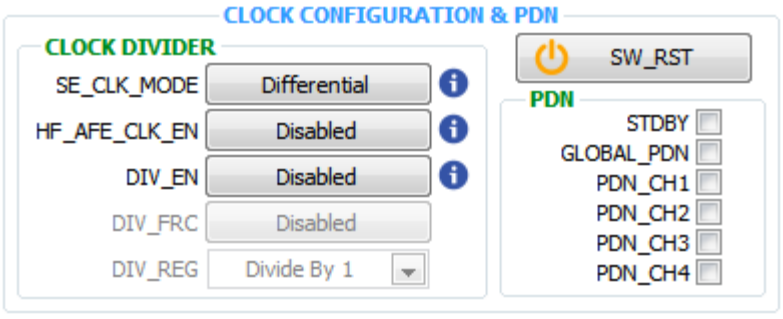


Figure 52. AFE5401-Q1 CLOCK CONFIGURATION & PDN Section (a)

CAUTION

It is possible to configure the device such that it violates the datasheet specifications.

The example shown in Figure 53 shows such a violation when ***DIV_REG*** is set to *Divide By 4* while the f_{CLKIN} to the device is set to *25MHz*.

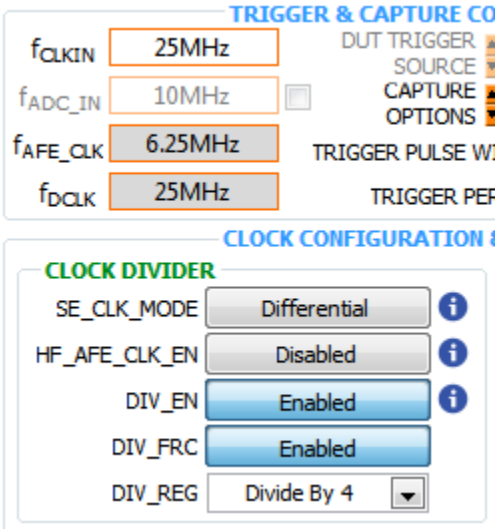


Figure 53. AFE5401-Q1 CLOCK CONFIGURATION & PDN Section (b)

In cases such as this, the message shown in Figure 54 appears, informing the user that a violation has occurred and correct operation cannot be guaranteed.

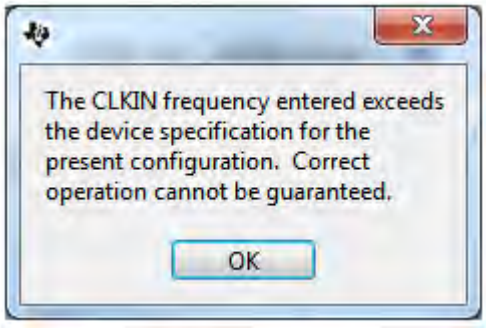


Figure 54. AFE5401-Q1 CLOCK CONFIGURATION & PDN Section (c)

7.2.3 Analog Config

The *ANALOG CONFIG* section shown in Figure 55 contains all the controls for the analog inputs to the AFE5401-Q1. As defined in the datasheet, the PGA gain increases by 15 dB when the equalizer function is enabled and is reflected in the GUI controls.

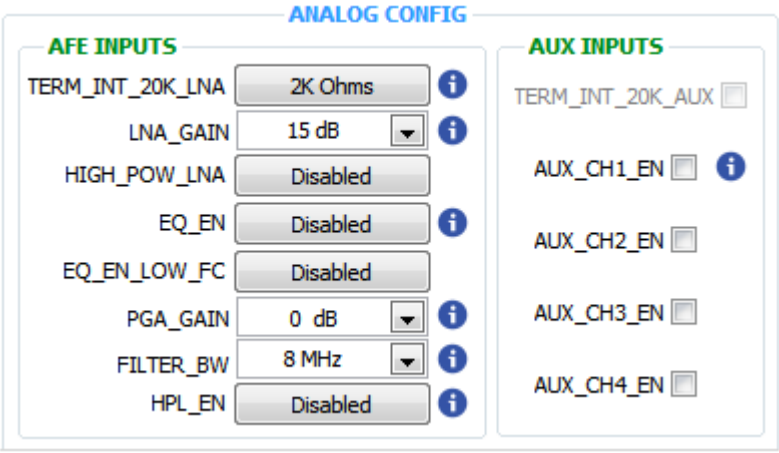


Figure 55. AFE5401-Q1 ANALOG CONFIG Section

7.2.4 Digital Configuration

The *DIGITAL CONFIGURATION* section, shown in Figure 56, provides all controls related to digital functionality of the device.

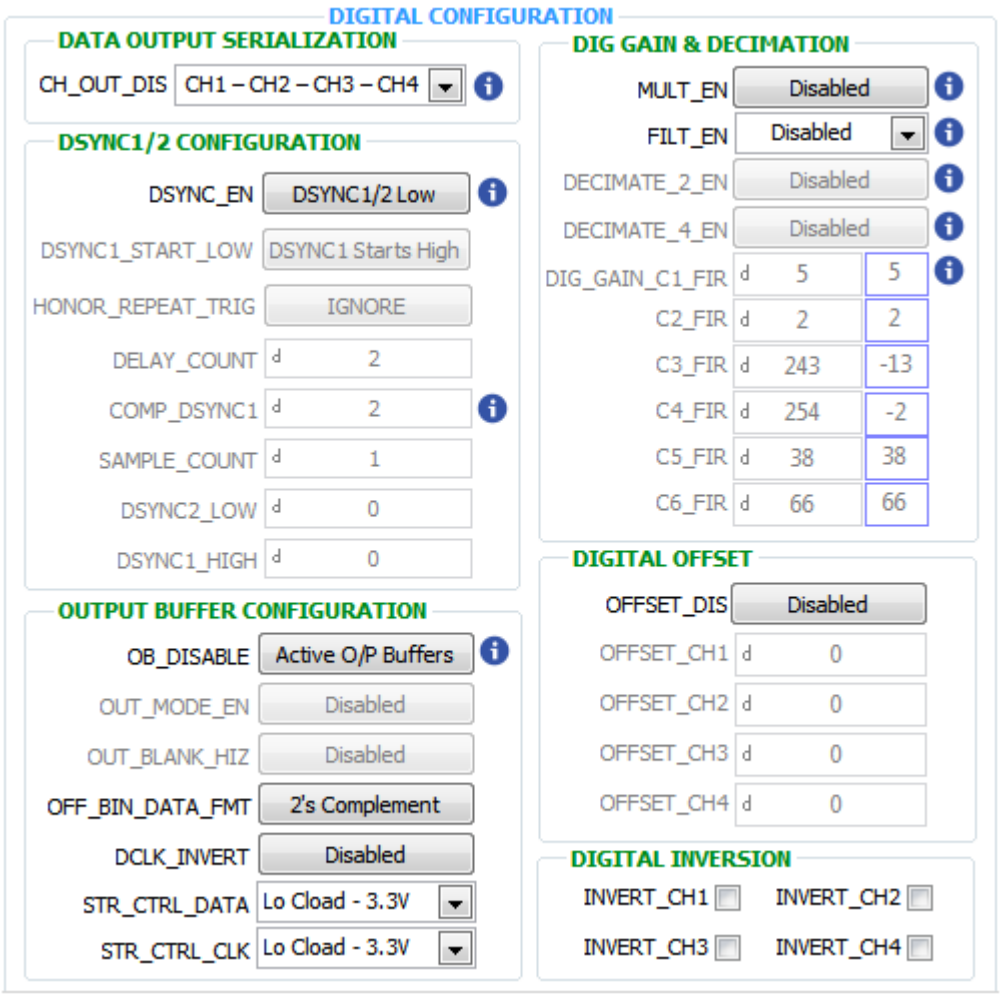


Figure 56. AFE5401-Q1 DIGITAL CONFIGURATION Section (a)

In the *DIG GAIN & DECIMATION* sub-section, the FIR filter coefficients are selected from the control ***FILT_EN*** as shown in Figure 57. Only when ***Custom Coeffs*** is selected can the ***Cx_FIR*** controls be input in either decimal or signed 2's complement format.

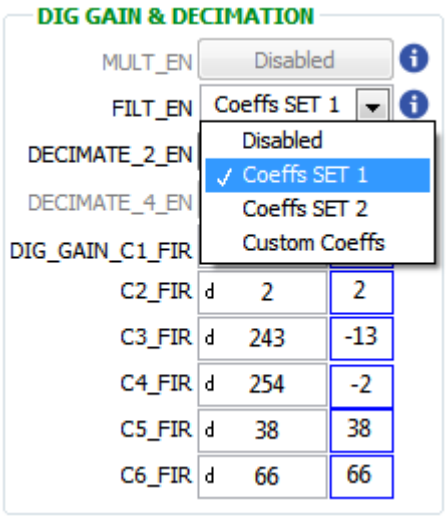


Figure 57. AFE5401-Q1 DIGITAL CONFIGURATION Section (b)

Also worth noting is that in order to configure the device for decimating by 4, both ***DECIMATE_2_EN*** and ***DECIMATE_4_EN*** should be Enabled. As these controls are changed, the ***ADC Output Data Rate*** displayed in the fixed left panel of the GUI is automatically updated.

7.2.5 PIN CTRL

The *PIN CTRL* section, shown in Figure 58, provides signals from the GUI to specific device pins. ***RESET*** is a self-resetting pulse that resets all SPI registers to the default power-on state. This function does the same as the ***SW_RST*** control. A third, alternative, method to reset the device is to press the **SW_RESET** button located at **SW1** in the RESET section of the EVM.

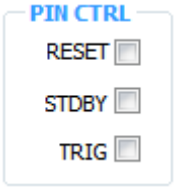


Figure 58. AFE5401-Q1 PIN CTRL Section

The device can set to standby mode by checking the ***STDBY*** box, thus, providing a logic high value to this device pin. This function does the same as the ***STDBY*** control in the GUI. Finally, as mentioned in Section 7.1, a single pulse trigger signal can be provided to device pin ***TRIG*** as an option for triggering the generation of the DSYNC1/2 output framing signals.

7.2.6 LAST WRITE

The *LAST WRITE* section, shown in Figure 59, displays the most recent data write to the serial interface of the device. It is useful for quickly understanding the register address of each control. This section is provided on both control tabs of the GUI.

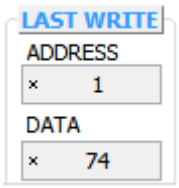


Figure 59. AFE5401-Q1 LAST WRITE Section

7.3 DIAGNOSTICS & TEST MODES Tab

The *DIAGNOSTICS & TEST MODES* tab shown in Figure 60 provides all controls for configuring the device for test modes and other diagnostics available.

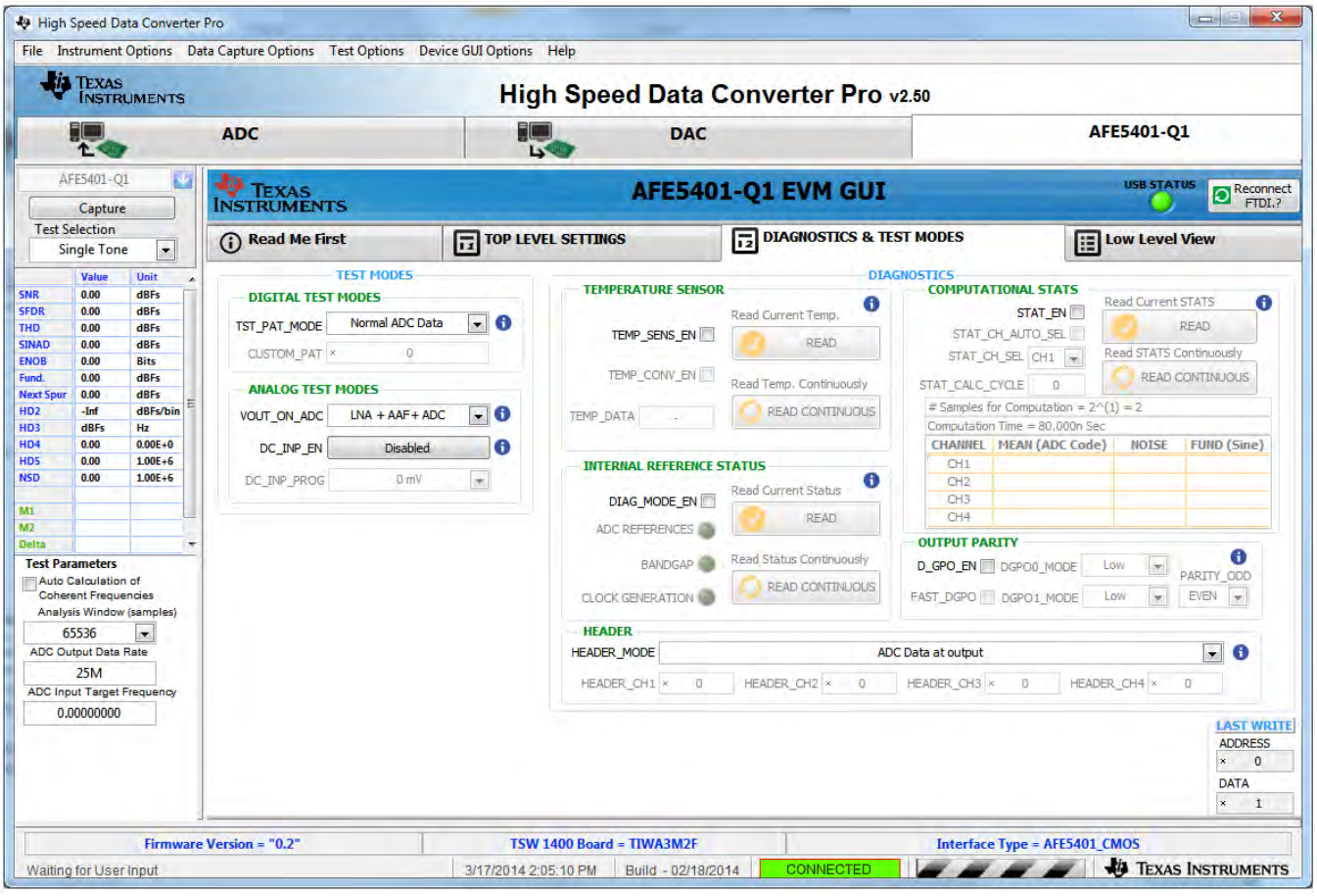


Figure 60. AFE5401-Q1 DIAGNOSTICS & TEST MODES Tab (a)

7.4 Low Level View Tab

The *Low Level View* tab shown in Figure 61 provides a register map with bit descriptions for all registers of the device. Writing and Read back of any register is possible on this tab. Also, the ***Save Config*** button allows for saving to a .cfg file the present configuration of all registers as well as the *TRIGGER & CAPTURE CONFIGURATION*. The ***Load Config*** button allows a user to recall such a saved state.

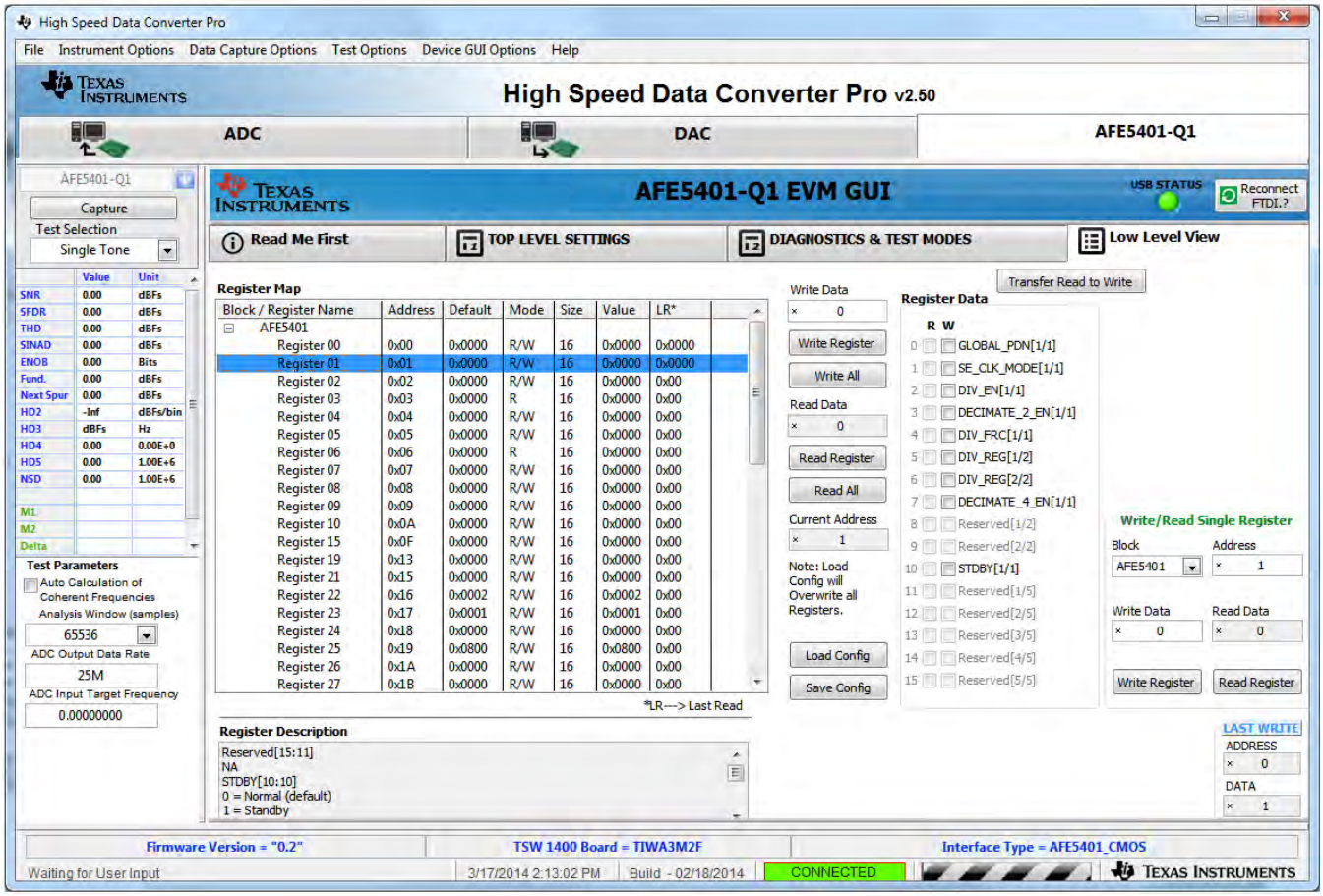


Figure 61. AFE5401-Q1 DIAGNOSTICS & TEST MODES Tab (b)

8 AFE5401-Q1 EVM Schematic

Figure 62 through Figure 70 show the AFE5401-Q1 EVM schematics.

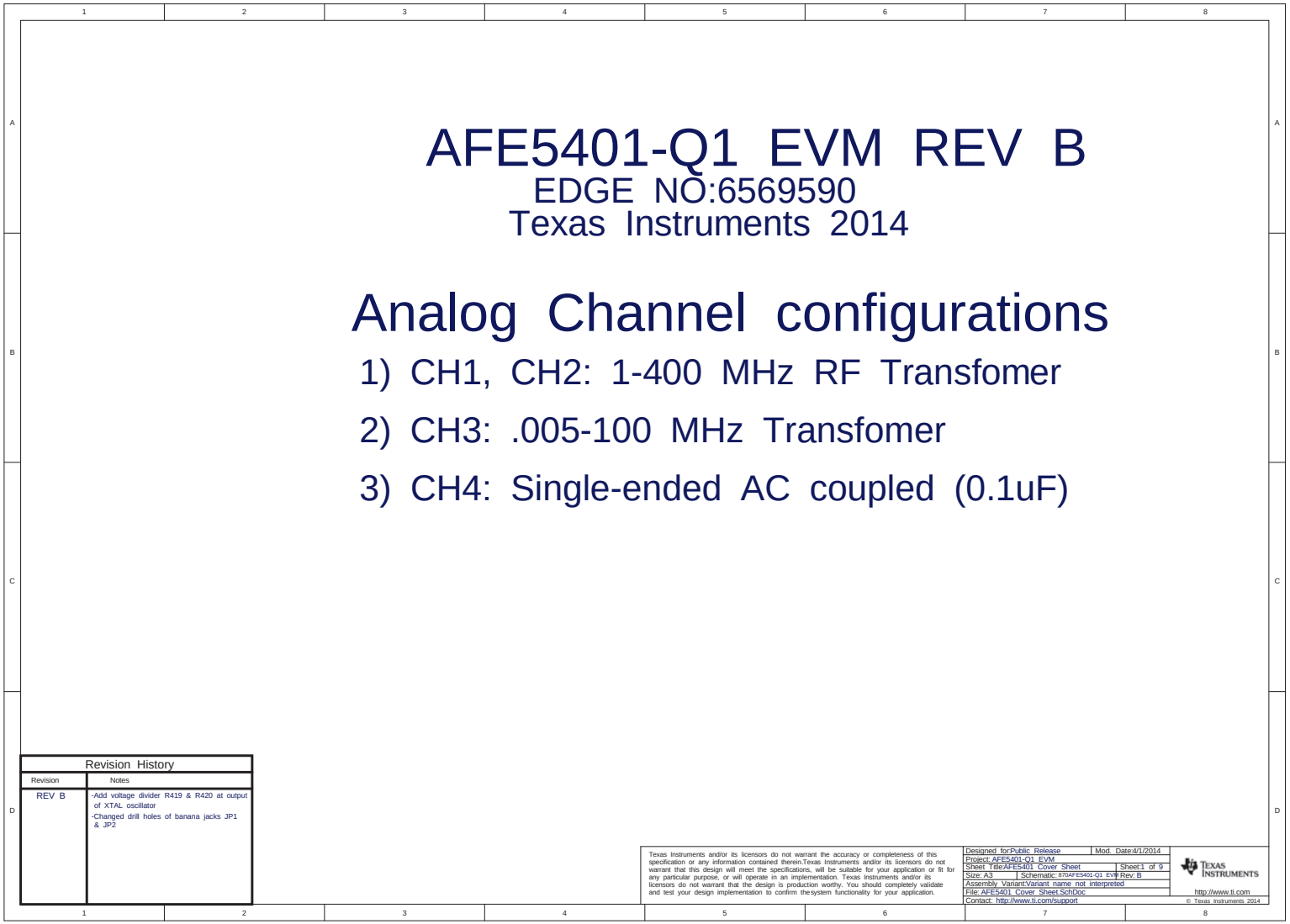


Figure 62. AFE5401-Q1 EVM Schematic Sheet 1

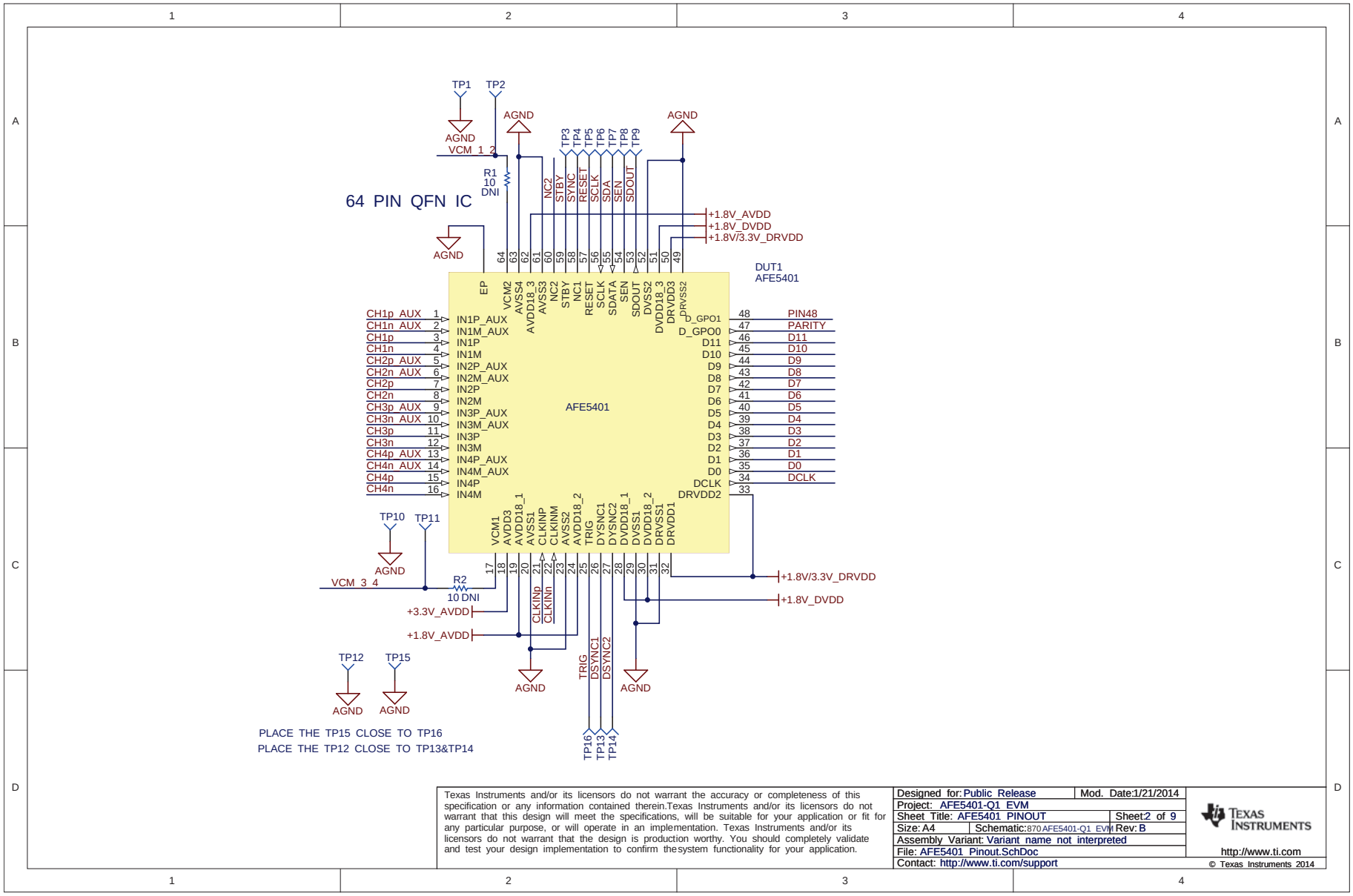


Figure 63. AFE5401-Q1 EVM Schematic Sheet 2

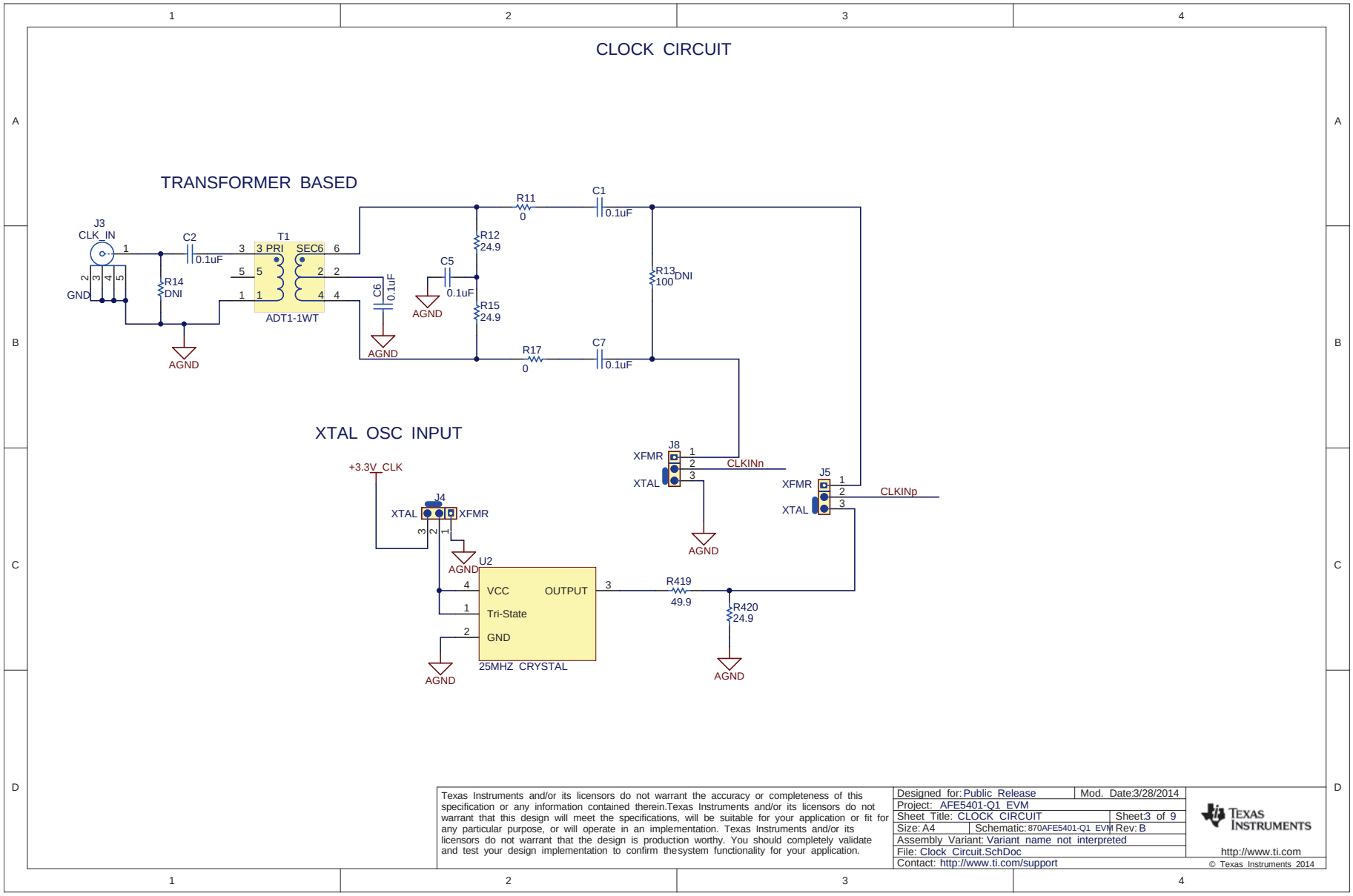


Figure 64. AFE5401-Q1 EVM Schematic Sheet 3

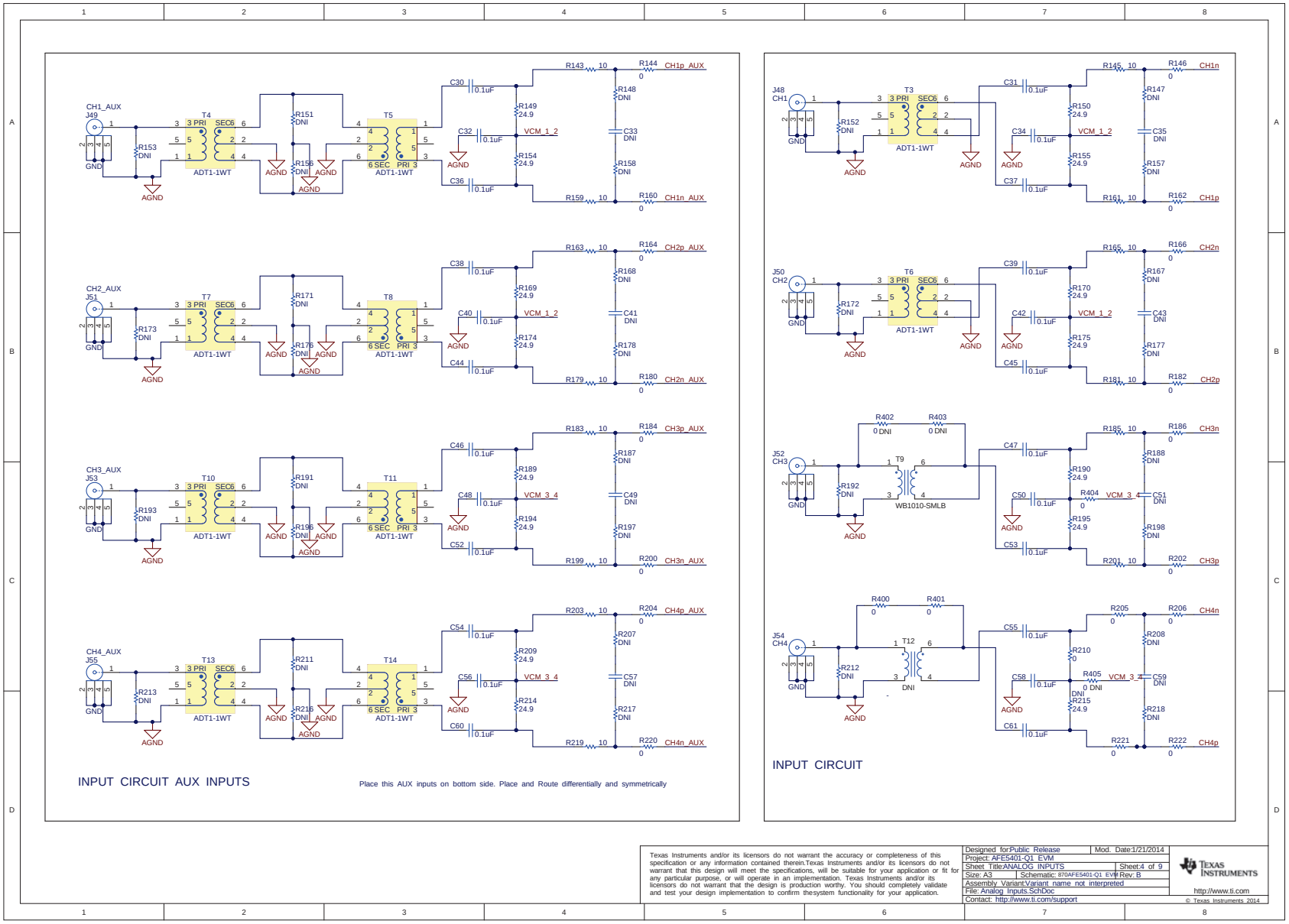


Figure 65. AFE5401-Q1 EVM Schematic Sheet 4

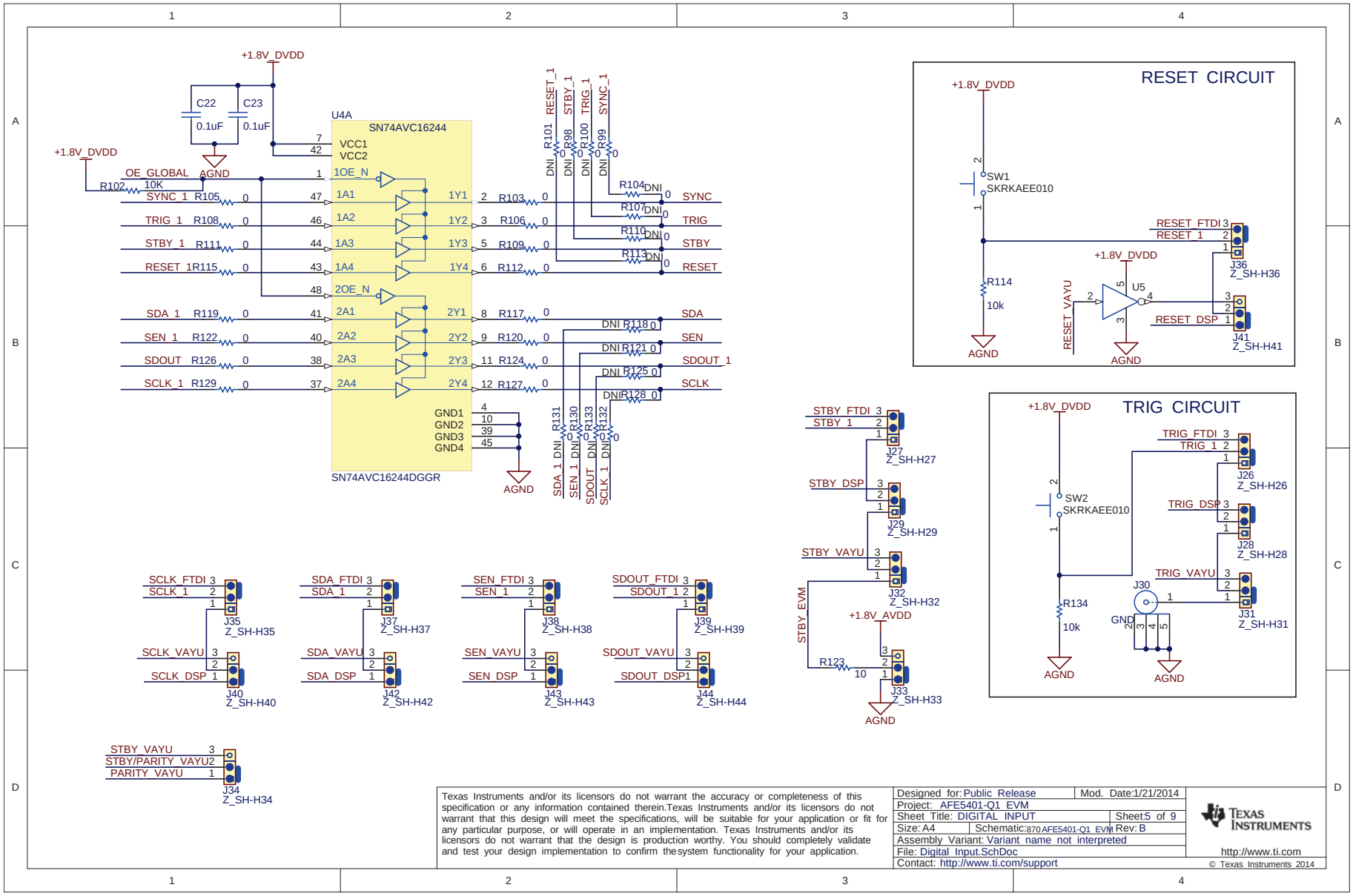


Figure 66. AFE5401-Q1 EVM Schematic Sheet 5

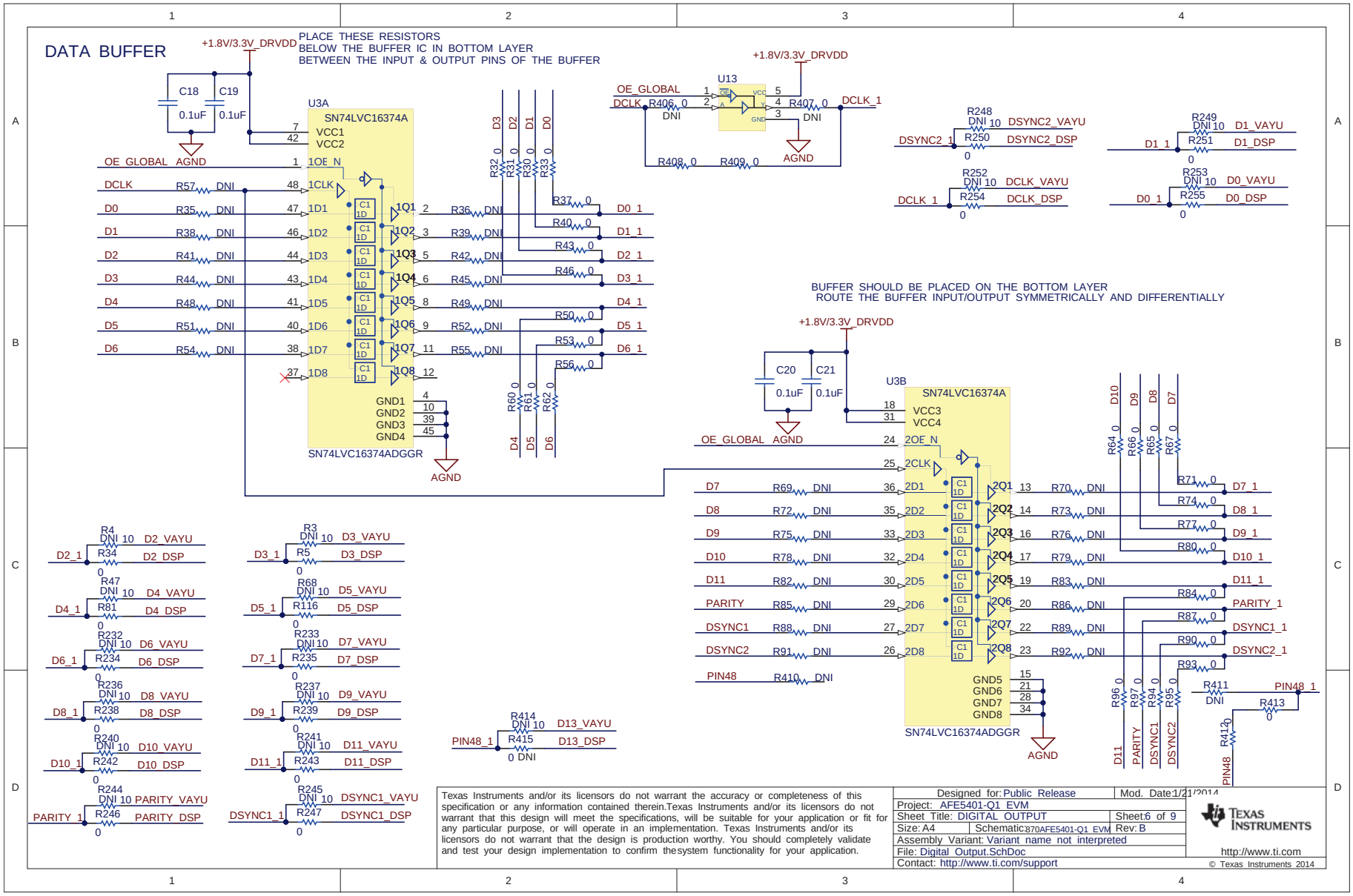


Figure 67. AFE5401-Q1 EVM Schematic Sheet 6

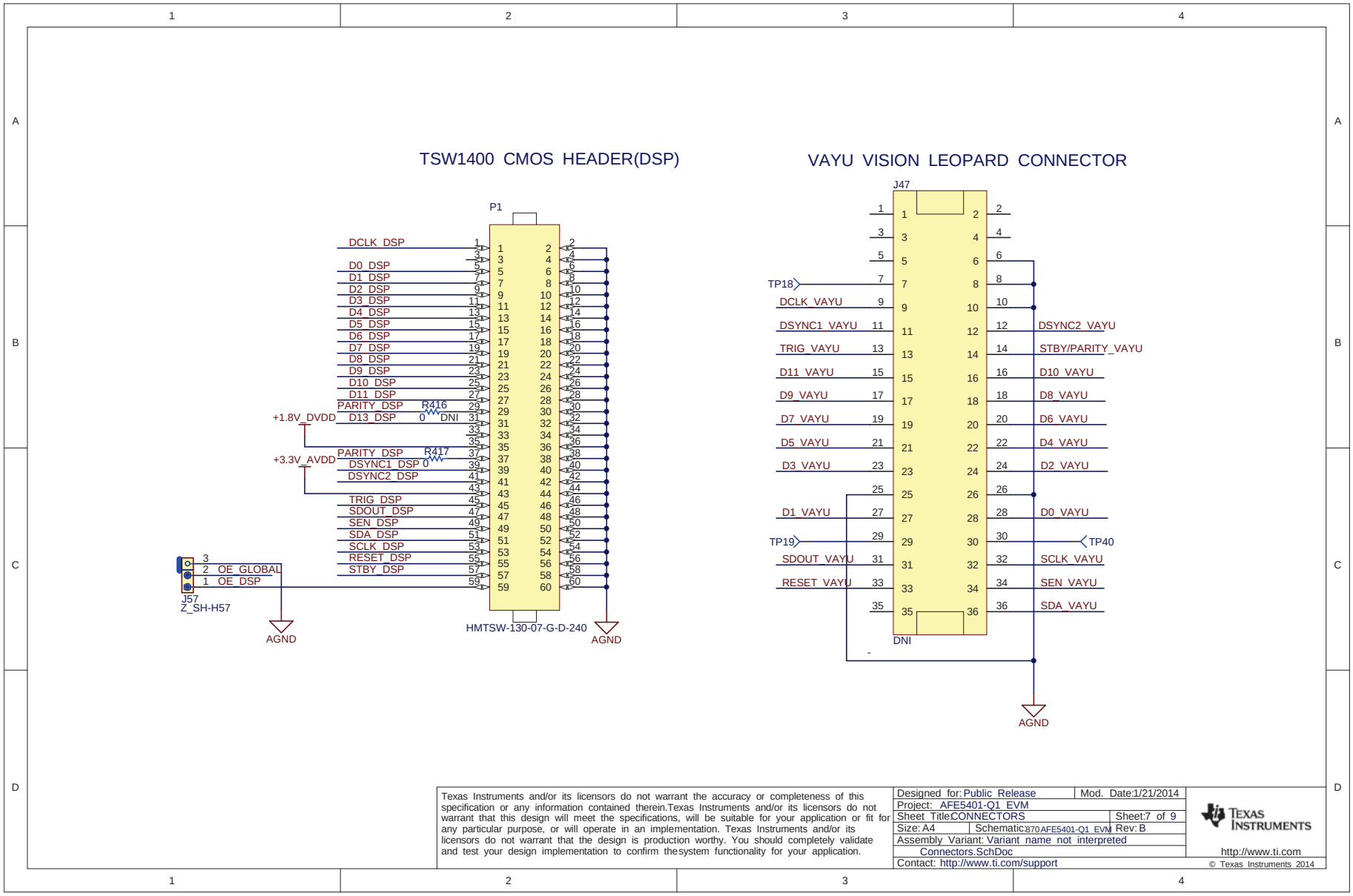


Figure 68. AFE5401-Q1 EVM Schematic Sheet 7

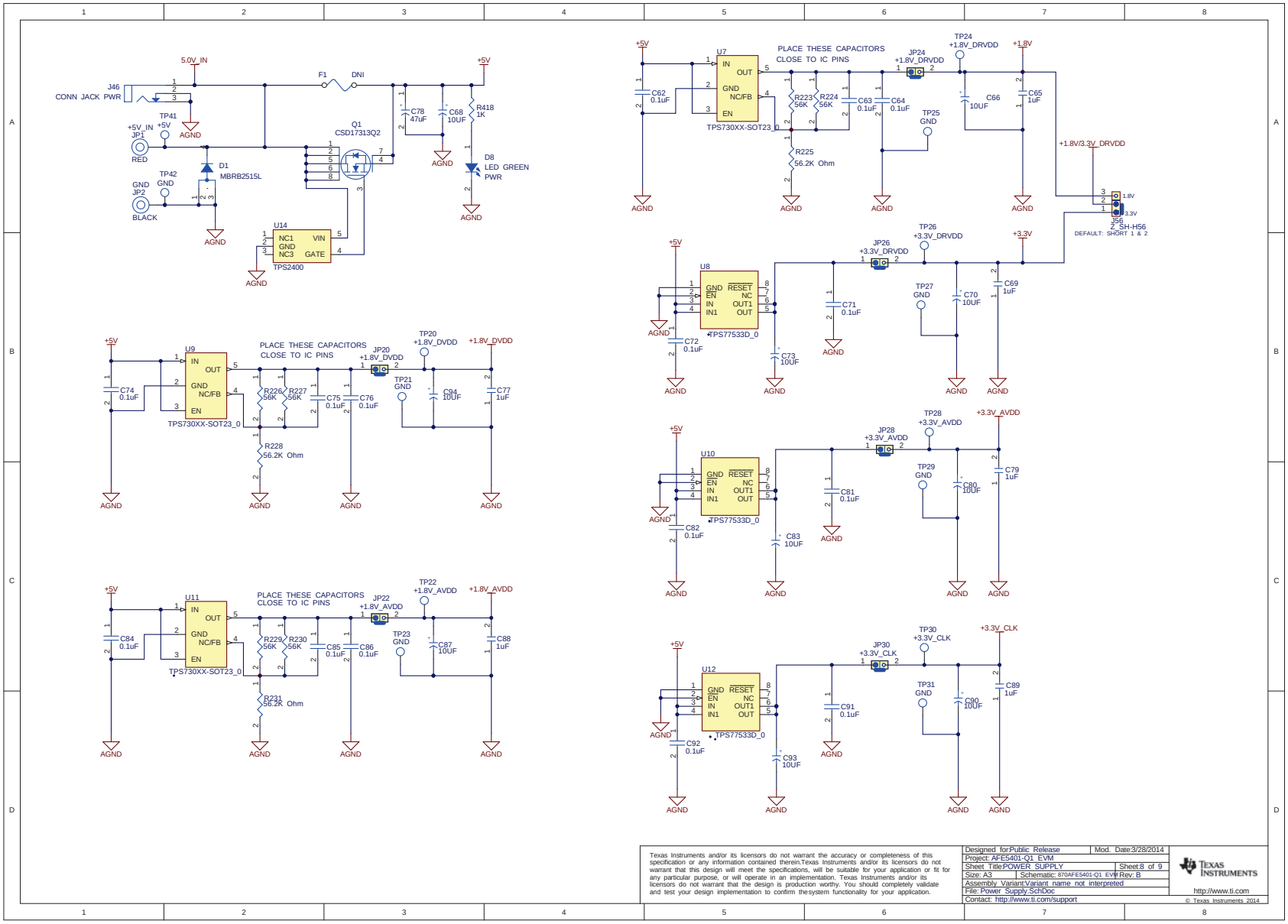


Figure 69. AFE5401-Q1 EVM Schematic Sheet 8

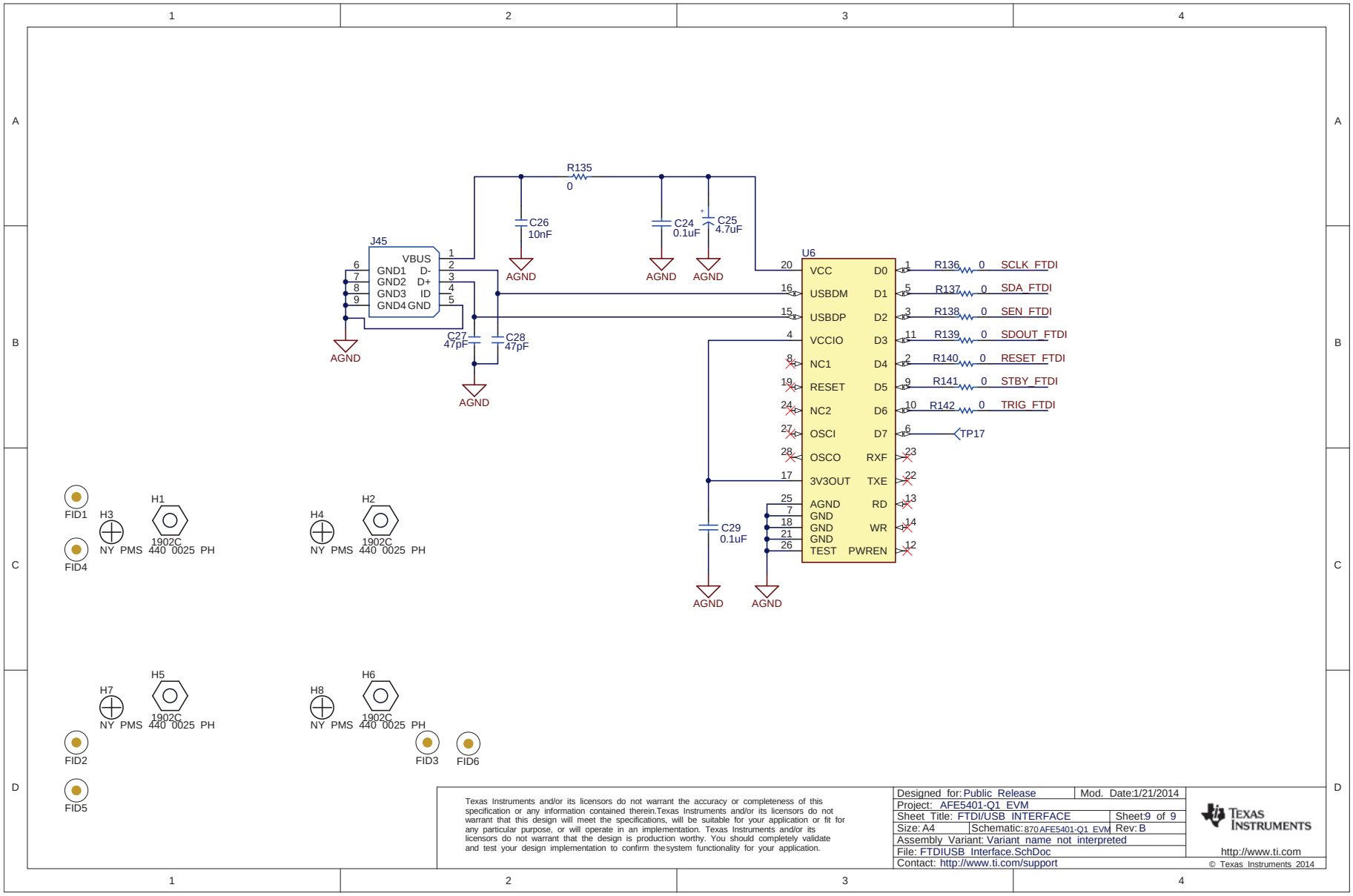


Figure 70. AFE5401-Q1 EVM Schematic Sheet 9

9 AFE5401-Q1 EVM Bill of Materials (BOM)

Table 3 lists the BOM for this EVM.

Table 3. AFE5401-Q1 EVM Bill of Materials

Item	Designator	Description	Manufacturer	PartNumber	QTY
1	C1, C2, C5, C6, C7, C30, C31, C32, C34, C36, C37, C38, C39, C40, C42, C44, C45, C46, C47, C48, C50, C52, C53, C54, C55, C56, C58, C60, C61	CAPACITOR, CERAMIC, 0.1UF, 10%, 16V, SMT0402	AVX	0402YC104KAT2A	29
2	C18, C19, C20, C21, C22, C23, C24, C29	CAPACITOR, CERAMIC, 0.1UF, 10%, 16V, SMT0402	TDK Corporation	C1005X5R1C104K050BA	8
3	C25	CAP TANTALUM 4.7UF 20V 10% SMD	AVX	TAJA475K020RNJ	1
4	C26	CAP 10000PF 50V CERM X7R 0603	MURATA	GRM188R71H103KA01D	1
5	C27, C28	CAP CERAMIC 47PF 50V 0603 SMD	MURATA	GRM1885C1H470JA01D	2
6	C62, C63, C64, C71, C72, C74, C75, C76, C81, C82, C84, C85, C86, C91, C92	CAP CER .10UF 50V X7R 10% 0603	AVX	06035C104JAT2A	15
7	C65, C69, C77, C79, C88, C89	CAP CER 1.0UF 16V X7R 10% 0603	AVX	0603YC105KAT2A	6
8	C66, C68, C70, C73, C80, C83, C87, C90, C93, C94	CAP TANT 10UF 16V 10% 1210	AVX	TAJB106K016RNJ	10
9	C78	CAP TANT 47UF 10V 10% 1210	AVX	TPSB476K010R0250	1
10	D1	DIODE SCHOTTKY 15V 25A D2PAK	ON SEMICONDUCTOR	MBRB2515LT4G	1
11	D8	LED GREEN CLEAR 1206 SMD	LITE-ON Inc	LTST-C150KGKT	1
12	DUT1	AFE5401 Quad Channel Analog Front End	TEXAS INSTRUMENTS	AFE5401	1
13	H1, H2, H5, H6	Standoff, Hex, 0.5"L #4-40 Nylon	KEYSTONE ELECTRONICS	1902C	4
14	H3, H4, H7, H8	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F FASTENER SUPPLY	NY PMS 440 0025 PH	4
15	J3, J30, J48, J49, J50, J51, J52, J53, J54, J55	CONN, SMA, RECEPTACLE STRAIGHT	AMPHENOL	901-144-8RFX	10
16	J4, J5, J8, J26, J27, J28, J29, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J56, J57	JUMPER,3P,.100CC	SULLINS CONNECTOR SOLUTIONS	PBC03SAAN	23
17	J45	CONN RECEPT USB 5POS RT ANG SMD	MOLEX	678038020	1
18	J46	CONN POWERJACK MINI R/A T/H	SWITCHCRAFT	RAPC722X	1
19	JP1	BANANA JACK, 15A, TURRET, RED	Alectron	ST-351A	1
20	JP2	BANANA JACK, 15A, TURRET, BLACK	Alectron	ST-351B	1
21	JP20, JP22, JP24, JP26, JP28, JP30	CONN HEADER 2POS .100" T/H GOLD	SAMTEC	HMTSW-102-07-G-S-.240	6
22	P1	CONNECTOR, MALE, 2.54 MM PITCH, DOUBLE ROW, VERTICAL, 60-PIN, TH, ROHS	SAMTEC	HMTSW-130-07-G-D-240	1
23	Q1	MOSFET N-CH 30V 5A 6SON	TEXAS INSTRUMENTS	CSD17313Q2	1

Table 3. AFE5401-Q1 EVM Bill of Materials (continued)

Item	Designator	Description	Manufacturer	PartNumber	QTY
24	R5, R11, R17, R30, R31, R32, R33, R34, R37, R40, R43, R46, R50, R53, R56, R60, R61, R62, R64, R65, R66, R67, R71, R74, R77, R80, R81, R84, R87, R90, R93, R94, R95, R96, R97, R103, R105, R106, R108, R109, R111, R112, R115, R116, R117, R119, R120, R122, R124, R126, R127, R129, R135, R136, R137, R138, R139, R140, R141, R142, R144, R146, R160, R162, R164, R166, R180, R182, R184, R186, R200, R202, R204, R205, R206, R210, R220, R221, R222, R234, R235, R238, R239, R242, R243, R246, R247, R250, R251, R254, R255, R400, R401, R404, R408, R409, R412, R413, R417	RES, 0 ohm, 5%, 0.063W, 0402	PANASONIC	ERJ-2GE0R00X	99
25	R12, R15, R149, R150, R154, R155, R169, R170, R174, R175, R189, R190, R194, R195, R209, R214, R420	RESISTOR, THICK FILM, 24.9 OHM, 1%, 0.1W, SMT0402	PANASONIC	ERJ-2RKF24R9X	17
26	R102	RESISTOR, THICK FILM, 10K OHM, 1%, 0.1W, SMT0402	PANASONIC	ERJ-2RKF1002X	1
27	R114, R134	RES, 10k ohm, 5%, 0.125W, 0805	PANASONIC	ERJ-6GEYJ103V	2
28	R123	RESISTOR, THICK FILM, 10 OHM, 1%, 0.1W, SMT0603	VISHAY	CRCW060310R0FKEA	1
29	R143, R145, R159, R161, R163, R165, R179, R181, R183, R185, R199, R201, R203, R219	RESISTOR, THICK FILM, 10 OHM, 1%, 0.063W, SMT0402	VISHAY	CRCW040210R0FKED	14
30	R223, R224, R226, R227, R229, R230	RES 56.0K OHM 1/10W 1% 0603 SMD	PANASONIC	ERJ-3EKF5602V	6
31	R225, R228, R231	RES 56.2K OHM 1/10W 1% 0603 SMD	PANASONIC	ERJ-3EKF5622V	3
32	R418	RES 1K OHM 1/10W 1% 0402 SMD	PANASONIC	ERJ-2RKF1001X	1
33	R419	RESISTOR, THICK FILM, 49.9 OHM, 1%, 0.1W, SMT0402	PANASONIC	ERJ-2RKF49R9X	1
34	SW1, SW2	Switch, Push Button, SMD	ALPS	SKRKAEE010	2
35	T1, T3, T4, T5, T6, T7, T8, T10, T11, T13, T14	TRANSFORMER, RF, 75 OHM, 0.4 MHZ TO 800 MHZ, 6-PIN, ROHS	MINI-CIRCUITS	ADT1-1WT	11
36	T9	TRANSFORMER, WIDE BAND RF, SMT	COILCRAFT	WB1010-SMLB	1
37	TP1, TP10, TP12, TP15, TP17, TP21, TP23, TP25, TP27, TP29, TP31, TP42	Testpoint (Black)	KEYSTONE ELECTRONICS	5001	12
38	TP2, TP11, TP18, TP19, TP40	Testpoint (White)	KEYSTONE ELECTRONICS	5002	5
39	TP3, TP4, TP5, TP13, TP14, TP16	Testpoint (Blue)	KEYSTONE ELECTRONICS	5117	6
40	TP6, TP7, TP8, TP9	Testpoint (Yellow)	KEYSTONE ELECTRONICS	5004	4
41	TP20, TP22, TP24, TP26, TP28, TP30, TP41	Testpoint (Red)	KEYSTONE ELECTRONICS	5000	7
42	U2	OSC 25.000 MHZ 3.3V SMD	ECS Inc	ECS-3953M-250-BN-TR	1
43	U3	IC, 16-BIT EDGE TRIGGERED D-TYPE FLIPFLOP, TSSOP-48 ROHS	TEXAS INSTRUMENTS	SN74LVC16374ADGGR	1
44	U4	IC, 16-BIT BUFFER/DRIVER 3-STATE OUTPUTS, TSSOP-48, ROHS	TEXAS INSTRUMENTS	SN74AVC16244DGGR	1
45	U5	IC, SINGLE INVERTER GATE, SOT23-5, DBV	TEXAS INSTRUMENTS	SN74LVC1GU04DBVT	1
46	U6	IC USB TO PARALLEL FIFO 28-SSOP	FTDI	FT245RL	1
47	U7, U9, U11	IC LDO REG 250MA ADJ-V SOT23-5	TEXAS INSTRUMENTS	TPS73201DBVR	3

Table 3. AFE5401-Q1 EVM Bill of Materials (continued)

Item	Designator	Description	Manufacturer	PartNumber	QTY
48	U8, U10, U12	IC 3.3V 500MA LDO REG 8-SOIC	TEXAS INSTRUMENTS	TPS77533D	3
49	U13	IC, SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT, SOT553-5, DRL	TEXAS INSTRUMENTS	SN74LVC1G125DRLR	1
50	U14	IC OVERVOLT PROT CTRLR SOT23-5	TEXAS INSTRUMENTS	TPS2400DBVT	1
51	Z_SH-H1, Z_SH-H4, Z_SH-H5, Z_SH-H8, Z_SH-H26, Z_SH-H27, Z_SH-H28, Z_SH-H29, Z_SH-H31, Z_SH-H32, Z_SH-H33, Z_SH-H34, Z_SH-H35, Z_SH-H36, Z_SH-H37, Z_SH-H38, Z_SH-H39, Z_SH-H40, Z_SH-H41, Z_SH-H42, Z_SH-H43, Z_SH-H44, Z_SH-H56, Z_SH-H57, Z_SH-H58, Z_SH-H59, Z_SH-H60, Z_SH-H61, Z_SH-H62	SHUNT FOR HEADER	SAMTEC	SNT-100-BK-T	29
52	C33, C35, C41, C43, C49, C51, C57, C59	CAPACITOR, SMT0402	-	CAP-SMT0402	0
53	F1	FUSE 2.0A 63V FAST SMD 1206	TE CONNECTIVITY	1206SFF200F/63-2	0
54	J47	CONNECTOR, FPC, STRAIGHT, 0.5 MM PITCH, 36-PIN, SMT, ROHS	MOLEX	52559-3679	0
55	R1, R2	RESISTOR, THICK FILM, 10 OHM, 5%, 0.1W, SMT0402	PANASONIC	ERJ-2GEJ100	0
56	R3, R4, R47, R68, R232, R233, R236, R237, R240, R241, R244, R245, R248, R249, R252, R253, R414	RESISTOR, THICK FILM, 10 OHM, 1%, 0.063W, SMT0402	VISHAY	CRCW040210R0F100	0
57	R13	RESISTOR, THICK FILM, 100 OHM, 5%, 0.1W, SMT0402	PANASONIC	ERJ-2GEJ101	0
58	R14, R147, R148, R151, R152, R153, R156, R157, R158, R167, R168, R171, R172, R173, R176, R177, R178, R187, R188, R191, R192, R193, R196, R197, R198, R207, R208, R211, R212, R213, R216, R217, R218	RESISTOR, SMT0402	-	RES-SMT0402	0
59	R35, R36, R38, R39, R41, R42, R44, R45, R48, R49, R51, R52, R54, R55, R57, R69, R70, R72, R73, R75, R76, R78, R79, R82, R83, R85, R86, R88, R89, R91, R92, R98, R99, R100, R101, R104, R107, R110, R113, R118, R121, R125, R128, R130, R131, R132, R133, R402, R403, R405, R406, R407, R410, R411, R415, R416	RES, 0 ohm, 5%, 0.063W, 0402	PANASONIC	ERJ-2GE0R00X	0
60	R215	RESISTOR, THICK FILM, 24.9 OHM, 1%, 0.1W, SMT0402	PANASONIC	ERJ-2RKF24R9X	0
61	T12	TRANSFORMER, WIDE BAND RF, SMT	COILCRAFT	WB1010-SMLB	0

10 AFE5401-Q1 EVM Layout

As shown in Figure 71, all analog inputs should be differentially and symmetrically routed to differential input pins of the AFE for best performance. CMOS outputs should be kept as short as possible to reduce the trace capacitance which will load the CMOS output buffers. It is recommended to match the lengths of the output traces including DCLK, DSYNC1, and DSYNC2 to eliminate skew and potential incorrect channelization in the receiver.

The device package consists of an exposed pad. In addition to providing a path for heat dissipation, the pad is also internally connected to the analog ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *AQF/SON PCB Attachment* (SLUA271).

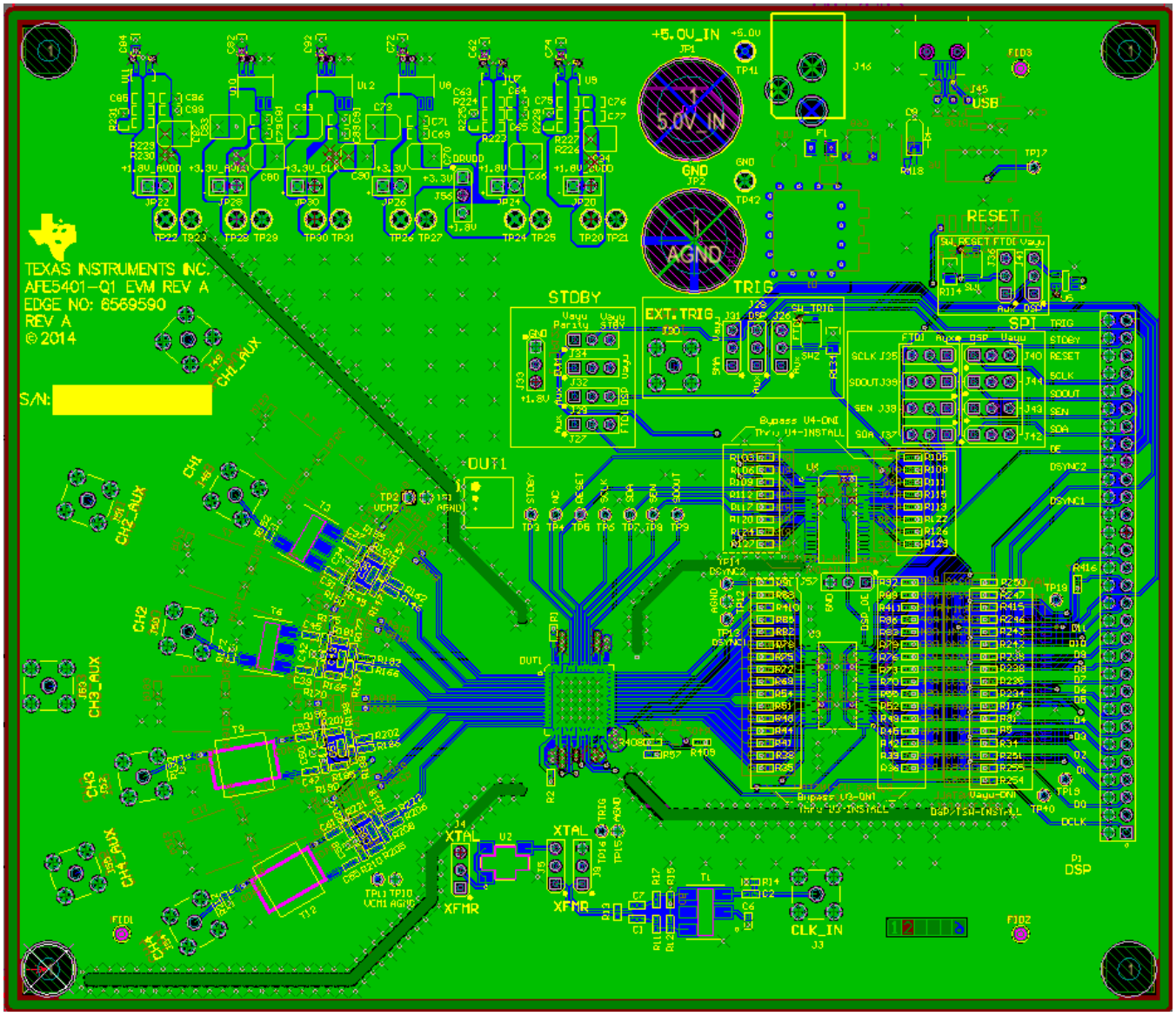


Figure 71. AFE5401-Q1 EVM Layout

Appendix A Blind Capture of RAMP Test Pattern

The simplest capture implementation is one in which no data framing is used (that is, ***DSYNC_EN*** = 0).

1. Perform the following steps as highlighted in Figure 72 and Figure 73.
   (a) Press the ***SW_RST*** button on the *TOP LEVEL SETTINGS* tab.
   (b) Power down all but Channel 1 on the TOP LEVEL SETTINGS tab
   (c) Set ***TEST_PAT_MODE*** to *Full Scale RAMP* on the *DIAGNOSTICS & TEST MODES* tab.

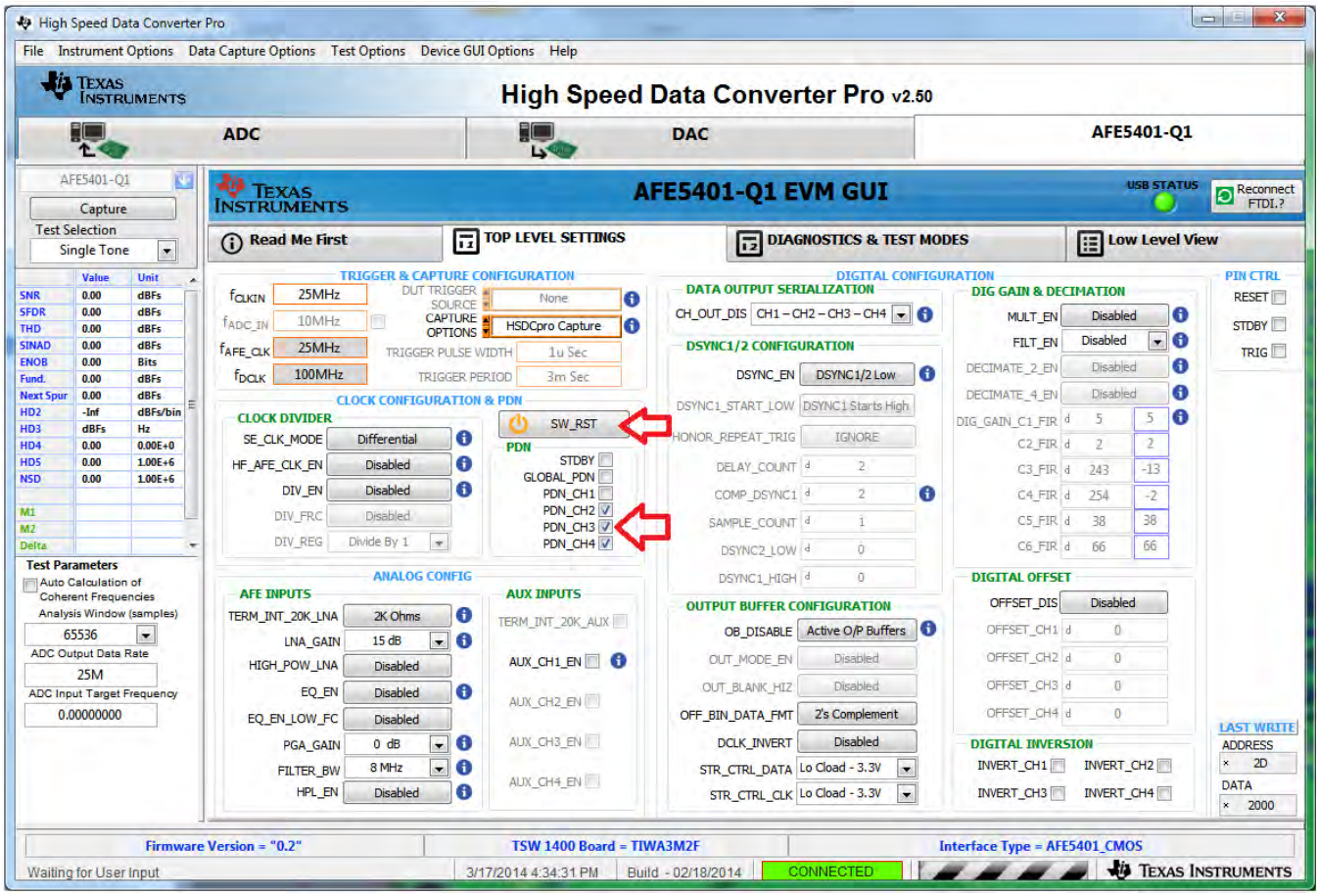


Figure 72. GUI Setup for Blind RAMP Test (a)

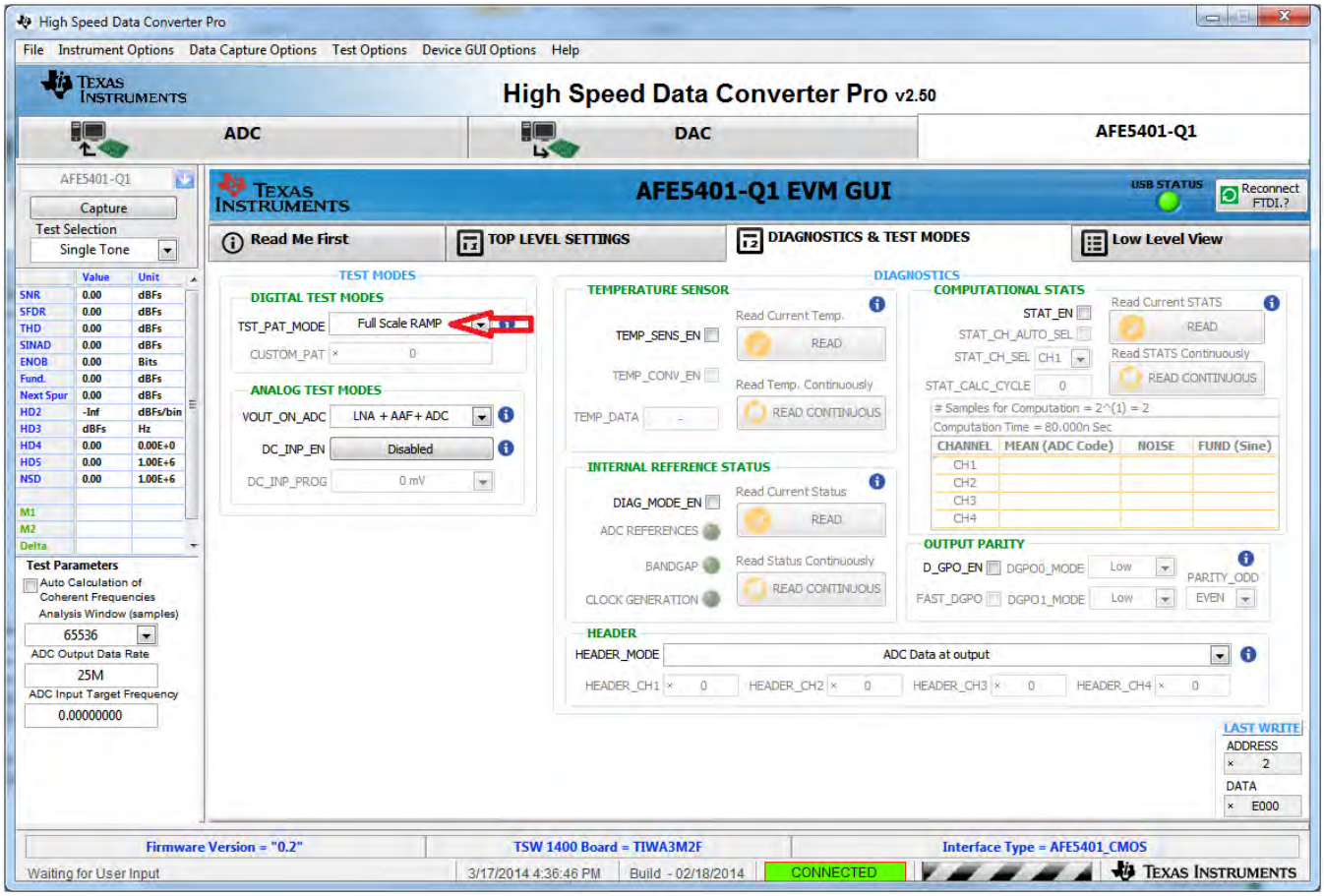


Figure 73. GUI Setup for Blind RAMP Test (b)

2. Capture and view the RAMP by performing the following steps; also illustrated in Figure 74:
   (a) Press the *ADC* tab in *HSDCpro*
   (b) Change the plot type from *Real FFT* to *Codes*
   (c) Press the *Capture* button.

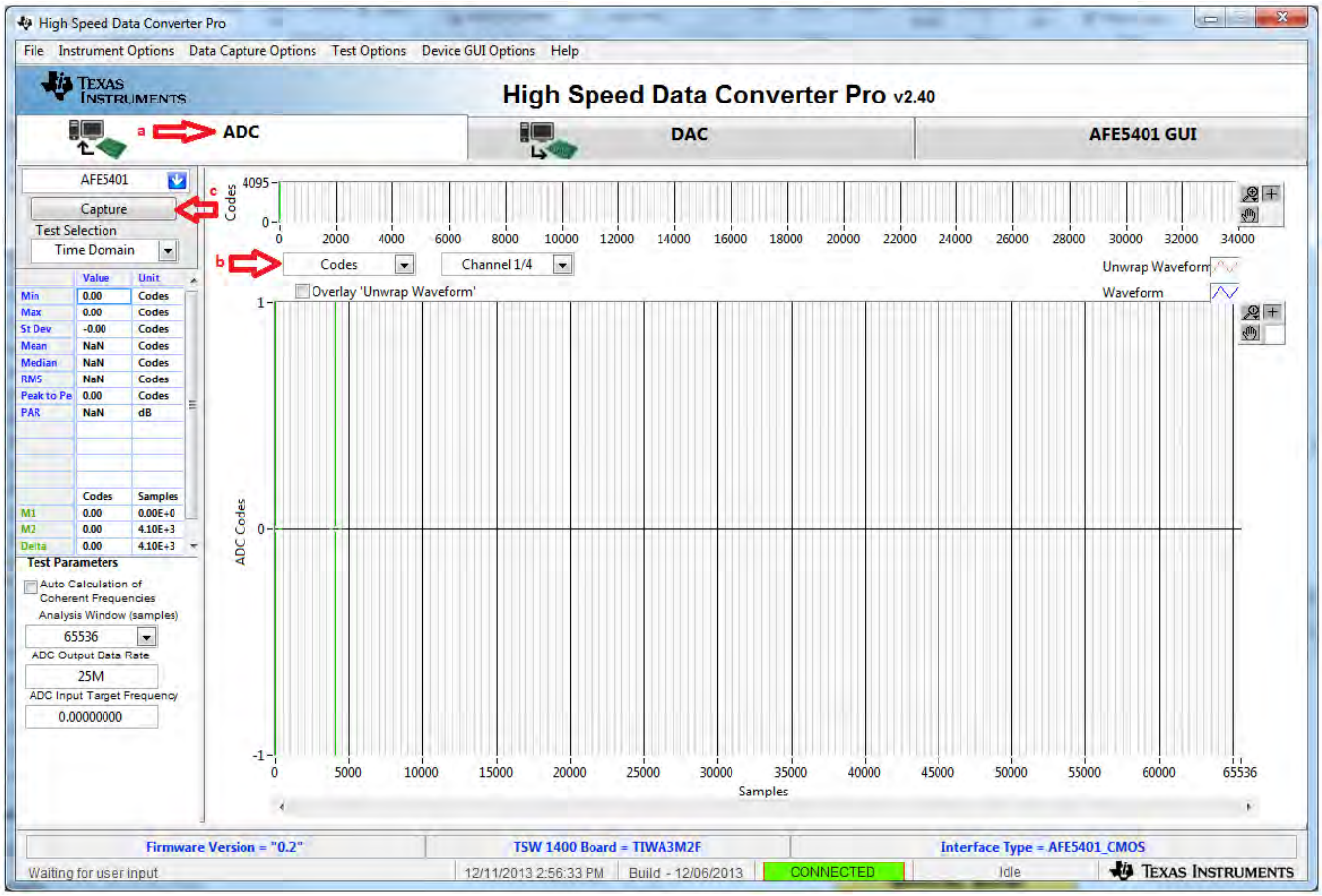


Figure 74. GUI Setup For Blind RAMP Test (c)

3. One might or might not observe the RAMP waveform in *Channel1/4* of *HSDCpro*. This is due to the fact that the output consists of four channels of data which are serialized. Without any framing, through the use of DYSNC1 and DSYNC2 output signals, the FPGA has no way of determining what sample belongs to which channels. It only knows that every 4th sample (if 4x serialization is used) belongs to the same channel. Therefore, the capturing RAMP waveform appears randomly on one of the four channels. By recapturing multiple times, the 'law of averages' mandates that the data sent from Channel 1 of the DUT eventually is displayed as channel 1 by the FPGA firmware.

Appendix B FPGA Triggered Capture of a RAMP Test Pattern

As stated in the datasheet, when a rising edge is detected on the **TRIG** pin of the AFE5401-Q1, the DSYNC1/2 output signals are generated as defined by several SPI registers. As described in Section 7.2.1, there are two methods that the FPGA uses to capture and frame data:

(a) N sample capture from first rising edge of the DSYNC2 signal where N is set in the *HSDCpro* GUI.

(b) N sample capture during active high state of the DSYNC2 signal where N is set in the *HSDCpro* GUI.

Each of these methods are explored here using a RAMP test pattern.

Capture on Rising Edge of DSYNC2

The receiver implementation is designed to begin data capture on the rising edge of a DSYNC2 output signal. From the *TOP LEVEL SETTINGS* tab of the *AFE5401-Q1 GUI*, perform the following procedures as shown in Figure 75:

(a) Click the ***SW_RST*** button

(b) Set ***DSYNC_EN*** to *DSYNC1/2* Active

(c) Set ***DUT TRIGGER SOURCE*** to *FPGA on TSW1400*

(d) Set ***CAPTURE OPTIONS*** to *DSYNC2 Rising Edge*

(e) Set ***TRIGGER PERIOD*** to *6m Sec*

(f) Set ***SAMPLE_COUNT*** to *70,000*

(g) Check ***PDN_CHx*** for x=2,3,4

(h) Set ***TST_PAT_MODE*** to *Full Scale RAMP* on the *DIAGNOSTICS & TEST MODES* tab of the GUI (not shown in Figure 75).

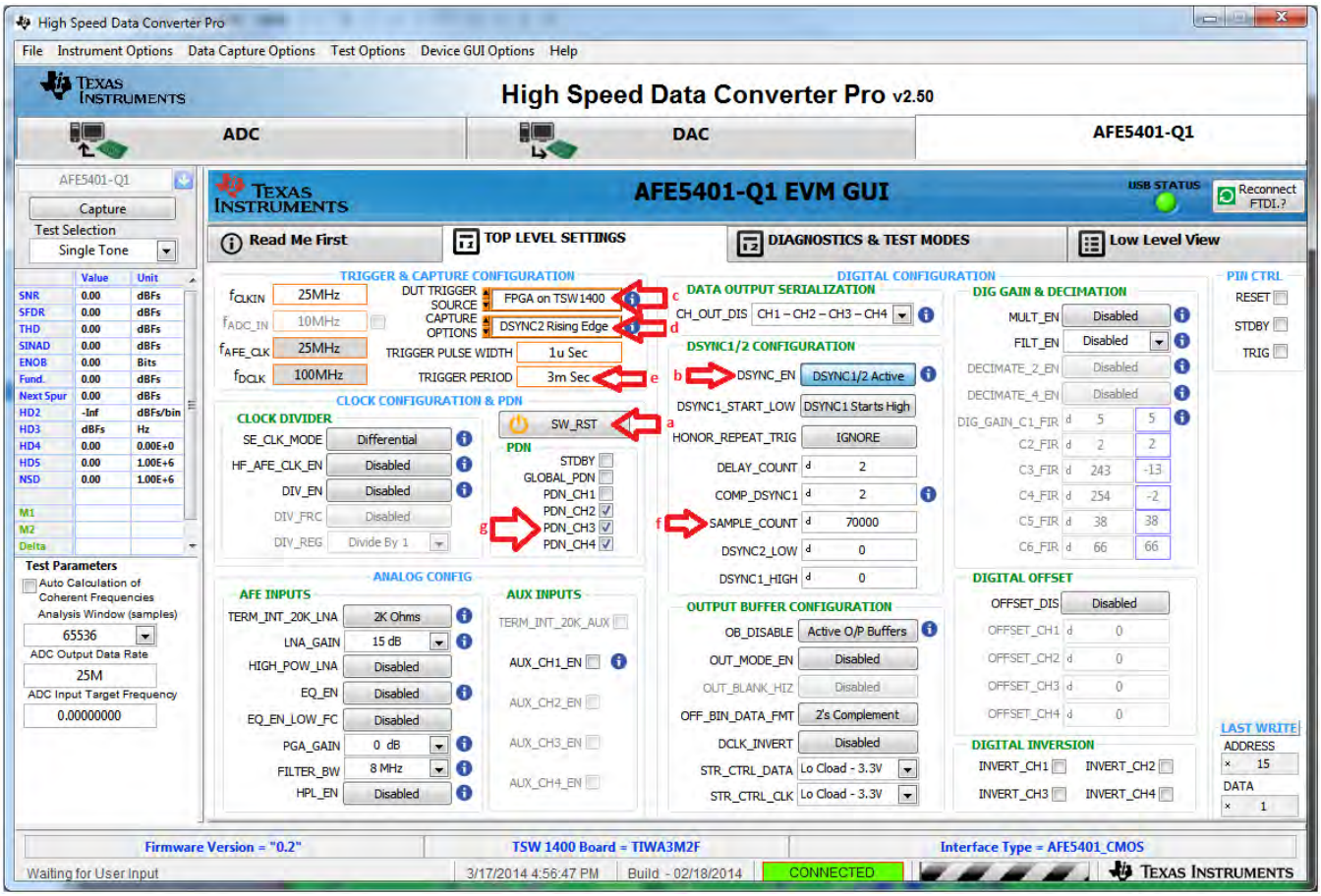


Figure 75. FPGA DSYNC2 Rising Edge Triggered RAMP Capture (a)

From the *ADC* tab of the GUI press the *Capture* button to see the captured RAMP function. Because *DSYNC_EN* is enabled and a trigger is being provided to the AFE5401-Q1 TRIG pin, the DYSNC1 and DSYNC2 outputs are generated. The FPGA firmware uses the DSYNC2 rising edge to 'mark' the start of a serialization. Therefore, the position of the channel data is known and can be displayed in its proper channel within *HSDCpro*, whereas, this was a random process when *DSYNC_EN* was disabled. Figure 76 illustrates this by displaying channels 1 and 2 simultaneously by using the *Test Options* drop-down menu in *HSDCpro*.

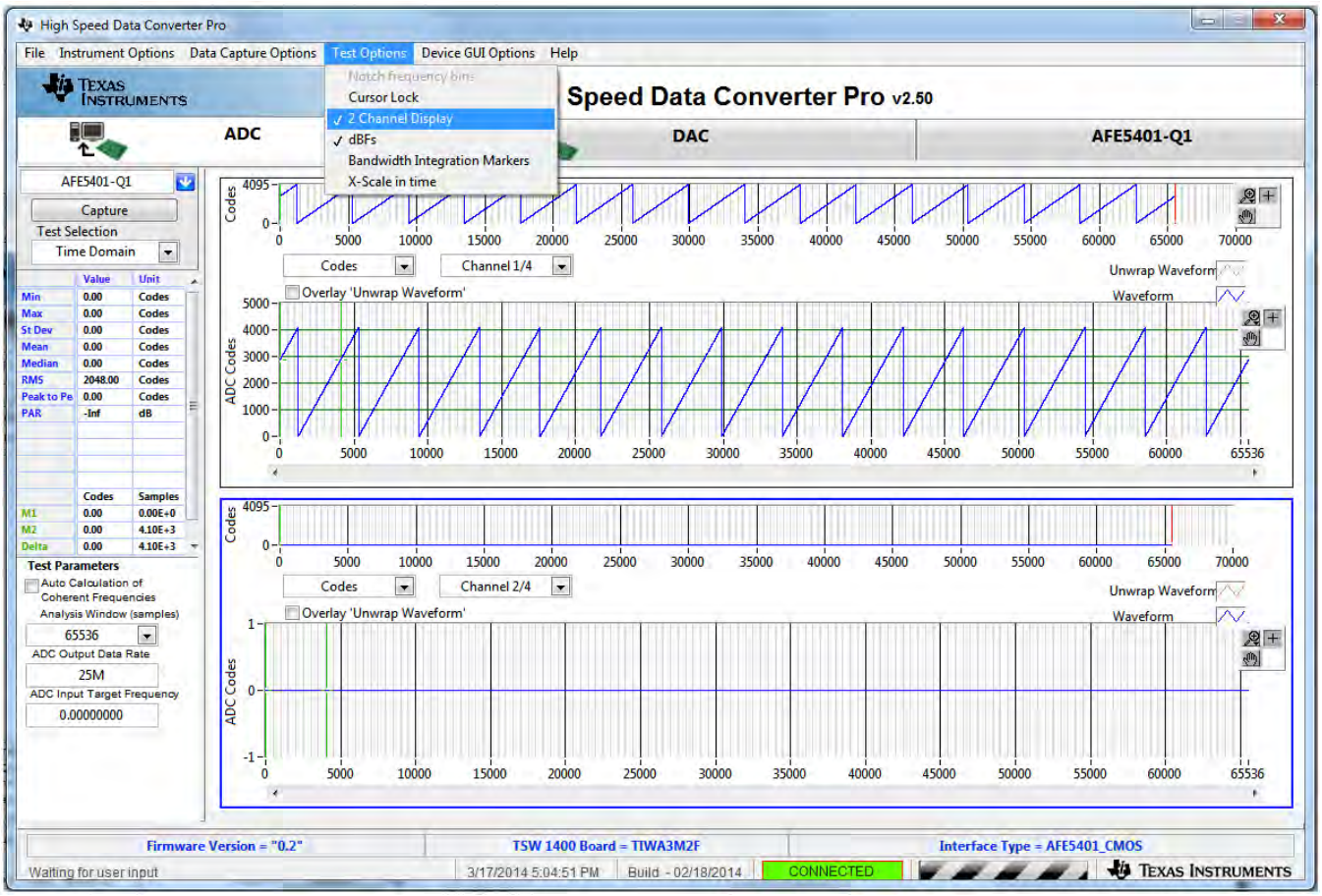


Figure 76. FPGA DSYNC2 Rising Edge Triggered RAMP Capture (b)

The RAMP captured in Figure 76 shows no discontinuities because ***OUT_MODE_EN*** is disabled. With ***OUT_MODE_EN*** enabled and ***OUT_BLANK_HIZ*** enabled there are two mechanisms that would cause a discontinuity: (1) if SAMPLE_COUNT is less than the number of samples being captured and displayed in *HSDCpro*, default set to 65536 samples or (2) if a trigger occurs before the capture of the 65k samples. Figure 77 shows the GUI setup with ***OUT_MODE_EN*** and ***OUT_BLANK_HIZ*** enabled with the ***SAMPLE_COUNT*** set to 20,000 samples.

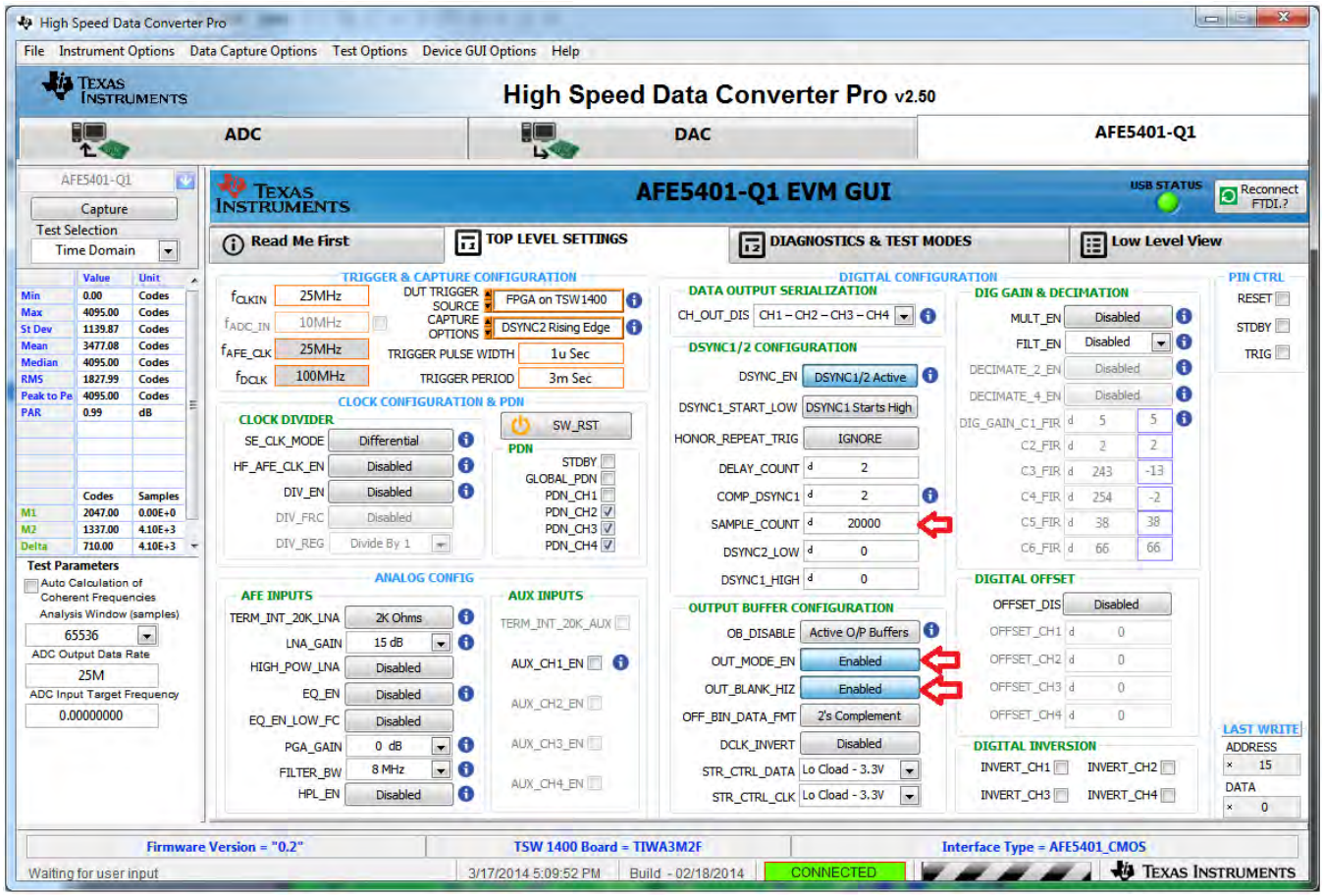


Figure 77. FPGA DSYNC2 Rising Edge Triggered RAMP Capture (c)

Figure 78 shows that once the ***SAMPLE_COUNT*** of *20,000* is achieved, the output is blanked for all subsequent samples, at least until the next **TRIG** event is encountered, thus, generating another DSYNC2 rising edge on which to capture.

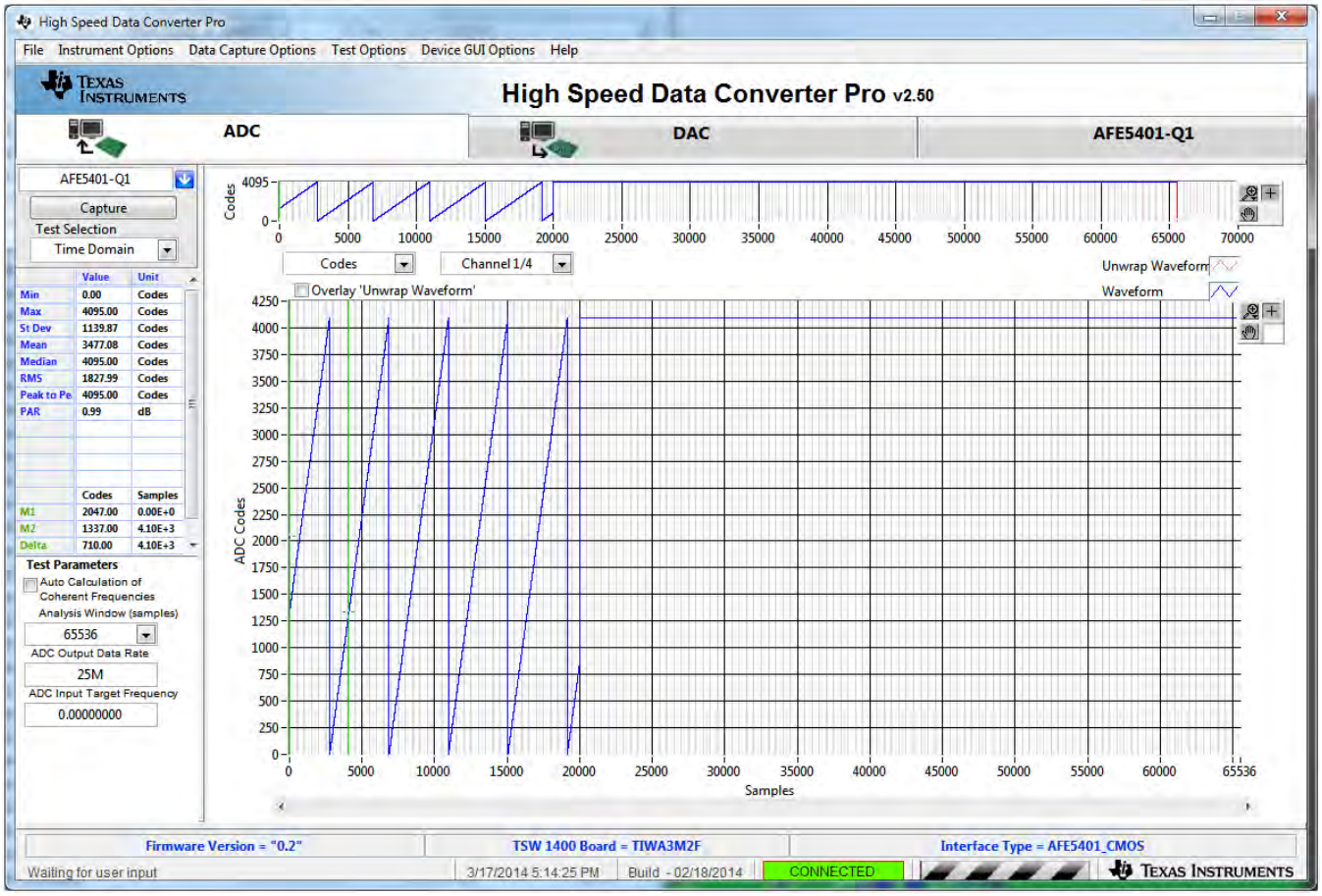


Figure 78. FPGA DSYNC2 Rising Edge Triggered RAMP Capture (d)

By changing the trigger period to ~500 µs, which equates to 12,500 samples/channel for a sampling frequency of 25MSPS, one can see how the *BLANKING_PHASE* ends and another *SAMPLE_PHASE* begins as shown in Figure 79 and Figure 80.

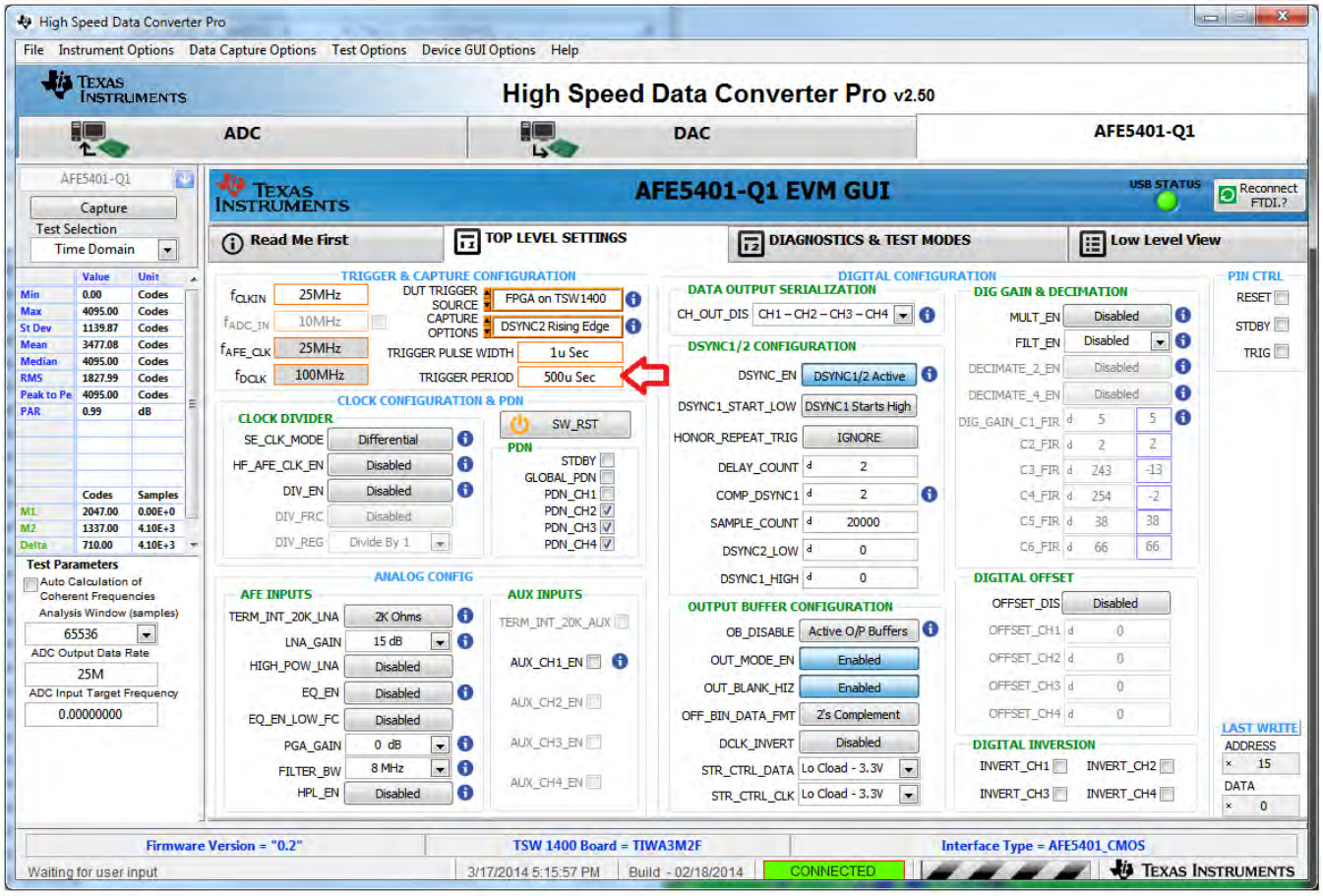


Figure 79. FPGA DSYNC2 Rising Edge Triggered RAMP Capture (e)

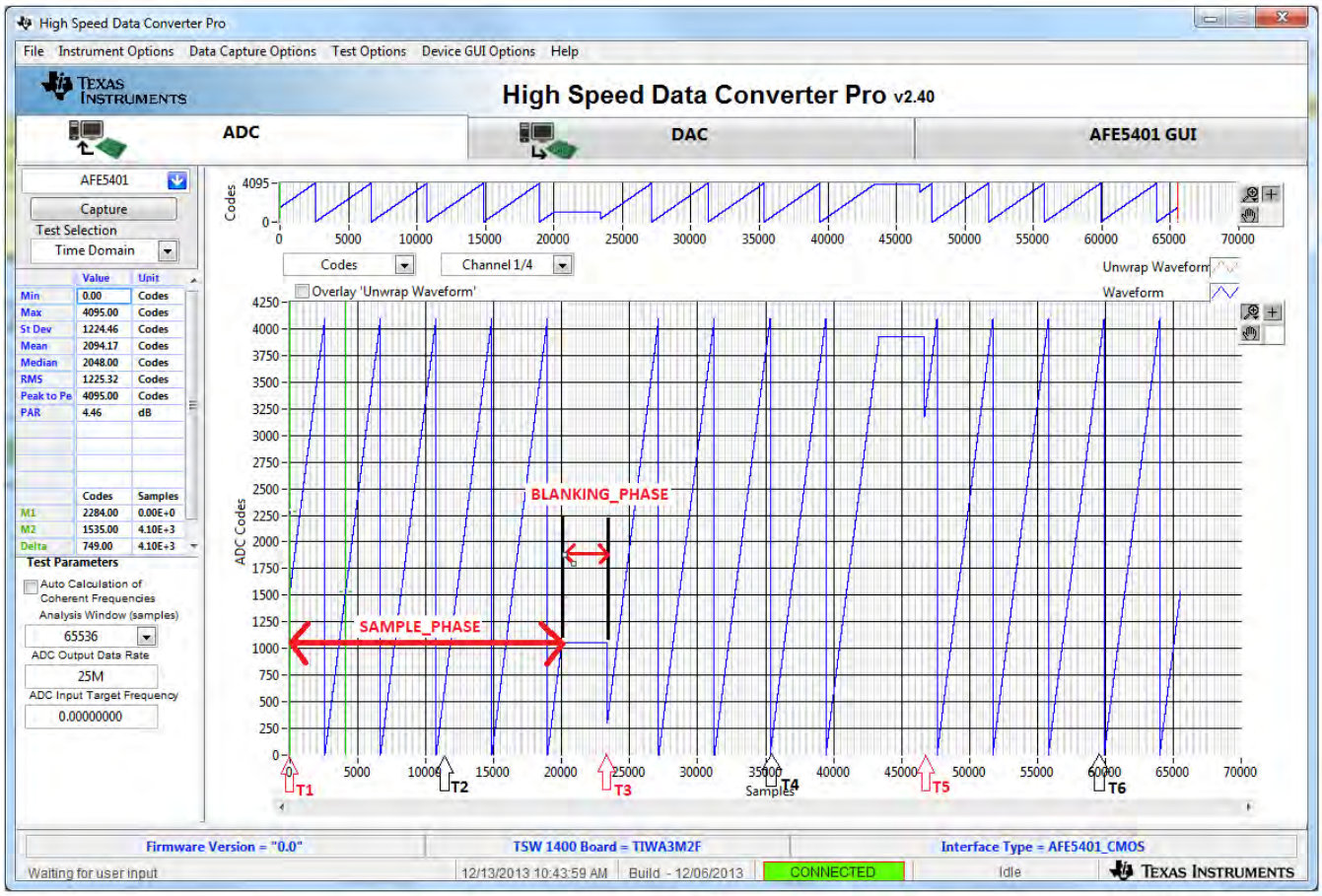


Figure 80. FPGA DSYNC2 Rising Edge Triggered RAMP Capture (f)

The approximate locations of the triggers are shown on the x-axis of Figure 80. Those triggers colored in BLACK are ones that are ignored because they occur during an active *SAMPLE_PHASE*. Those triggers colored RED invoke a new *SAMPLE_PHASE* and end the BLANKING_PHASE.

Capture on DSYNC2 Active High

This receiver implementation is designed to capture data only during the active high state of the DSYNC2 output signal. With the GUI in the same state as that shown in Figure 77, with the exception of ***CAPTURE OPTIONS*** now set to *DSYNC2 Active High*, a capture displayed in Figure 81 illustrates the *BLANKING PHASE* has been eliminated. Discontinuities in the captured waveform at multiples of the SAMPLE_COUNT correspond to the time when the DSYNC2 output signal goes low and when the subsequent DSYNC2 signal (generated from the subsequent trigger) goes high. With this implementation the ***OUT_MODE_EN*** and ***OUT_BLANK_HIZ*** controls become obsolete as the data during this time is ignored by the receiver.

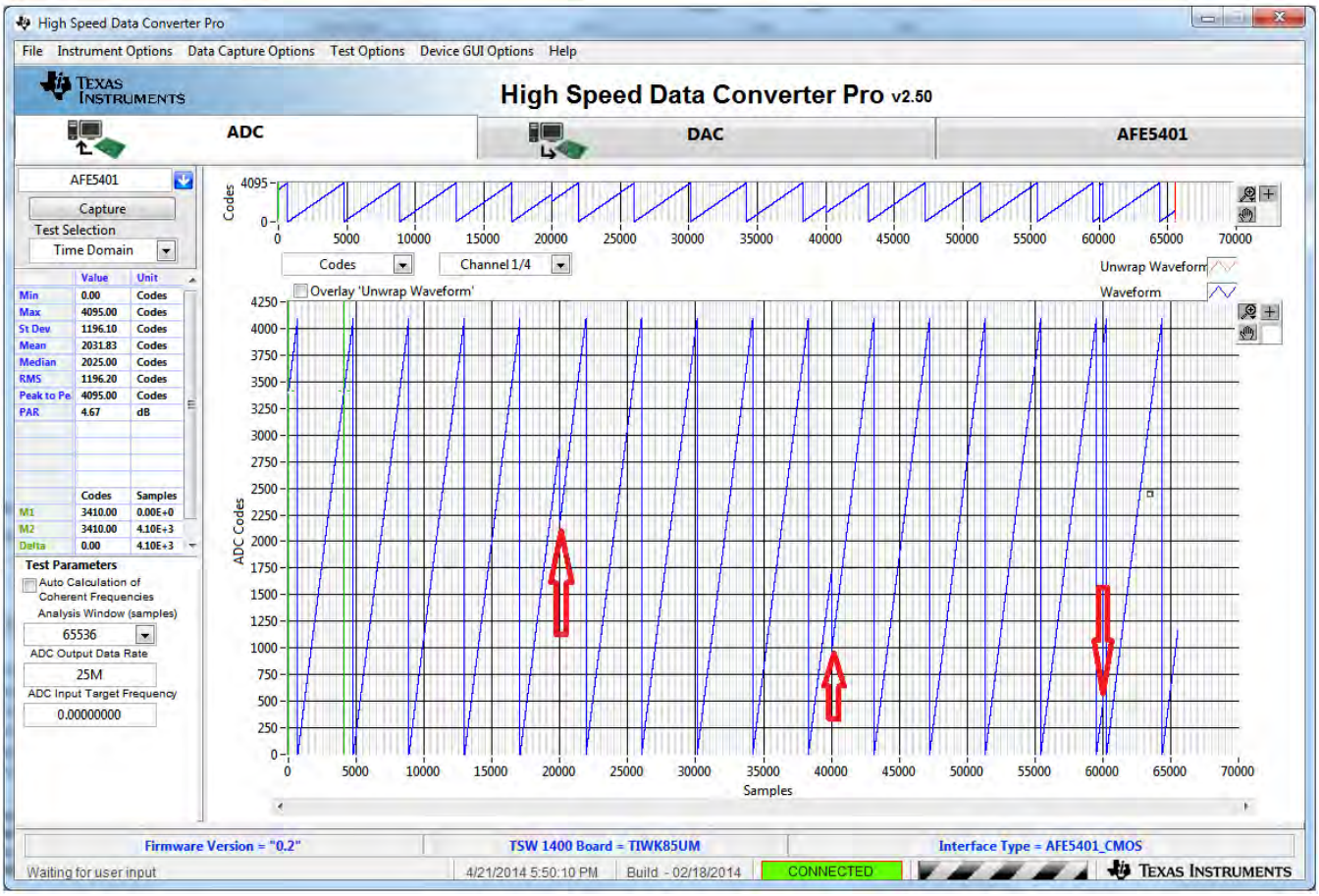


Figure 81. FPGA DSYNC2 Active High Triggered RAMP Capture (g)

Revision History

Changes from Original (March 2014) to A Revision	Page
• Changed revision information regarding **High Speed Data Converter Pro GUI Installer** to include only revision J or higher	5
• Changed destination directory instruction - the default directory must be used. Added a **NOTE:** regarding same issue.	6
• Changed destination directory instruction - the default directory must be used. Added a **NOTE:** regarding same issue.	11

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
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