Errata

MSPM0L222x, MSPM0L122x Microcontrollers

ABSTRACT

This document describes the known exceptions to the functional specifications (advisories).

Note

This errata document is for the pre-production version of the MSPM0L222x and MSPM0L122x MCUs. Erratas are subject to change at the time of final release.

ADVANCE INFORMATION

Table of Contents

Trademarks

1 Functional Advisories

Advisories that affect the device's operation, function, or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev X
ADC_ERR_02	✓
ADC_ERR_06	✓
COMP_ERR_03	✓
I2C_ERR_01	✓
I2C_ERR_03	✓
I2C_ERR_04	✓
LCD_ERR_01	✓
LFSS_ERR_01	✓
LFSS_ERR_02	✓
RTC_A_ERR_01	✓
SPI_ERR_03	✓
SRAM_ERR_01	✓
SYSOSC_ERR_01	✓
UART_ERR_02	✓
VREF_ERR_02	✓

2 Preprogrammed Software Advisories

Advisories that affect factory-programmed software.

✓ The check mark indicates that the issue is present in the specified revision.

3 Debug Only Advisories

Advisories that affect only debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev X
DEBUGSS_ERR_01	✓

4 Fixed by Compiler Advisories

Advisories that are resolved by compiler workaround. Refer to each advisory for the IDE and compiler versions with a workaround.

✓ The check mark indicates that the issue is present in the specified revision.

5 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

Support tool naming prefixes:

X: Development-support product that has not yet completed Texas Instruments internal qualification testing.

null: Fully-qualified development-support product.

XMS devices and X development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format.

5.1 Device Symbolization and Revision Identification

The package diagrams below indicate the package symbolization scheme, and Table 5-1 defines the device revision to version ID mapping.

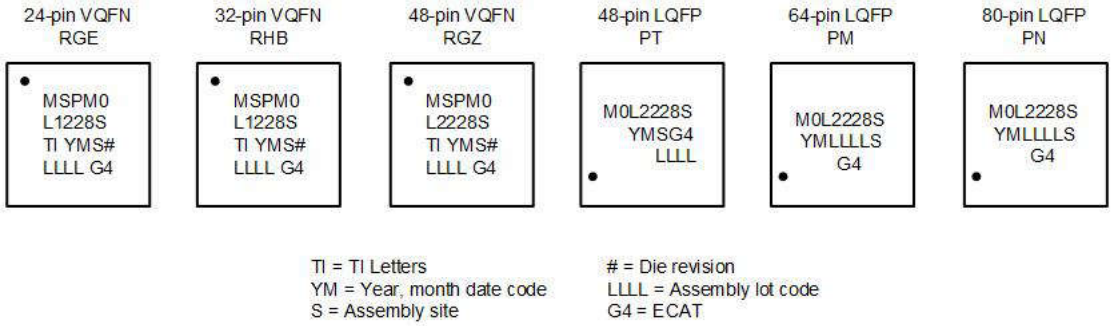

Figure 5-1. Package Symbolization

Table 5-1. Die Revisions

Revision Letter (package marking)	Version (in the device factory constants memory)
X	1

The revision letter indicates the product hardware revision. Advisories in this document are marked as applicable or not applicable for a given device based on the revision letter. This letter maps to an integer stored in the memory of the device, which can be used to look up the revision using application software or a connected debug probe.

ADVANCE INFORMATION

6 Advisory Descriptions

ADC_ERR_02 *ADC does not release the fast clock request in between periodical triggers*

Revisions Affected

Rev X

Details

When the ADC is set up in repeat mode and triggered periodically via the event fabric, it does not release its fast clock request in between triggers. IF so, the ADC will hold the clock request AND consume extra power.

Workaround

Configuring the ADC in single mode (run to completion with ADC disabling at end of channel/sequence), AND THEN using a software interrupt at the end of the ADC sequence to re-enable the ADC to wait for the next trigger.

ADC_ERR_06 *ADC Output code jumps degrading DNL/INL specification*

Revisions Affected

Rev X

Details

The ADC may have errors at a rate as high as 1 in 2M conversions in 12-bit mode. When a conversion error occurs, it will be a significant random jump in the digital output of the ADC without a corresponding change in the ADC input voltage. The magnitude of this jump is larger near major transitions in the bit values of the ADC result (more bits transitioning from 1->0, or 0->1), and largest around midscale (2048 or 0x800).

Depending on the application needs the best workaround may vary, but the following workarounds in software are proposed. Selection of the best workaround is left to the judgment of the system designer.

Workaround 1

Upon ADC result outside of application threshold (via ADC Window Comparator or software thresholding), trigger or wait for another ADC result before making critical system decisions

Workaround 2

During post-processing, discard ADC values which are sufficiently far from the median or expected value. The expected value should be based on the average of real samples taken in the system, and the threshold for rejection should be based on the magnitude of the measured system noise.

Workaround 3

Use ADC sample averaging to minimize the effect of the results of any single incorrect conversion.

COMP_ERR_03 *COMP hysteresis features are non-functional when using input exchange feature*

Revisions Affected

Rev X

Description

When using hysteresis features of the COMP module, and exchanging the inputs of the COMP (COMPx.CTL1.EXCH = 1), the COMP module becomes unstable.

Workaround

Do not apply internal hysteresis methods when utilizing COMP module in input exchange feature.

DEBUGSS_ERR_01 *Debugger reads of SRAM ECC/Parity codes return incorrect values*

Revisions Affected

Rev X

Details

A Debugger read of the SRAM ECC/Parity codes aperture (starting at 0x2030.0000) can return incorrect values.

Workaround

Do not rely on debugger reads of the ECC/Parity codes aperture to compute or verify expected parity/ECC codes versus observed codes. Instead, use CPU software code to perform ECC/Parity code reads and verification.

I2C_ERR_01 *I2C module may hold the SDA line in SBMUS mode when an SMBUS quick command is issued*

Revisions Affected

Rev X

Details

When the I2C module is target mode and configured for SBMUS, IF the bus controller issues an SMBUS quick command addressed to the device (an I2C START condition followed by a 7-bit address, 1-bit R/W signal, 1-bit ACK, and an I2C STOP condition) with the R/W bit set to read, THEN the I2C module may attempt to pull the SDA line low at the same time that the bus controller is attempting to signal the I2C STOP condition, preventing the STOP condition from completing successfully.

Workaround

Load data into the I2C module transmit FIFO with the MSB set to 1 before the address ACK is completed to prevent the I2C module from driving the SDA line low. This will allow the bus controller to issue the STOP condition successfully and complete the SMBUS quick command.

I2C_ERR_03 *I2C peripheral mode cannot wake up device when sourced from MFCLK*

Revisions Affected

Rev X

Description

IF I2C module is configured in peripheral mode
AND I2C is clocked from MFCLK (Middle Frequency Clock)
AND device is placed in STOP2 or STANDBY0/1 power modes,
THEN I2C fails to wakeup the device when receiving data.

Workaround

Set I2C to be clocked by BUSCLK instead of MFCLK, if needing low power wakeup upon receiving data in I2C peripheral mode.

I2C_ERR_04 ***When SCL is low and SDA is high the Target I2C is not able to release the stretch***

Revisions Affected

Rev X

Details

When the device is in IDLE mode and the SCL is pulled low with the clock stretching enabled the SCL is not able to recover.

By default, clock stretching is enabled (SWUEN bit) and when the controller has released SCL, the Target is unable to release the SCL line, driving SCL to 0 continuously.

Workaround

Disable SWUEN

LCD_ERR_01 ***Increased time to achieve low-power mode spec when LCD module is off.***

Revisions Affected

Rev X

Details

Increased time to achieve data sheet I_{DD} current specification for low-power modes when LCD module is off.

Workaround

Turn on LCD module for standby mode to quickly achieve accurate I_{DD} current draw.

No workaround for shutdown mode.

LFSS_ERR_01 ***Increased VBAT current when VDD is less than VBAT***

Revisions Affected

Rev X

Details

When VBAT is greater than VDD increased current is drawn through VBAT.

Workaround

No workaround. VDD must be greater than VBAT to maintain low VBAT current.

LFSS_ERR_02 ***VBAT current increased when using LFXT and IWDT***

Revisions Affected

Rev X

Details

VBAT caurrent is significantly increased when IWDT is enabled with LFXT as the clock source for LFSS.

Workaround

Do not run IWDT and LFXT at the same time.

RTC_A_ERR_01 ***First interrupt coming from Pre-Scaler 2 comes 2 seconds earlier***

Revisions Affected

Rev X

ADVANCE INFORMATION

RTC_A_ERR_01
(continued)

First interrupt coming from Pre-Scaler 2 comes 2 seconds earlier

Details

The first interrupt and only the first coming from the prescaler 2 will come 2 seconds earlier than configured for. Subsequent interrupts will have the correct time difference.

For example, when configured for 4s, the interrupts will appear at 2s, 6s, 10s, etc. If configured for 8s the interrupts will appear at 6s, 14s, 22s, etc. If configured for 16s the interrupts will appear at 14s, 30s, 46s, etc.

Workaround

Compensate for the 2 second early triggering when designing your application.

SRAM_ERR_01	***Mixing No-ECC/Parity aperture and ECC aperture accesses from CPU/DMA can lead to functional errors***
Revisions Affected	Rev X
Details	If CPU access are configured to use the No-ECC/Parity aperture and DMA to use the ECC aperture, it may lead to intermittent faults.
Workaround	Do not mix and match No-ECC/Parity/ECC aperture accesses between CPU and DMA. Use the same type of aperture for both CPU and DMA accesses. If a safety mechanism requires injecting faults, then avoid using the DMA concurrently while this safety diagnostic is being exercised by the CPU software.

SPI_ERR_03	***When configured as peripheral for a multi-peripheral application, received data will have a right shift on communications after the first.***
Revisions Affected	Rev X
Details	When the MCU is set as peripheral: In multi-peripheral scenario, SPI controller first communicates with peripheral0 and then communicates with peripheral1. After finishing communication with peripheral1, the controller again communicates with peripheral0. During the second communication with peripheral0, received data of peripheral0 will have a right shift in the first frame. The peripheral0 is getting data as 0x3B when the controller sent data 0x76.
Workaround	To support multi peripheral scenario, CSCLR needs to be enabled at peripheral end to reset the RX and TX bit counters.

ADVANCE INFORMATION

SYSOSC_ERR_01 ***MFCLK drift when using SYSOSC FCL together with STOP1 mode***

Revisions Affected

Rev X

Details

When MFCLK is enabled AND SYSOSC is using the frequency correction loop (FCL) mode AND the STOP1 low power operating mode is used, THEN the MFCLK may drift by 2 cycles when SYSOSC shifts from 4MHz back to 32MHz (either upon exit from STOP1 to RUN mode or upon an asynchronous fast clock request that forces SYSOSC to 32MHz).

Workaround1

Use STOP0 mode instead of STOP1 mode. There is no MFCLK drift when STOP0 mode is used.

Workaround2

Do not use SYSOSC in the FCL mode (leave FCL disabled) when using STOP1.

UART_ERR_02 ***UART End of Transmission interrupt not set when only TXE is enabled***

Revisions Affected

Rev X

Details

UART End of transmission interrupt(EOT) is not setting when device is set for transmit only (CTL0.TXE = 1). EOT is setting only when both CTL0.TXE and CTL0.RXE are enabled.

Workaround

Set both CTL0.TXE and CTL0.RXE. You do not need to assign a pin to be the UART receive pin.

VREF_ERR_02 ***Vref Module will turn off when in standby mode when COMP is also active***

Revisions Affected

Rev X

Details

When using the COMP and internal VREF in STANDBY mode, the VREF module will turn off.

Workaround

Use COMP and internal VREF in STOP2 Mode.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2024	*	Initial Release

ADVANCE INFORMATION

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265