Application Report
SLEA016 - October 2003

TVP5146 SCART and OSD

HPA Digital Audio Video

ABSTRACT

The TVP5146 video decoder provides support for a SCART interface, which is commonly used in the European market to provide synchronized composite and component video simultaneously. Various fast switching and overlay options are available, including digital RGB overlay. The various overlay modes are addressed along with the TVP5146 hardware and software setup requirements.

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1 Introduction

The TVP5146 offers a SCART mode of operation for simultaneous hookup of composite video and analog RGB component inputs. The SCART interface, commonly used in the European market, carries synchronous composite video and analog RGB video on the same interface, with the composite video (CVBS) serving as the timing source for both. Sync signals are typically not present on the analog RGB signals. A fast-switch signal may be present on the interface for control of switching between the input sources. The FSS/GPIO input terminal of the TVP5146 can be used to switch actively between the CVBS and RGB inputs. The analog RGB inputs must be synchronous to CVBS, because all TVP5146 internal timing and sampling is derived from this composite input signal.

Support for digital RGB overlay is also provided through the use of three digital RGB input terminals and the FSO/GPIO fast-switch input terminal of the TVP5146. Eight colors of digital RGB can be overlaid on a composite, S-video, or component input source. As with the SCART analog overlay, the digital RGB must be synchronous with the input source. Digital RGB overlay is only available when a 10-bit ITU-R BT.656 digital output format is used.

Both SCART and digital overlay modes can be used for on-screen RGB graphics or picture-in picture applications. The FSS/GPIO input terminal serves as the fast switch for SCART operation, while the FSO/GPIO terminal serves as the fast switch for digital overlay operations. Four delay controls are provided for adjusting timing between input sources and timing between fast switch inputs and the input sources. Only slight internal delay adjustments are possible, so coarse positioning must be controlled by the OSD source. Figure 1 shows a block diagram of the fast switches and delay controls. The FSS/GPIO input controls SCART switching, while the FSO/GPIO input controls digital overlay switching. Table 1 shows the overlay modes that are supported with the I^2C fast-switch control register (28h). The parentheses in the table entries help define the priority of the overlay. Detailed descriptions of the I^2C registers related to SCART and overlay options are shown in Appendix A.

Note: All TVP5146 digital inputs are 3.3-V compliant, so care should be taken not to exceed these levels on the digital RGB and fast switch input terminals. This may require signal attenuation depending on the application and devices used. Resistor dividers or transistor based level shifters should work in most cases.

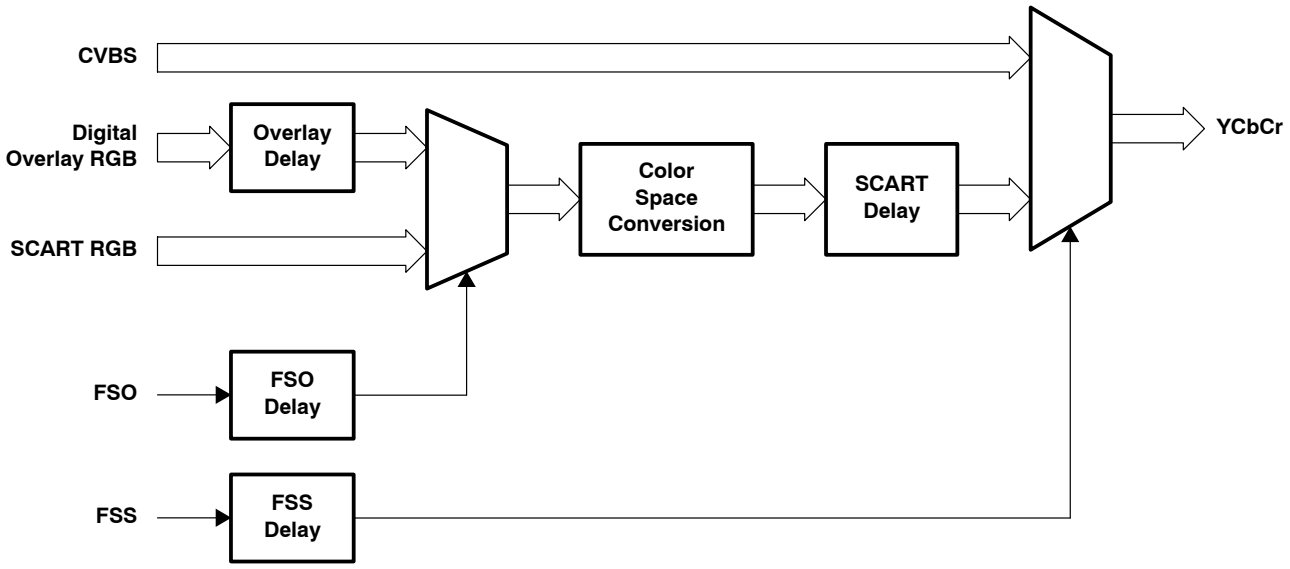


Figure 1. Fast-Switch Control of SCART and Digital Overlay

Table 1. Supported Overlay Modes (I^2C Register 28h)

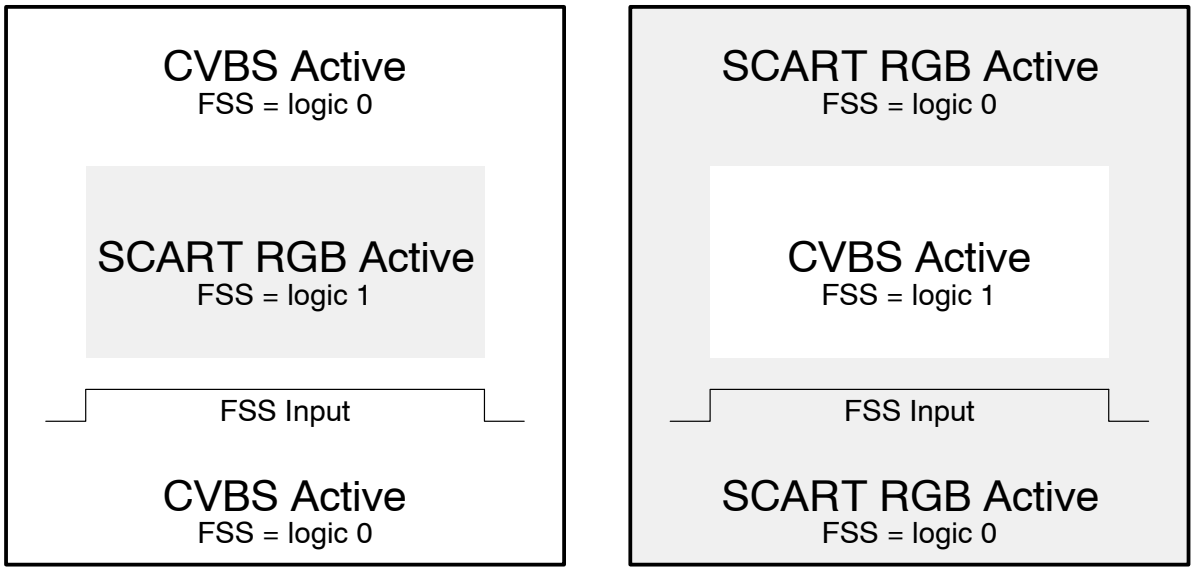
Modes	Description
000	CVBS ←→ SCART
001	CVBS, S_VIDEO ←→ Digital overlay
010	Component ←→ Digital overlay
011	(CVBS ←→ SCART) ←→ Digital overlay
100	(CVBS ←→ Digital overlay) ←→ SCART
101	CVBS ←→ (SCART ←→ Digital overlay)
110	CVBS only
111	Component only

2 SCART Mode

The TVP5146 has four 30-MSPS, 10-bit A/D channels that can be set up to sample composite CVBS video and component RGB/YPbPr inputs simultaneously. In the SCART mode of operation, all synchronization and timing is derived from the CVBS video input signal. This CVBS signal must always be assigned to input terminal VI_4_A (pin 23) for proper SCART operation. Various SCART input configurations are selectable in the I^2C input select register (00h) and are shown in Appendix A along with the other overlay and fast-switch related registers. Automatic gain control is provided for the CVBS input signal, but a fixed, manually controlled gain is used for the RGB/YPbPr inputs. The default fixed gain settings are set for nominal RGB input levels.

Various SCART overlay options are also available and selectable in I^2C register 28h. Pixel-by-pixel switching is supported by use of the FSS/GPIO fast-switch input terminal. This FSS input can be used to overlay RGB graphics pixel-by-pixel or can be used to define a window for picture-in-picture applications. Internal scaling is not supported, so all overlay formatting must be handled by the video source.

Figure 2 shows a typical application where RGB is overlaid with CVBS. The polarity of the FSS/GPIO input terminal defines which input source is passed to the digital output in any instance. The polarity FSS bit in I^2C register 28h can be used to invert the polarity of the FSS fast switch input, essentially inverting the overlay. Typical hardware and I^2C software configurations for this mode of operation are shown in Table 2 and Figure 3. Level translation may be required for the fast-switch input.



Polarity FSS in Register 28h = 1 Polarity FSS in Register 28h = 0

Figure 2. SCART Overlay With CVBS (Mode 000: CVBS ←→ SCART)

Table 2. Typical I^2C Setup for SCART RGB Overlay With CVBS

I^2C Subaddress	Contents	Description
00h	CCh	Assign CVBS to VI_4_A , select SCART RGB and assign to VI_1_A, VI_2_A, and VI_3_A
28h	04h	Select CVBS <> SCART fast switch mode, polarity FSS = 0, FSS sampled on falling edge

Note: See Appendix A for a more detailed description of the I^2C registers.

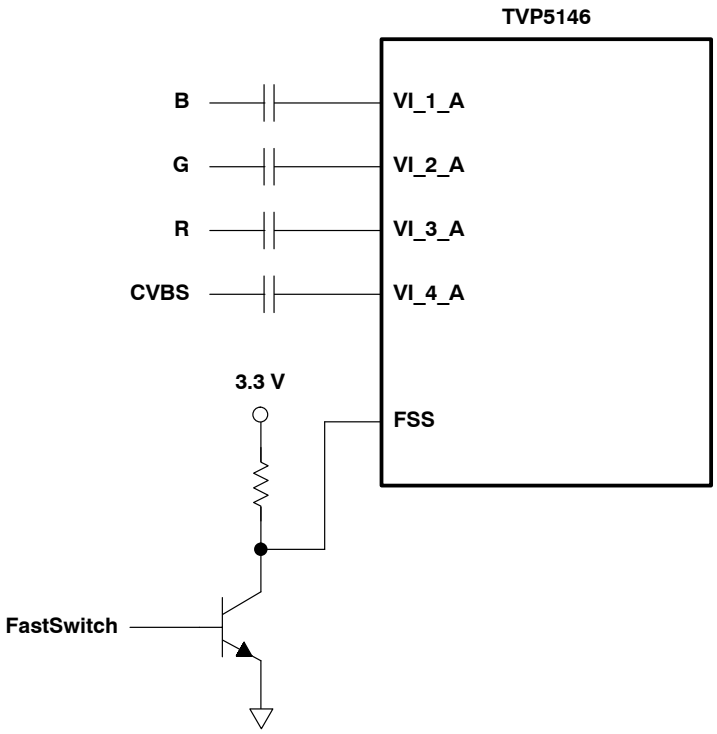


Figure 3. Typical RGB, CVBS, and FSS Connections for SCART

3 Digital RGB Overlay

The TVP5146 also provides support for pixel-by-pixel overlay of digital RGB on decoded CVBS, S-video, or component video. Three input terminals (C_6_GPIO_RED, C_7_GPIO_GREEN, and C_8_GPIO_BLUE) are available for a total of eight possible colors. In this mode of operation, the TVP5146 receives digital RGB from a back-end processor or OSD device that is synchronized to the input video source and the TVP5146. The FSO/PGIO input terminal, similar to the FSS/GPIO input used for SCART overlay, is used as the fast-switch control for digital overlay. Best performance is achieved when this FSO control and the digital RGB inputs are synchronized with the TVP5146 DATACLK output.

As with SCART overlay, the polarity of the FSO input terminal defines which input source is active in any given instance. The polarity FSO bit in I^2C register 28h can be used to invert this polarity (Figure 4 and Figure 5). Figure 6, Table 3, and Table 4 show typical hardware and software configurations for digital RGB overlay with CVBS and component YPbPr inputs.

Digital overlay is only supported when a 10-bit output format is used. If a 20-bit output format is required, SCART overlay can be used to overlay the digital RGB on CVBS as analog RGB (Figure 7). This method can also offer improved performance if the digital RGB cannot be properly synchronized with the TVP5146 DATACLK. Resistor dividers should be used to establish proper analog RGB input levels. In this mode of operation, I^2C software setup is identical to the SCART overlay mode.

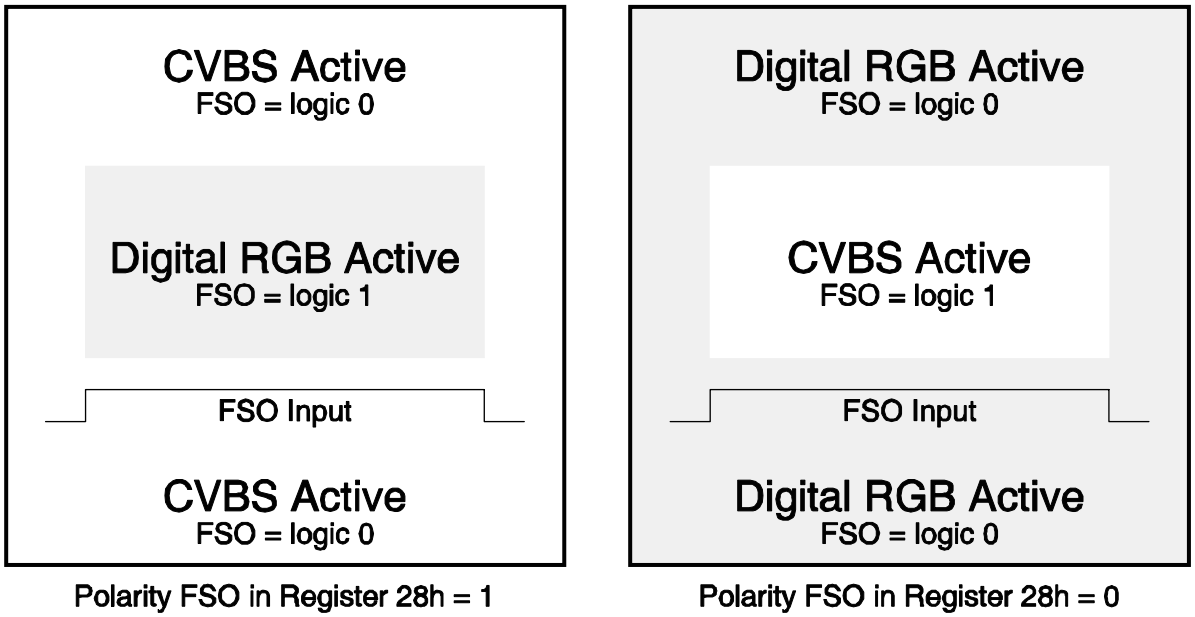


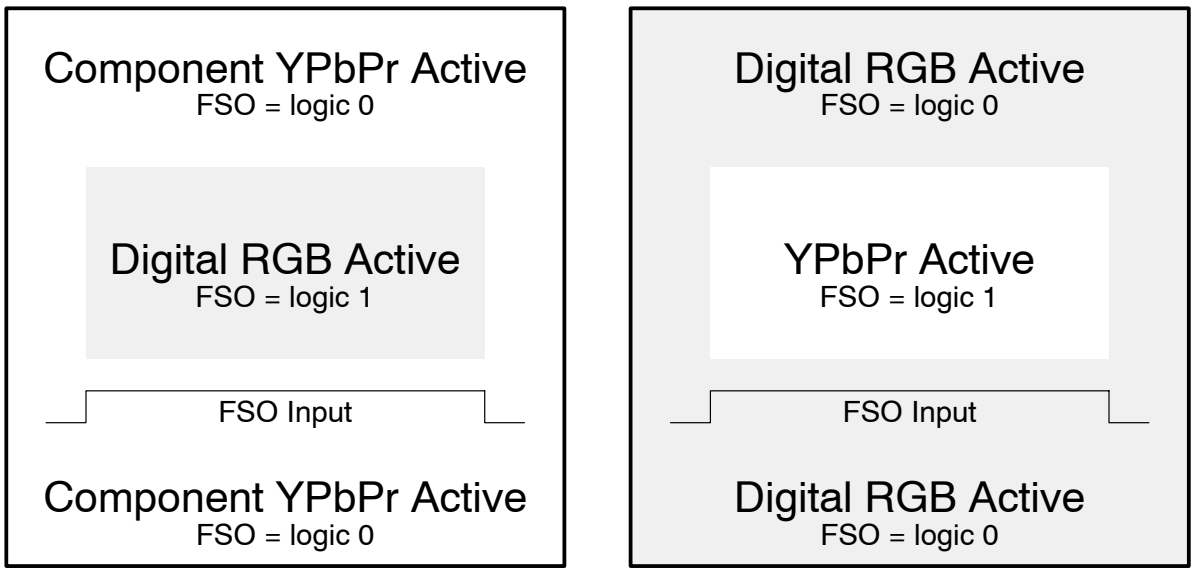
Figure 4. Digital RGB Overlay with CVBS (Mode 001: (CVBS, S_VIDEO ←→ Digital Overlay)

Note: Video output switching is controlled by the FSO/GPIO input terminal. The FSO polarity bit in I^2C register 28h can be used to invert the polarity of the FSO fast-switch input.

Table 3. Typical I^2C Setup for Digital RGB Overlay With CVBS

I^2C Subaddress	Contents	Description
00h	0Ch	Assign only CVBS to VI_4_A.
28h	28h	Select CVBS, S_VIDEO ←→ Digital overlay fast-switch mode, polarity FS0 = 0, FS0 sampled on falling edge.

Note: See Appendix A for a more detailed description of the I^2C registers.



Polarity FSO in Register 28h = 1 Polarity FSO in Register 28h = 0

Figure 5. Digital RGB Overlay With Component YPbPr (Mode 2: Component ←→ Digital Overlay)

Table 4. Typical I^2C Setup for Digital RGB Overlay With Component YPbPr

I^2C Subaddress	Contents	Description
00h	94h	Assign only YPbPr to VI_1_A, VI_2_A, and VI_3_A.
28h	48h	Select component ←→ Digital overlay fast-switch mode, polarity FS0 = 0, FS0 sampled on falling edge.

Note: See Appendix A for a more detailed description of the I^2C registers.

Figure 6 is a block diagram depicting digital RGB overlay. Eight colors of digital RGB can be overlaid on CVBS, S-video, or component inputs. Best performance is achieved if digital RGB data and FSO are synchronized to DATACLK. Digital overlay is only supported when a 10-bit output format is used.

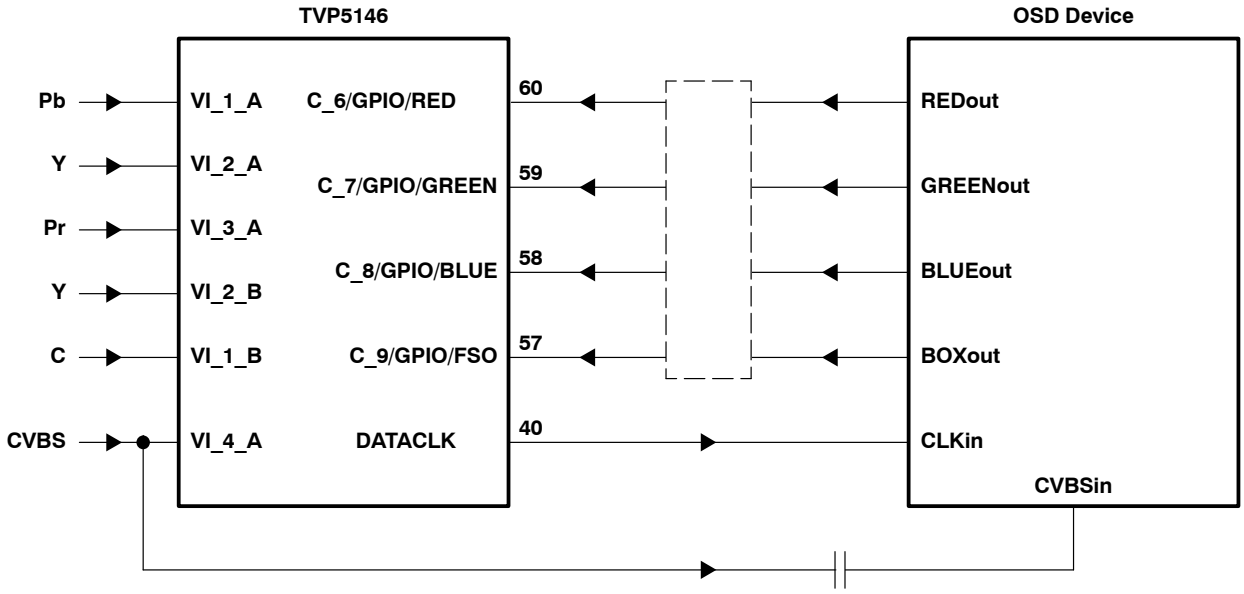


Figure 6. Digital RGB Overlay

Note: Digital RGB and FSO inputs are 3.3-V compliant. Attenuation or level translation may be required with some OSD devices.

Figure 7 is a block diagram depicting the SCART-mode overlay of digital RGB. If 20-bit output format is required, SCART analog overlay can be used to overlay digital RGB on CVBS video. Resistor dividers should be used to establish proper analog input levels. This method can also offer performance advantages in 10-bit applications, if RGB data cannot be synchronized properly to the TVP5146 DATACLK.

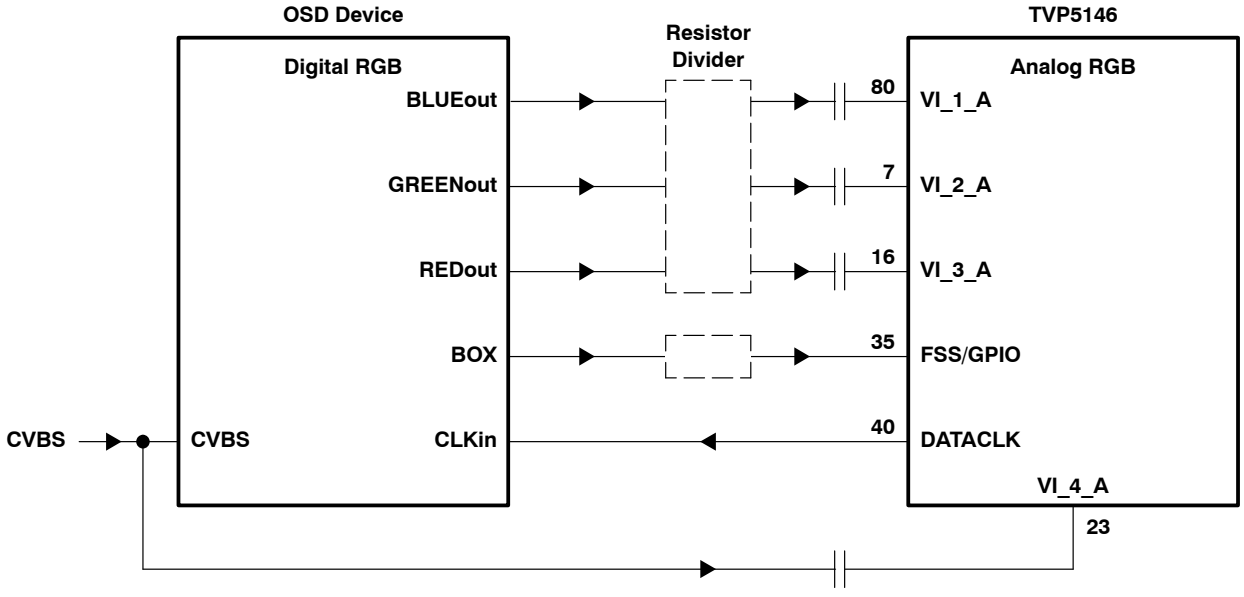


Figure 7. SCART-Mode Overlay of Digital RGB

Appendix A. SCART- and Overlay-Related I²C Registers

Input Select

Subaddress	00h

Default (00h)

7	6	5	4	3	2	1	0
Input select [7:0]							

	INPUT(S) SELECTED	Input Select [7:0]								
		7	6	5	4	3	2	1	0	HEX
CVBS	VI_1_A (default)	0	0	0	0	0	0	0	0	00
	VI_1_B	0	0	0	0	0	0	0	1	01
	VI_1_C	0	0	0	0	0	0	1	0	02
	VI_2_A	0	0	0	0	0	1	0	0	04
	VI_2_B	0	0	0	0	0	1	0	1	05
	VI_2_C	0	0	0	0	0	1	1	0	06
	VI_3_A	0	0	0	0	1	0	0	0	08
	VI_3_B	0	0	0	0	1	0	0	1	09
	VI_3_C	0	0	0	0	1	0	1	0	0A
	VI_4_A	0	0	0	0	1	1	0	0	0C
S-Video	VI_2_A(Y), VI_1_A(C)	0	1	0	0	0	1	0	0	44
	VI_2_B(Y), VI_1_B(C)	0	1	0	0	0	1	0	1	45
	VI_2_C(Y), VI_1_C(C)	0	1	0	0	0	1	1	0	46
	VI_2_A(Y), VI_3_A(C)	0	1	0	1	0	1	0	0	54
	VI_2_B(Y), VI_3_B(C)	0	1	0	1	0	1	0	1	55
	VI_2_C(Y), VI_3_C(C)	0	1	0	1	0	1	1	0	56
	VI_4_A(Y), VI_1_A(C)	0	1	0	0	1	1	0	0	4C
	VI_4_A(Y), VI_1_B(C)	0	1	0	0	1	1	0	1	4D
	VI_4_A(Y), VI_1_C(C)	0	1	0	0	1	1	1	0	4E
	VI_4_A(Y), VI_3_A(C)	0	1	0	1	1	1	0	0	5C
	VI_4_A(Y), VI_3_B(C)	0	1	0	1	1	1	0	1	5D
	VI_4_A(Y), VI_3_C(C)	0	1	0	1	1	1	1	0	5E
RGB	VI_1_A(B), VI_2_A(G), VI_3_A(R)	1	0	0	0	0	1	0	0	84
	VI_1_B(B), VI_2_B(G), VI_3_B(R)	1	0	0	0	0	1	0	1	85
	VI_1_C(B), VI_2_C(G), VI_3_C(R)	1	0	0	0	0	1	1	0	86
YPbPr	VI_1_A(Pb), VI_2_A(Y), VI_3_A(Pr)	1	0	0	1	0	1	0	0	94
	VI_1_B(Pb), VI_2_B(Y), VI_3_B(Pr)	1	0	0	1	0	1	0	1	95
	VI_1_C(Pb), VI_2_C(Y), VI_3_C(Pr)	1	0	0	1	0	1	1	0	96
SCART	VI_1_A(B), VI_2_A(G), VI_3_A(R), VI_4_A(CVBS)	1	1	0	0	1	1	0	0	CC
	VI_1_B(B), VI_2_B(G), VI_3_B(R), VI_4_A(CVBS)	1	1	0	0	1	1	0	1	CD
	VI_1_C(B), VI_2_C(G), VI_3_C(R), VI_4_A(CVBS)	1	1	0	0	1	1	1	0	CE
	VI_1_A(Pb), VI_2_A(Y), VI_3_A(Pr), VI_4_A(CVBS)	1	1	0	1	1	1	0	0	DC
	VI_1_B(Pb), VI_2_B(Y), VI_3_B(Pr), VI_4_A(CVBS)	1	1	0	1	1	1	0	1	DD
	VI_1_C(Pb), VI_2_C(Y), VI_3_C(Pr), VI_4_A(CVBS)	1	1	0	1	1	1	1	0	DE

Fast-Switch Control

Subaddress	28h

Default (CCh)

7	6	5	4	3	2	1	0
Mode [2:0]			Reserved	FSO edge	FSS edge	Polarity FSO	Polarity FSS

Mode [2:0]: Select fast-switch modes

000 = CVBS ←→ SCART
001 = CVBS, S_VIDEO ←→ Digital overlay
010 = Component ←→ Digital overaly
011 = (CVBS ←→ SCART) ←→ Digital overlay
100 = (CVBS ←→ Digital overlay) ←→ SCART
101 = CVBS ←→ (SCART ←→ Digital overlay)
110 = Composite only (default)
111 = Component only

FSO edge: FSO is sampled at rising or falling edge of sampling clock

0 = Rising edge
1 = Falling edge (default)

FSS edge: FSS is sampled at rising or falling edge of sampling clock

0 = Rising edge
1 = Falling edge (default)

Polarity FSO

0 = Digital RGB overlay is active when the FSO input is low.
1 = Digital RGB overlay is active when the FSO input is high.

Polarity FSS

0 = SCART overlay is active when the FSO input is low.
1 = SCART overlay is active when the FSO input is high.

Fast-Switch Overlay Delay

Subaddress	29h

Default (00h)

7	6	5	4	3	2	1	0
Reserved			FSO delay [4:0]				

FSO delay [4:0]: Adjusts delay between digital RGB and FSO

01111 = +15-pixel delay
00001 = +1-pixel delay
00000 = 0-pixel delay (default)
11111 = -1-pixel delay
10000 = -16-pixel delay

Fast-Switch SCART Delay

Subaddress	2Ah

Default (00h)

7	6	5	4	3	2	1	0
Reserved			FSS delay [4:0]				

FSS delay [4:0]: Adjusts delay between FSS and component RGB/YPbPr

01111 = +15-pixel delay
00001 = +1-pixel delay
00000 = 0-pixel delay (default)
11111 = -1-pixel delay
10000 = -16-pixel delay

Overlay Delay

Subaddress	2Bh

Default (00h)

7	6	5	4	3	2	1	0
Reserved			Overlay delay [4:0]				

Overlay delay[4:0]: Adjusts delay between digital RGB and CVBS (or S-Video or component video)

01111 = +15-pixel delay
00001 = +1-pixel delay
00000 = 0-pixel delay (default)
11111 = -1-pixel delay
10000 = -16-pixel delay

SCART Delay

Subaddress	2Ch

Default (00h)

7	6	5	4	3	2	1	0
Reserved			SCART delay [4:0]				

SCART delay[4:0]: Adjusts delay between CVBS and component (RGB) video

01111 = +15-pixel delay
00001 = +1-pixel delay
00000 = 0-pixel delay (default)
11111 = -1-pixel delay
10000 = -16-pixel delay

Appendix B. Additional Overlay Options

Figure 8 shows fast-switch mode 003. In this mode, CVBS is first overlaid with SCART and the result then overlaid with digital RGB. FSO has priority over FSS.

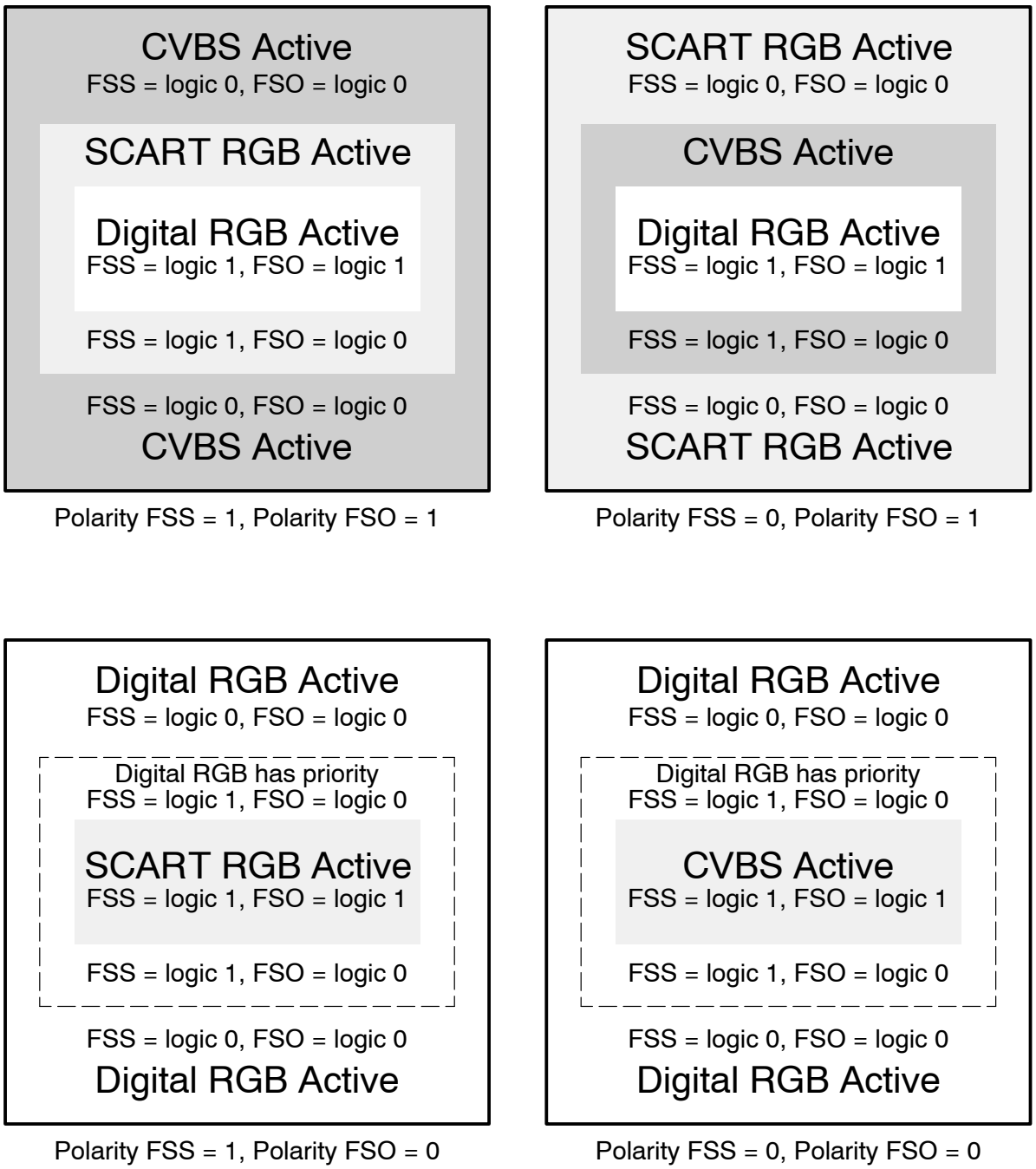


Figure 8. Fast-Switch Mode 003 [(CVBS ←→ SCART) ←→ Digital Overlay]

Figure 9 shows fast-switch mode 004. In this mode, CVBS is overlaid with digital RGB, and the result then overlaid with SCART. FSS has priority over FSO.

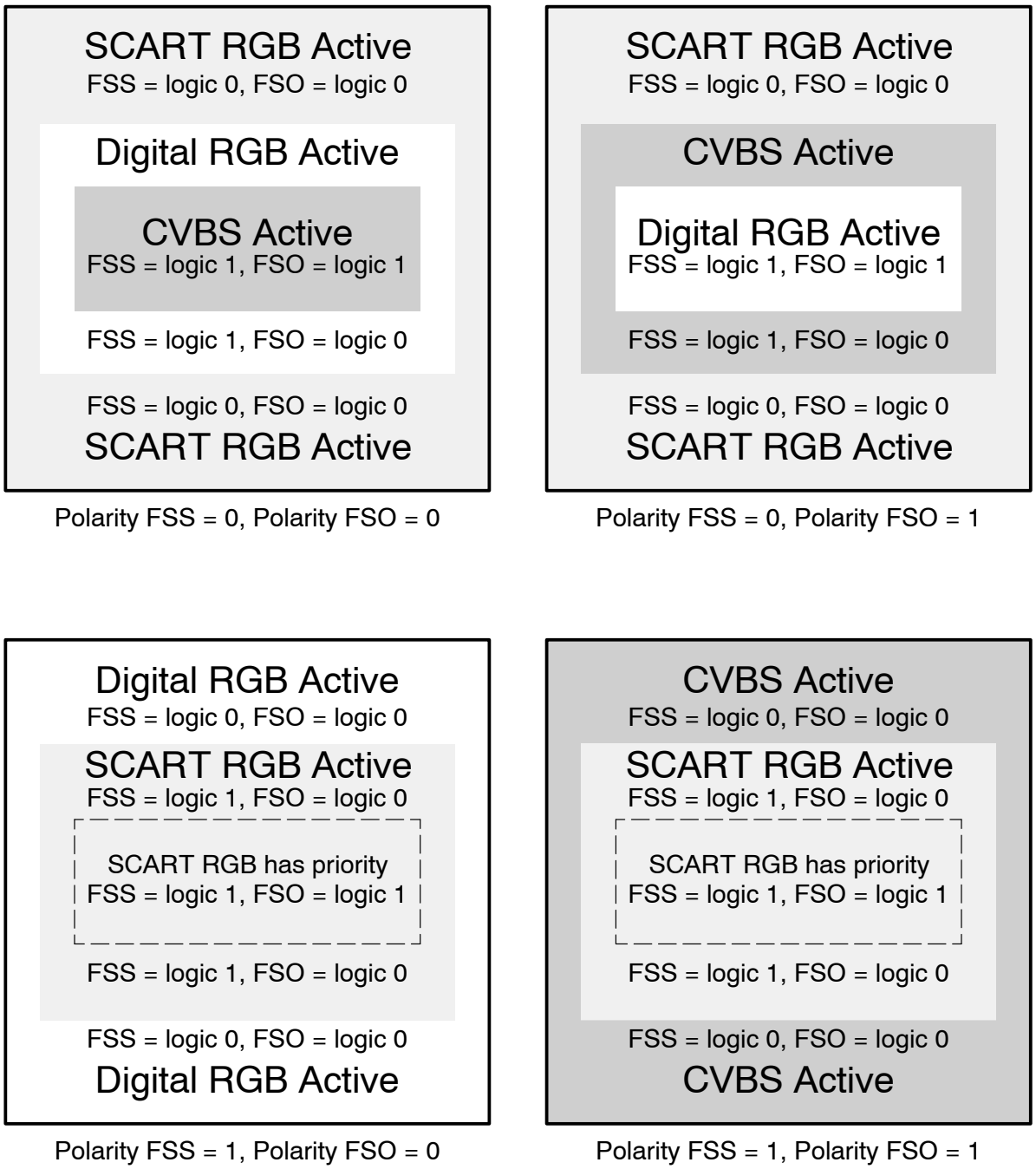


Figure 9. Fast Switch Mode 004 [(CVBS ←→ Digital Overlay) ←→ SCART]

Figure 10 shows fast-switch mode 005. In this mode, SCART is overlaid with digital RGB, and the result then overlaid with CVBS. FSS has priority over FSO.

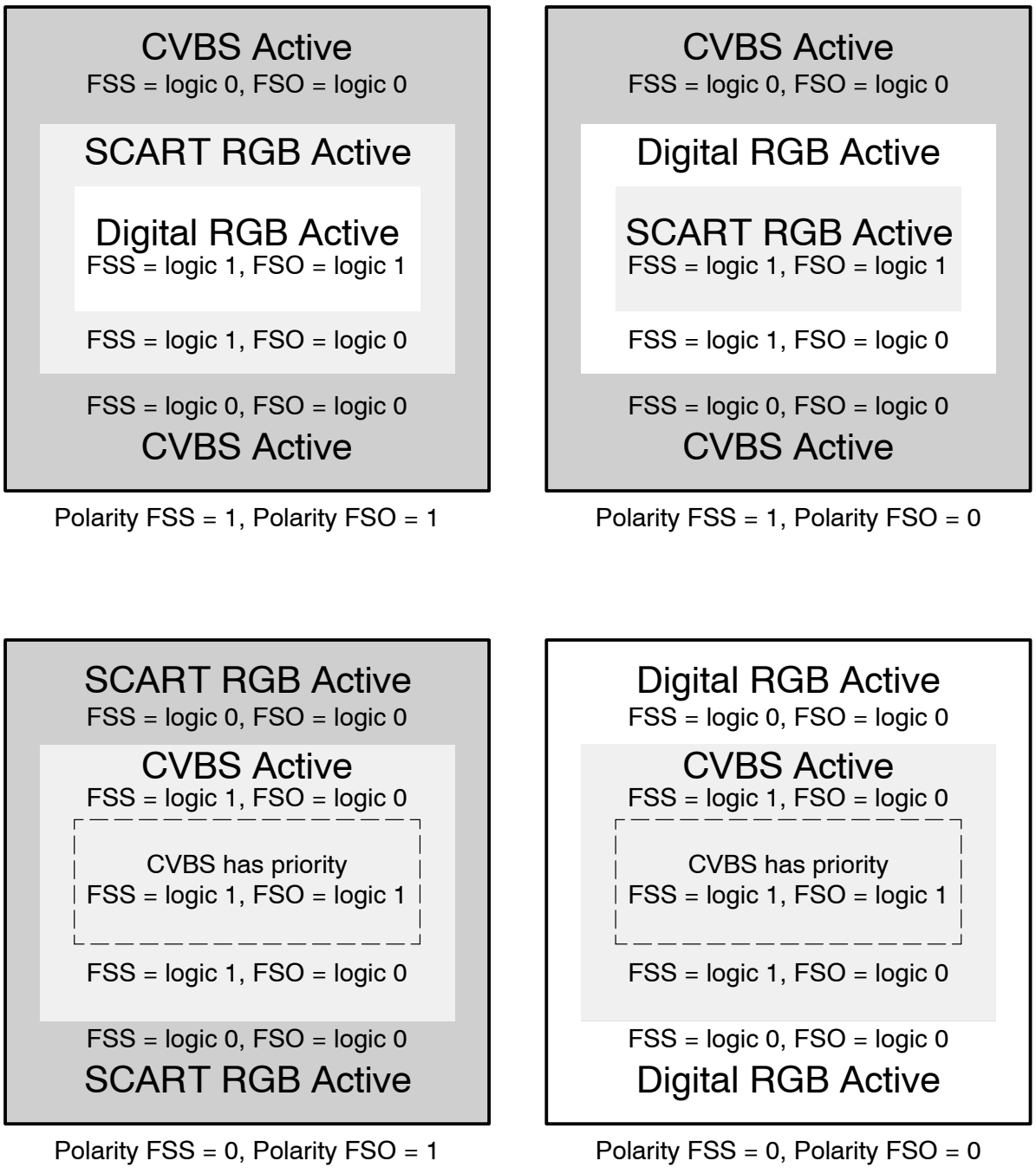


Figure 10. Fast Switch Mode 005 [CVBS ←→ (SCART RGB ←→ Digital Overlay)]

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