

## TVP5150AM1 PCB Layout Guidelines

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- Ensure that power bus/plane routing is adequate to handle current requirements of device. The maximum power for this device is 185 mW.
  - The maximum current for 3.3V I/O supply is 7.9 mA.
  - The maximum current for 1.8VD is 33.5 mA.
  - The maximum current for 1.8VAPLL is 7.9 mA.
  - The maximum current for 1.8VACore is 39.2 mA.
- Place TVP5150AM1 as close as possible to the video input jacks.
- All device decoupling capacitors should be placed near the power and ground pins of the device.
- Keep reasonable clearances between the 14.31818-MHz crystal/associated circuitry and adjacent trace routing. Reasonable clearances of eight to ten times the associated trace width, ground shields placed around adjacent video traces, and placing a slot/cutout around 14.31818-MHz crystal and associated circuitry in ground plane and ground fill layers all help with signal isolation.
- Two analog video input traces should have a minimum clearance of eight to ten times the associated trace width between each other and any adjacent traces to minimize potential crosstalk.
- A 50- $\Omega$  board impedance is recommended while maintaining a composite (CVBS) video input trace impedance close to 75  $\Omega$ .
- SDA/SCL traces should be routed together and have a minimum clearance of ten times the trace width from any adjacent traces.
- Maximum specified loading condition for digital video output traces (YOUT[6:0]) and PCLK/SCLK is 10 pF.
- 22- $\Omega$  or 33- $\Omega$  series terminators are recommended in data and clock lines.
- All high-speed signals routed on the bottom of board should be routed over solid power/ground planes and not routed over power/ground splits. Route signals over their associated power/ground planes where possible.
- Use ground fills on top and bottom of the board for additional signal isolation.
- A split ground plane approach is preferred but is not a requirement.
- If a split ground plane (AGND/DGND) approach is used for board layout, Figure 1 shows the recommendation for the split relative to device pins. If split ground plane approach is not used, a cutout/slot should still be placed around 14.31818-MHz crystal and associated circuitry as depicted in Figure 1 for improved isolation.

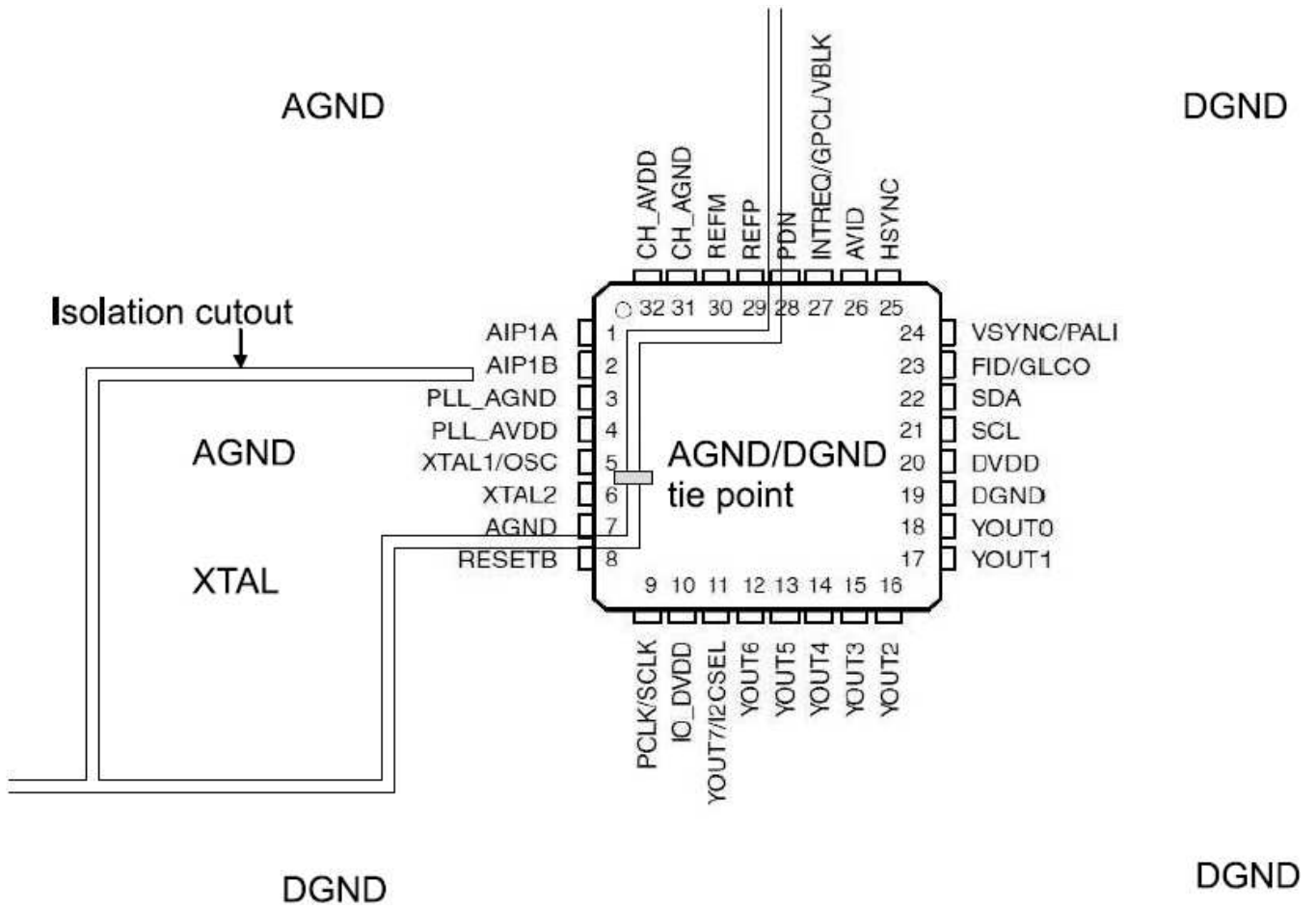


Figure 1. Split Ground Planes (TQFP Package)

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