Application Report
SLEA110–May 2011

TVP5160 3D Noise Reduction Calibration Procedure

1 Introduction

The TVP5160 supports temporal frame recursive noise reduction (3DNR). This feature reduces the level of noise in CVBS, S-Video, or component video inputs by comparing multiple frames of data and canceling out the resulting noise.

The 3DNR utilizes the same frame buffer memory used by the 3DYC and may operate concurrently with 3DYC. The modes of operation for the 3DNR and 3DYC are listed in Table 1.

Table 1. 3DNR and 3DYC Modes of Operation

Mode	Operation	Memory Required
Mode 0	3DYC + 3DNR	4 MBytes
Mode 1	3DYC only	2 MBytes
Mode 2	2D 5-line CF + 3DNR	2 MBytes
Mode 3	2D 5-line CF only (default)	None

2 Technology Overview

The purpose of 3DNR is to reduce the noise present in the input signal. A simplified block diagram of the 3DNR is shown in Figure 1. A noise measurement is made on the sync tip of the digitized composite video or luma channel input during active video. It is processed by the on-chip processor to generate controls for the 3DNR blocks that are applied to the luma (y) and demodulated chroma (uv) outputs of the YC separation.

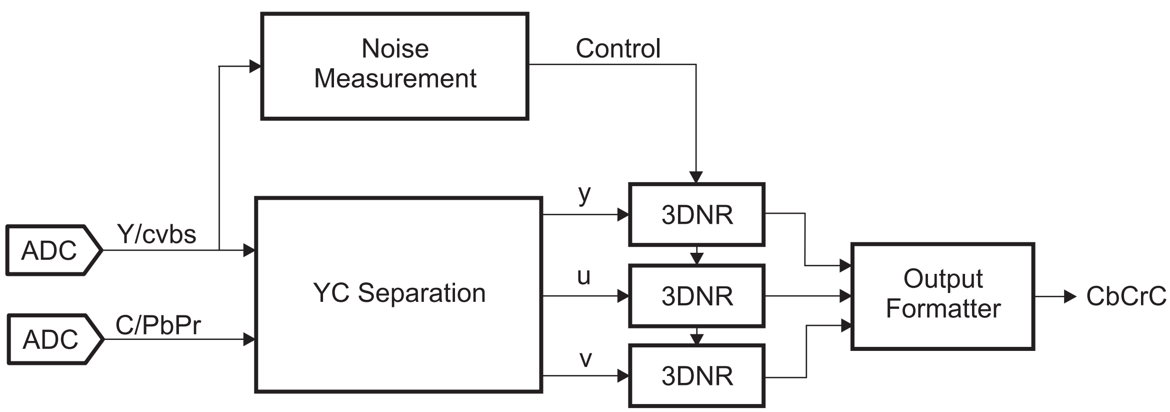
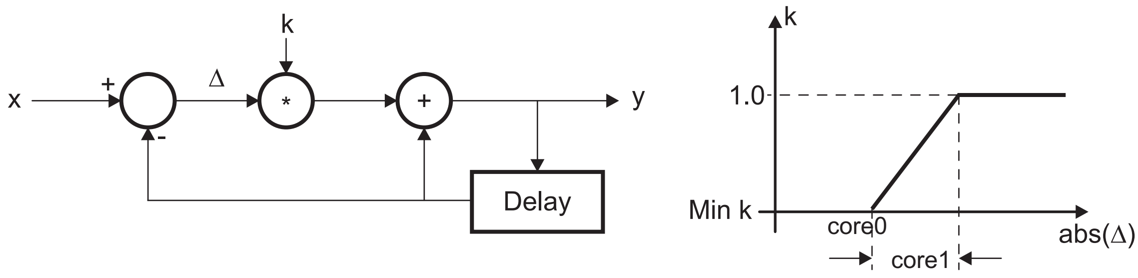


Figure 1. 3D Noise Reduction

The 3DNR block consists of a recursive filter that averages its input with a frame delayed output. Figure 2 shows the filter.



$$y_n = k \times x_n + (1 - k) \times y_{n-1} = k \times (x_n - y_{n-1}) + y_{n-1}$$

Figure 2. 3D Noise Reduction Filter

The Δ is the difference between the incoming pixel and frame delayed pixel and represents the level of motion or noise present. The k parameter is computed on a pixel basis and specifies the filter time constant. When k is 1.0 the input is passed through to the output and when k is 0.0 the output circulates in the frame delay buffer causing a still picture (freeze frame). When k is between 0.0 and 1.0 averaging is performed on the input and frame delayed output. This is the area in which 3DNR is performed.

When k is 1.0 and the input is passed through to the output, either motion or an excessive level of noise is present. In this case, the Δ parameter becomes larger than Core1, and the filter and frame delay buffer are reinitialized. No 3DNR is performed.

When k is 0.0, the output circulates in the frame delay buffer causing a still picture (freeze frame). This means that no noise is present and 3DNR is not performed. To avoid the picture from freezing, k is constrained to a minimum value of 0.1.

When k is between 0.1 and 1.0 (pixels are static), 3DNR is performed where the filter averages frames and reduces the noise.

Core0 and core1 are coring thresholds which are computed based on the noise measurement. These computations are adaptive and are not manually adjustable. It is possible to read the Core0 and Core1 values in I^2C registers described in Section 3.

The coring values are calculated in firmware as follows:

y_core0 = 3 × y noise sensitivity / 128 × noise measurement / (2 × number of noise samples)
uv_core0 = 3 × uv noise sensitivity / 128 × noise measurement / (4 × number of noise samples)
number of noise samples = 256

y_core1 = smallest power of 2 larger than y_core0
uv_core1 = smallest power of 2 larger than uv_core0

To avoid a hard switch between the coring thresholds the difference between Core0 and Core1 is checked; if small Core1 is increased by a factor of 2.

if (abs(y_core1 - y_core0) < (y_core0 >> 2)) *y_core1 = 2 × y_core1*
if (abs(uv_core1 - uv_core0) < (uv_core0 >> 2)) *uv_core1 = 2 × uv_core1*

A programmable limit is applied to core0 such that the noise adaptation may be disabled when the noise becomes excessive.

For low noise, the motion detection parameter km from 3DYC may be used as another parameter to control k. This feature is enabled by using the 3DNR Low Noise Limit Register (5Eh), which is applied to the noise measurement. Experimenting with this register beyond the default value has provided little improvement to the 3DNR performance.

3 3DNR Manual Mode

A manual mode of operation can be enabled to override the automatic adjustment of Y core0 and UV core0 based on the noise measurement. In this case, the 3DNR can be controlled manually by writing to Y core0 (register 66h) and UV core0 (register 67h).

Manual mode is enabled by writing 01h to I²C register D4h.

4 I²C Registers

Table 2 lists the I²C registers which control 3DNR. The most significant byte (MSB) of the noise measurement represents the average noise amplitude. The weak signal condition is determined by comparison of the MSB of the noise measurement with the low and high thresholds. If the noise is greater than the high threshold, then weak signal is TRUE; else, if the noise is less than the low threshold, then weak signal is FALSE.

Table 2. I²C Registers for 3DNR

Register Name	Address	Default	Description	R/W
Chrominance Processing Control 1	0Dh	00h	bit 2 enables 3DNR	R/W
3DNR Y Noise Sensitivity	5Ah	80h	y noise sensitivity	R/W
3DNR UV Noise Sensitivity	5Bh	80h	uv noise sensitivity	R/W
3DNR Y Coring Threshold Limit	5Ch	80h	y coring limit	R/W
3DNR UV Coring Threshold Limit	5Dh	40h	uv coring limit	R/W
3DNR Low Noise Limit	5Eh	80h	low noise limit	R/W
Noise Measurement LSB	64h		noise measurement LSB	R
Noise Measurement MSB	65h		noise measurement MSB	R
3DNR Y Core0	66h		y core0	R
3DNR UV Core0	67h		uv core0	R
Weak Signal High Threshold	95h	60h	weak signal upper threshold	R/W
Weak Signal Low Threshold	96h	50h	weak signal lower threshold	R/W
Manual 3DNR Mode Enable	D4h	00h	bit 1 enables manual mode	R/W

5 Configuring the SDRAM Controller

The SDRAM controller of the TVP5160 must be properly initialized before enabling 3DNR. This is to ensure the SDRAM controller is configured for the memory size used.

Table 3 shows the SDRAM control register used to configure the SDRAM controller. The bit definitions are also provided. Typically only the Configuration and the Enable bits must be set to configure the SDRAM controller. The SDRAM_CLK delay control has been optimized by default for most SDRAM parts.

After the SDRAM controller is properly configured, 3DNR may be enabled by setting the Chrominance Processing Control 1 register (0Dh) to 04h.

Table 3. SDRAM Control Register – 59h

7	6	5	4	3	2	1	0
Reserved	**SDRAM_CLK delay control**				**Enable**	**Configuration[1:0]**	

Configuration[1:0]

Bit 1	Bit 0	Arrangement	
0	0	2 banks x 2048 rows x 256 columns	16 Mbits
0	1	4 banks x 2048 rows x 256 columns	32 Mbits
1	0	2 banks x 4096 rows x 256 columns	32 Mbits
1	1	4 banks x 4096 rows x 256 columns	64 Mbits

Memories with more rows, columns and/or banks can be used as long as the minimum requirements are met. Additional rows, columns and/or banks are ignored and unused by the memory controller.

The memory controller must be configured before enabling 3DYC or 3DNR; otherwise, incorrect operation of the memory controller will result.

Enable

0 = SDRAM controller disabled (default)

1 = SDRAM controller enabled

SDRAM_CLK Delay Control[3:0]

These bits change the delay from the default position of SDRAM_CLK in increments of approximately 0.58 ns.

Bit 3	Bit 2	Bit 1	Bit 0	Delay
0	0	0	0	0 (default)
0	0	0	1	0.58 ns
1	0	0	0	1.16 ns
1	1	1	1	9.3 ns

6 Calibration Procedure

Calibration of 3DNR may be done in the following sequence by adjusting the Y/UV Coring Limit registers as well as the Y/UV Noise Sensitivity registers. It may also be beneficial to use the slider controls available in the TVP5160 EVM software, WinVCC. The coring limits and noise sensitivity for Y/UV are adjustable using the slider controls within this Windows-based software.

The input source into the TVP5160 should be a video test pattern that is modulated to RF by a VCR, attenuated, and then demodulated to baseband by another VCR. Calibration is done separately for luma and chroma. A grey raster pattern is used for luma and a blue raster for chroma.

1. Set coring limits for luma and chroma to maximum
2. Set sensitivities for luma and chroma to minimum
3. Increase sensitivity for luma (chroma) until noise is minimum
4. Decrease coring limit for luma (chroma) until noise starts to increase
5. Read the sensitivity parameter and use it as the permanent setting
6. Read the coring limit parameter and use it as the permanent setting

Table 4 shows example Noise Sensitivity and Coring Limit settings given input sources of approximately 10-, 15-, and 20-dB attenuation. These values are experimental and derived from internal testing on various television tuners.

Table 4. Example 3DNR Settings

RF Attenuation (dB)	5Ah	5Bh	5Ch	5Dh
10	80h	80h	14h	0Ah
15	80h	80h	24h	12h
20	80h	80h	38h	1Ch

7 Characteristics

Figure 3 through Figure 5 show various characteristics of the TVP5160 3DNR.

Figure 3 shows the 3DNR characteristics for low levels of noise for different core0 values; core1 is equal to 2*core0. Figure 3 shows the k versus delta characteristic where delta is the difference between the input and the frame delayed output of the 3DNR filter. As the noise increases, the core0 and core1 values increase.

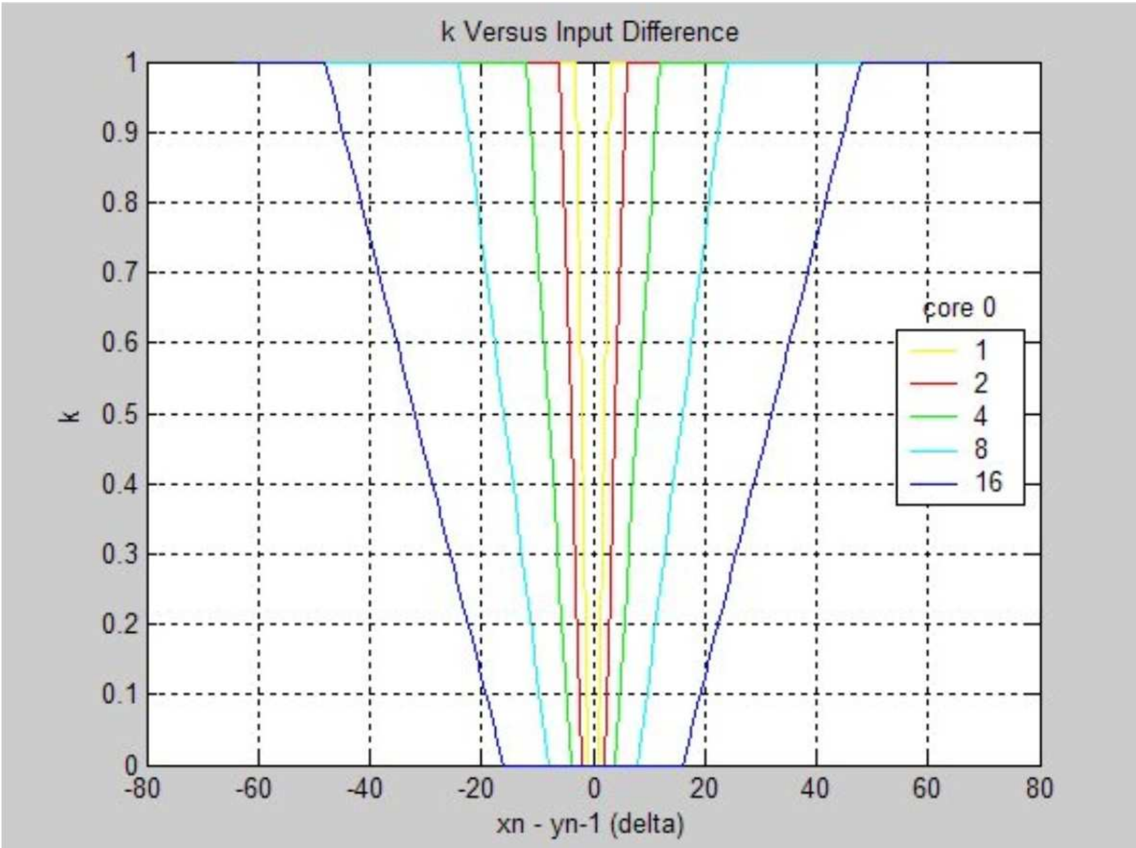


Figure 3. k vs delta

Figure 4 shows the output difference between the current and previous frame pixel versus delta. The coring takes effect for small delta and its range is a function of the core0 value.

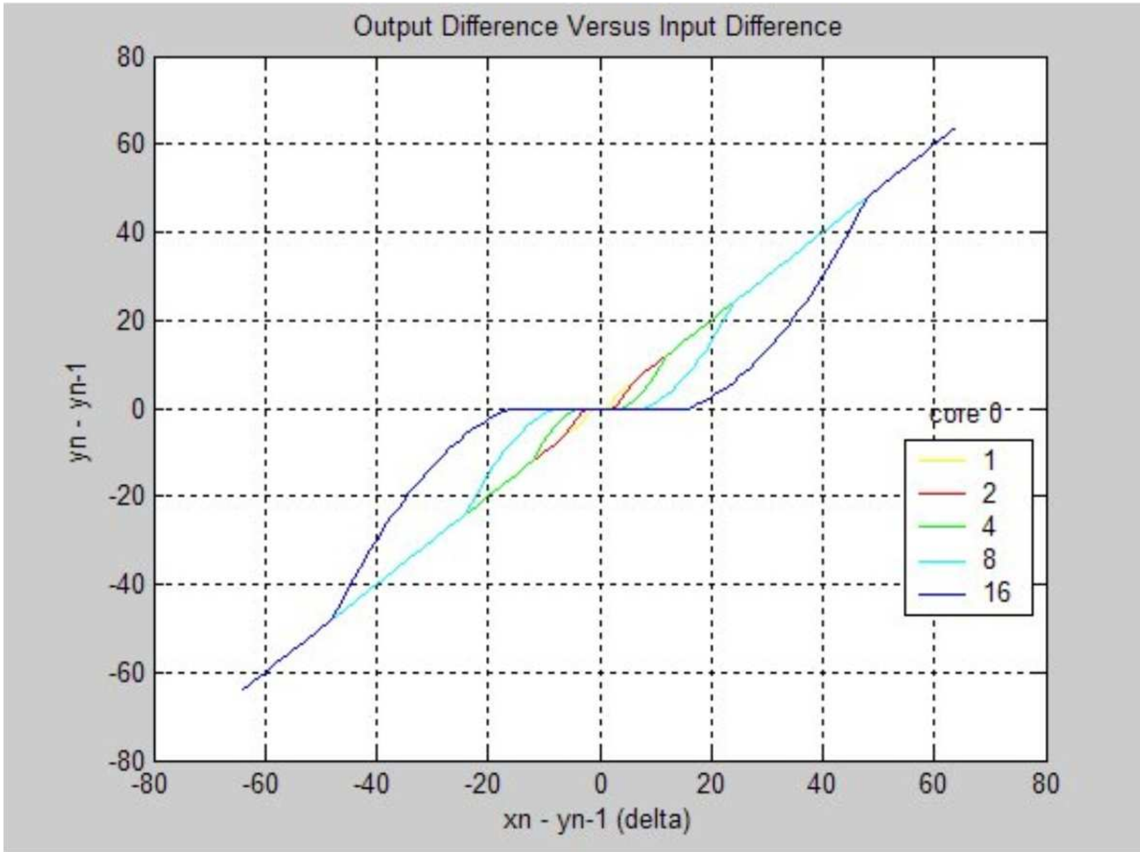


Figure 4. Output Difference vs Delta

Figure 5 shows the I/O difference versus delta for different values of core0. For small delta the I/O difference is the noise; when delta increases beyond a threshold then the I/O difference decreases to zero at which the input is passed through the filter to the output.

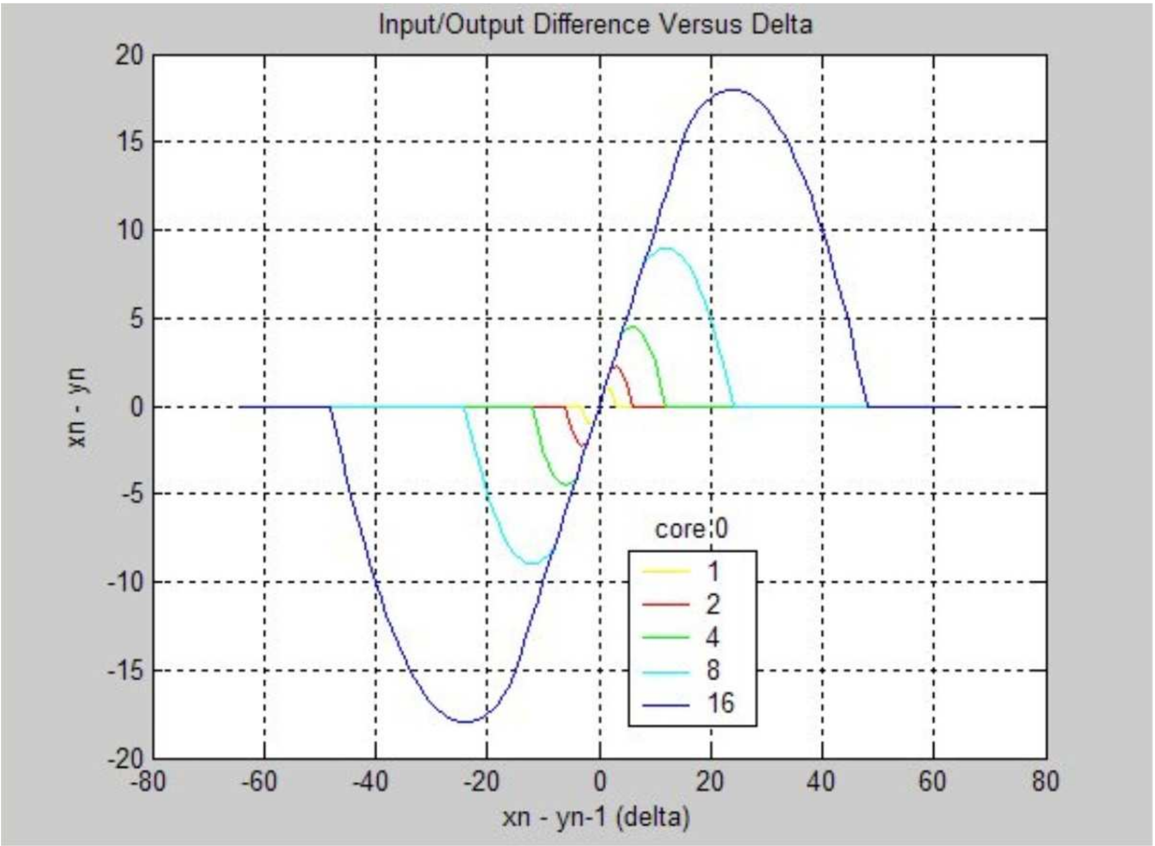


Figure 5. I/O Difference vs Delta

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265