TEXAS INSTRUMENTS

DAVREF633

Design Guidelines for the TAS5086 Six-Channel Digital Audio PWM Processor and TAS5111/TAS5112A Digital Amplifier Power Output Stage—Single-Ended Configuration

Design Guide

December 2004

Digital Audio Group

SLEU059

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Preface

Read This First

About This Manual

This manual describes design guidelines for the DAVREF633 reference design from Texas Instruments.

How to Use This Manual

This document contains the following chapters:

- ❑ Chapter 1 – Introduction
- ❑ Chapter 2 – System Interfaces
- ❑ Chapter 3 – Protection
- ❑ Chapter 4 – Performance Graphs
- ❑ Chapter 5 – System Setup and Debugging
- ❑ Chapter 6 – Bill of Materials, Layout, and Schematics

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

CAUTION

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

WARNING

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following table contains a list of data sheets that have detailed descriptions of the integrated circuits used in the design of the DAVREF633 board. These items can be obtained at the URL http://www.ti.com.

Document Title	Literature Number
TAS5086 data sheet	N/A
TAS5111 Digital Amplifier Power Stage data sheet	SLES049
TAS5112A Digital Amplifier Power Stage data sheet	SLES094
System Design Considerations for True Digital Audio Power Amplifiers	SLAA117

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Chapter 1

Introduction

The DAVREF633 PurePath Digital™ reference design demonstrates three integrated circuits, TAS5086DBT, TAS5112ADFD, and TAS5111DAD from Texas Instruments (TI).

The TAS5086 is a high-performance 32-bit (24-bit input) multichannel PurePath Digital pulse-width modulator (PWM) based on Equibit™ technology with a fully symmetrical AD modulation scheme. The device also has integrated bass management and downmixing capabilities.

The power stages are high-performance digital amplifiers. In this reference design, they are designed to drive four 4-Ω loudspeakers up to 20 W at 10%THD+N (TAS5112ADFD) in the single-ended (SE) configuration, and two 4-Ω loudspeakers up to 25 W at 10% THD+N (TAS5111DAD) in the SE configuration. Each power stage has integrated gate drivers, matched and electrically isolated enhancement-mode N-channel power DMOS transistors, and protection/fault-reporting circuitry.

The DAVREF633 reference design is configured with six SE channels. This reference design, together with a TI input design DAVMC003 and DeVaSys USB-I^2C interface, is a complete 6-channel digital audio amplifier system which includes digital input (S/PDIF). This reference is intended for home theater applications such as DVD mini-component systems, home theater in a box (HTIB), DVD receivers, or plasma display panels (PDP).

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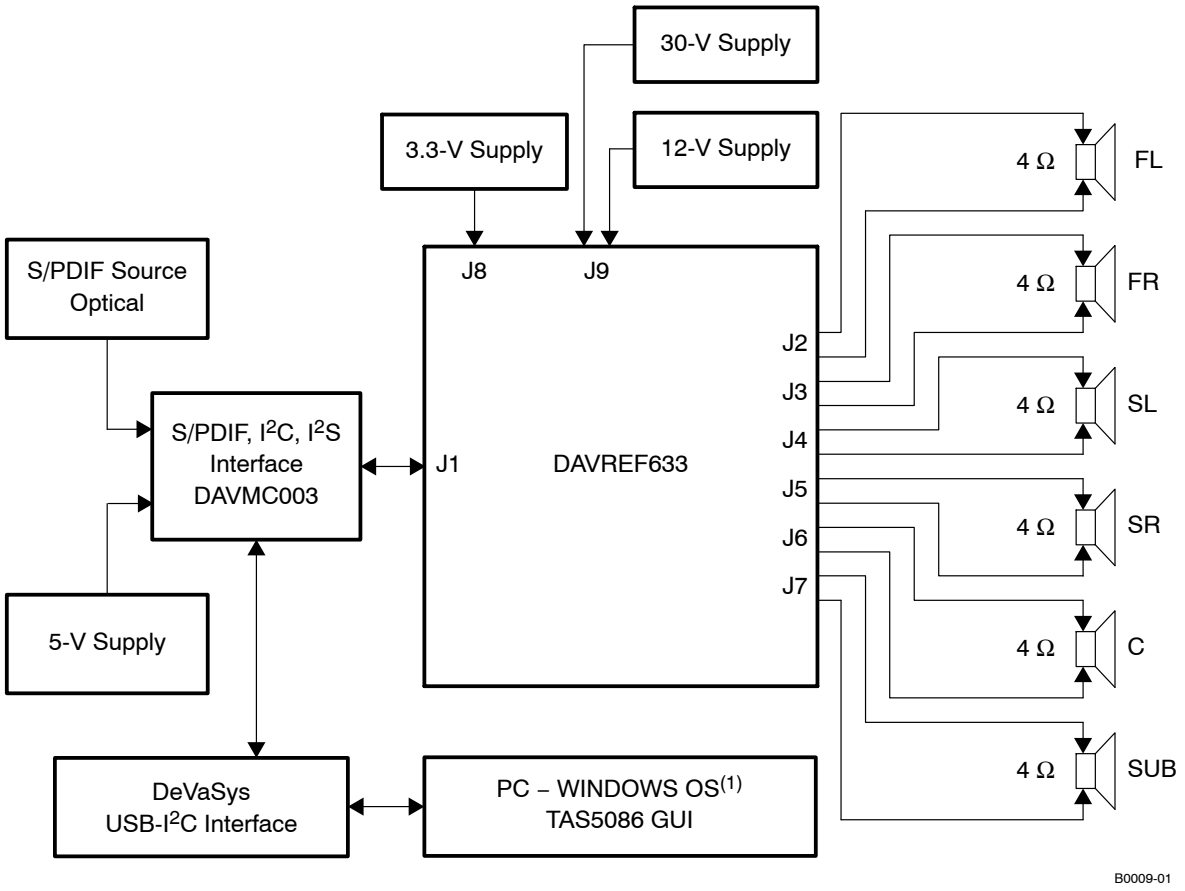
Figure 1–1. PurePath Digital System



(1) TAS5086 GUI can run on any Windows™ OS that supports USB.

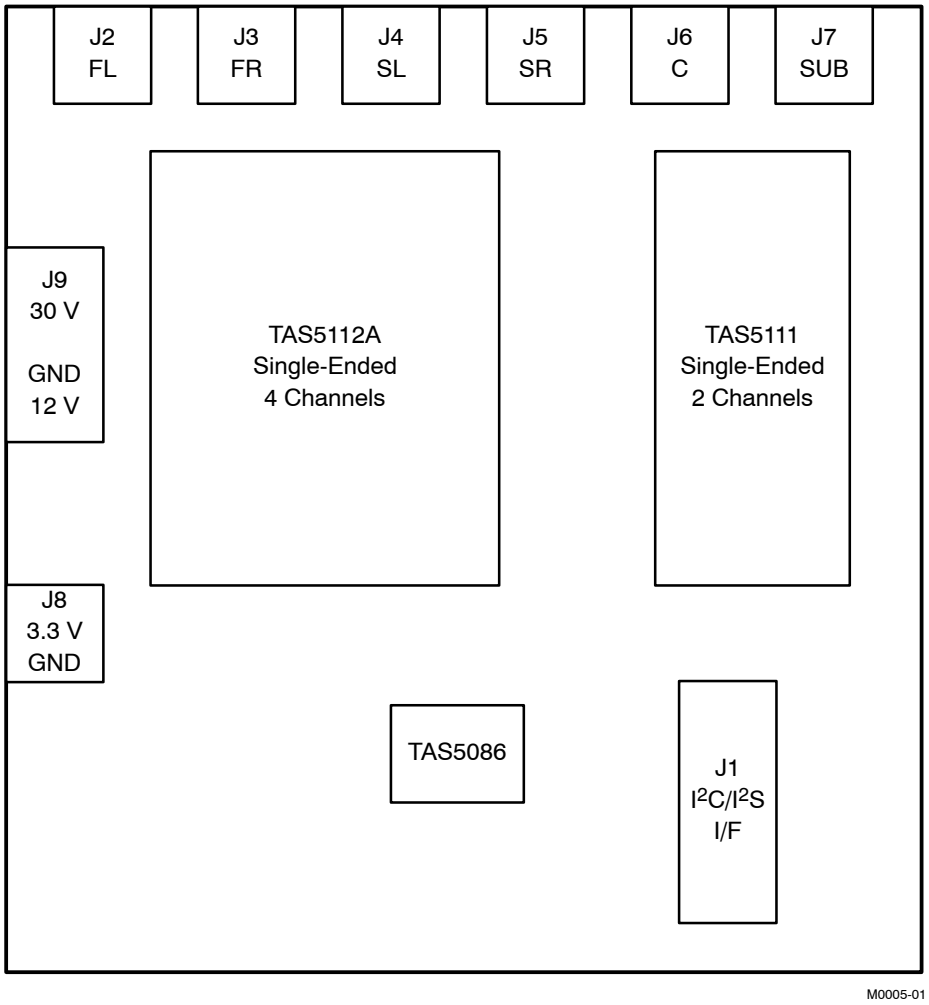
1.1 DAVREF633 Features

- 6-channel PurePath Digital reference design
- Self-contained protection system (short-circuit and thermal)
- Standard I^2S/I^2C control connector for TI input board
- Designed for double-sided, plated-through, two-layer PCB

1.2 Reference Layout

Layout for the DAVREF633 is illustrated in Figure 1−2.

Figure 1−2. Layout for the DAVREF633 (Rough Outline)



Chapter 2

System Interfaces

This chapter describes the DAVREF633 reference design relative to the power supply unit (PSU) and system interfaces.

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2.1 Power Stage-to-PSU Interface

The DAVREF633 reference design must be powered from three external regulated power supplies. High audio performance requires a stabilized output-stage power supply with low ripple voltage and low output impedance.

Note: The length of the power supply cable must be minimized. Increasing the length of the PSU cable increases the distortion for the amplifier at high output levels and low frequencies.

Maximum output-stage supply voltage depends on the speaker load resistance. Check the recommended maximum supply voltage in the TAS5111 and TAS5112A data sheets.

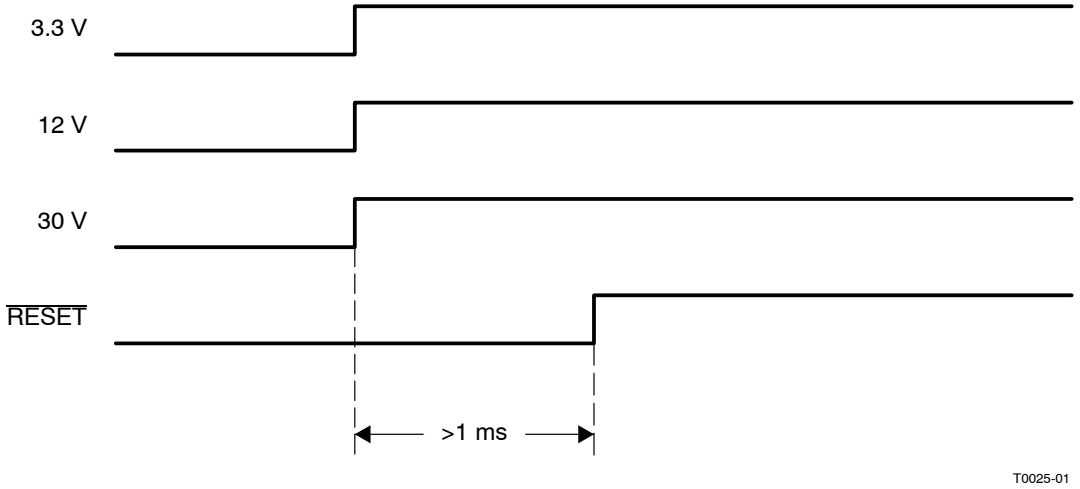
Table 2–1. Recommended Power Supplies

Description	Voltage Limitations (4–Ω to 8–Ω Load)	Current Recommendations
System power supply	3.3 V	0.25 A
Gate-drive supply	12 V	0.25 A
Output power-stage supply	0–30.5 V	5 A(1)

(1) The rated current corresponds to six channels full scale (25 W/4 Ω each), which is most likely adequate for a standard 6-channel amplifier design.

The recommended power-up sequence for both TAS5111 and TAS5112A is shown in Figure 2–1. For proper TAS5111/5112A operation, the $\overline{\text{RESET}}$ signal should be kept low during power up. $\overline{\text{RESET}}$ is pulled low for 200 ms during power up by the DAVMC003 S/PDIF–I^2S–I^2C interface board.

Figure 2–1. Recommended Power-Up Sequence



2.2 PSU Connector (J8)

Figure 2–2. J8 Pin Numbers (PCB Connector, Top View)

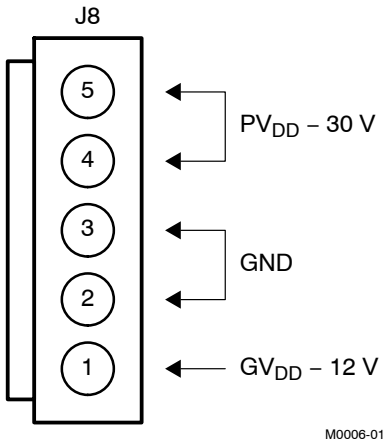


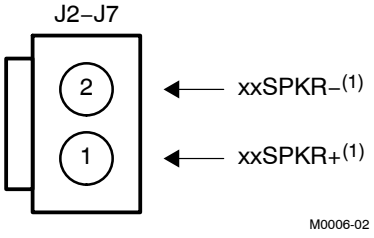
Table 2–2. J8 Pin Description

Pin	Net–Name in Schematics	Description
1	GVDD	Gate-drive power supply (12 V)
2	GND	Ground
3	GND	Ground
4	PVDD	Power-stage supply (30 V)
5	PVDD	Power-stage supply (30 V)

2.3 Loudspeaker Connectors (J2–J7)

Both positive and negative speaker outputs are floating and must not be connected to ground (e.g., through an oscilloscope).

Figure 2–3. J2–J7 Pin Numbers (PCB Connector, Top View)



(1) xx = FL, FR, SL, SR, C, or SUB

Table 2–3. J2–J7 Pin Description

Pin	Net–Name in Schematics	Description
1	xxSPKR+	Speaker positive output
2	xxSPKR–	Speaker negative output

2.4 Digital Power-Supply Connector (J9)

Figure 2–4. J9 Pin Numbers

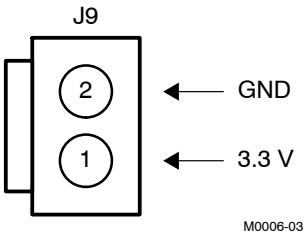


Table 2–4. J9 Pin Description

Pin	Net–Name in Schematics	Description
1	3.3 V	Digital power supply
2	GND	Ground

2.5 Digital Audio and Control Interface (J1)

The digital audio interface contains digital audio signal data (I^2S), clocks, serial control data, serial clock (I^2C), etc. See the preliminary TAS5086 data manual on the supplied CD for signal timing and details not explained in this document.

Table 2–5. J1 Pin Description

Pin	Net–Name in Schematics	Description
1	LRCLK	I^2S left-right clock
2	$\overline{\text{SHUTDOWN}}$	Power-stage shutdown when asserted
3	SCLK	I^2S bit clock
4	GND	Ground
5	SDIN2	I^2S data 2, channels 3 and 4
6	GND	Ground
7	SDIN3	I^2S data 2, channels 5 and 6
8	GND	Ground
9	SDIN1	I^2S data 2, channels 1 and 2
10	GND	Ground
11	MCLK	Master clock input. Low-jitter system clock for PWM generation and reclocking. Ground connection from source to TAS5086 must be a low-impedance connection.
12	GND	Ground
13	SCL	Serial clock – I^2C
14	GND	Ground
15	SDA	Serial data – I^2C
16	GND	Ground
17	$\overline{\text{MUTE}}$	Input mute signal. Mute when asserted
18	GND	Ground
19	$\overline{\text{RESET-IN}}$	Reset signal. Reset when asserted
20	3.3 V	3.3-V power supply input from DAVMC003

Chapter 3

Protection

This chapter provides a brief overview of the DAVREF633 fault-protection capabilities.

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3.1 Short-Circuit Protection and Fault-Reporting Circuitry

The TAS5111 and TAS5112A have a self-protecting circuit that provides device fault reporting (including high-temperature protection and short-circuit protection). The TAS5111 and TAS5112A are configured in power-stage autorecovery mode and therefore reset automatically after all errors (M1 and M2 are set low). This means that the device both restarts itself after an error occurs and reports through the $\overline{SD}$ error signal.

3.2 Device Fault Reporting

The $\overline{OTW}$ and $\overline{SD\_XX}$ outputs from TAS5111 and TAS5112A indicate fault conditions. See the TAS5111 and TAS5112A data sheets for a detailed description of these pins.

Chapter 4

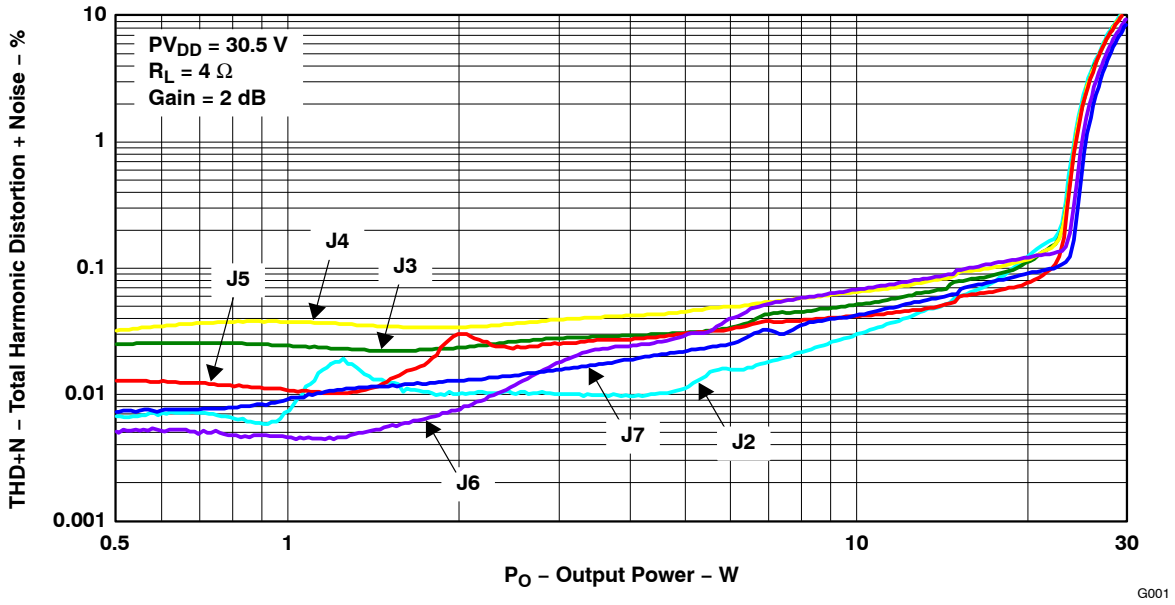
Performance Graphs

This chapter contains graphs showing various performance characteristics of the DAVREF633 reference design.

Topic **Page**

4.1 THD+N vs Power

Figure 4–1. THD+N vs Power



4.2 THD+N vs Frequency

Figure 4–2. THD+N vs Frequency at 0 dB

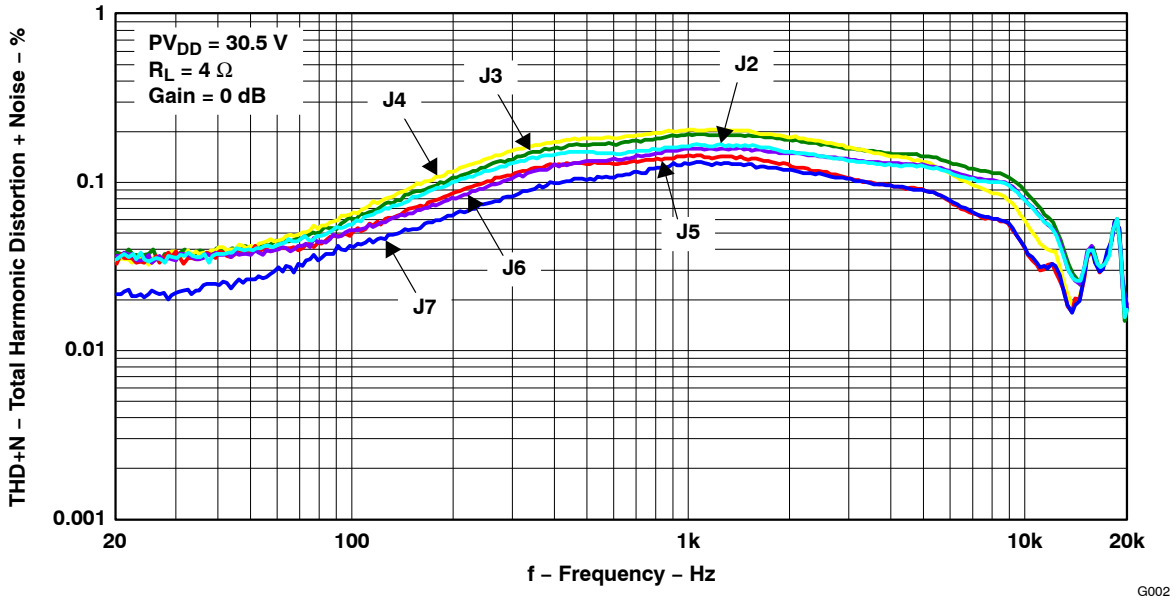
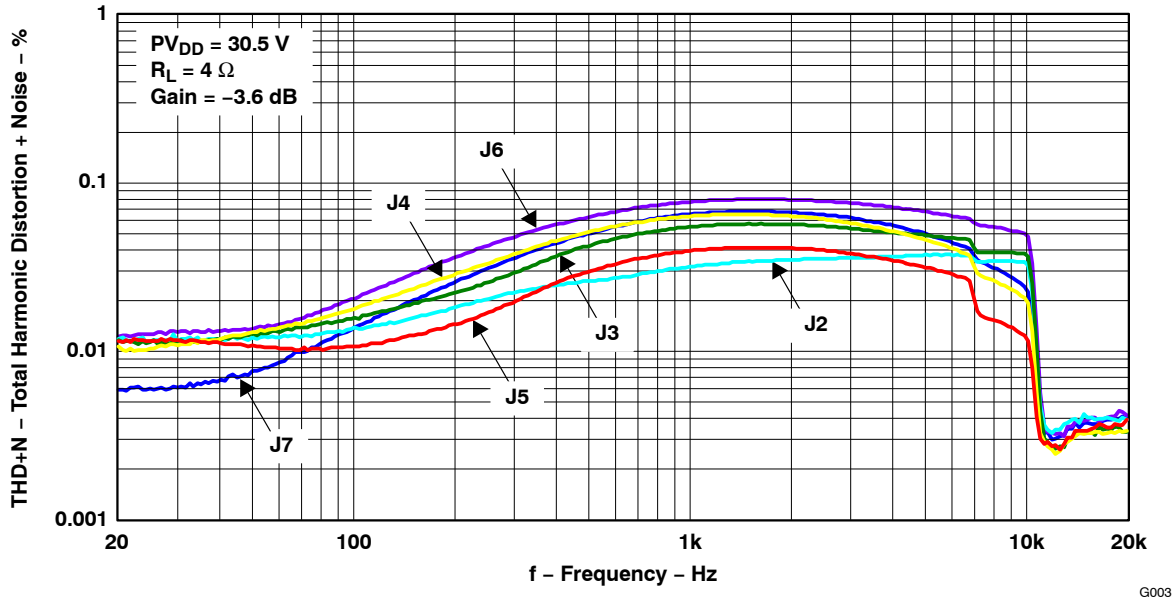
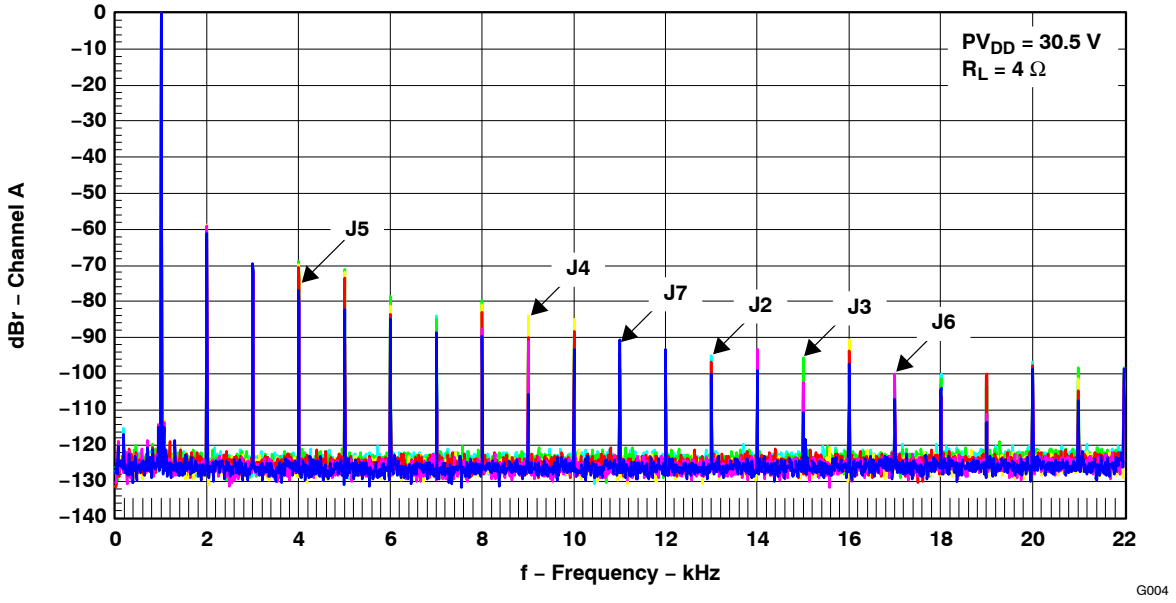


Figure 4–3. THD+N vs Frequency at 10 W



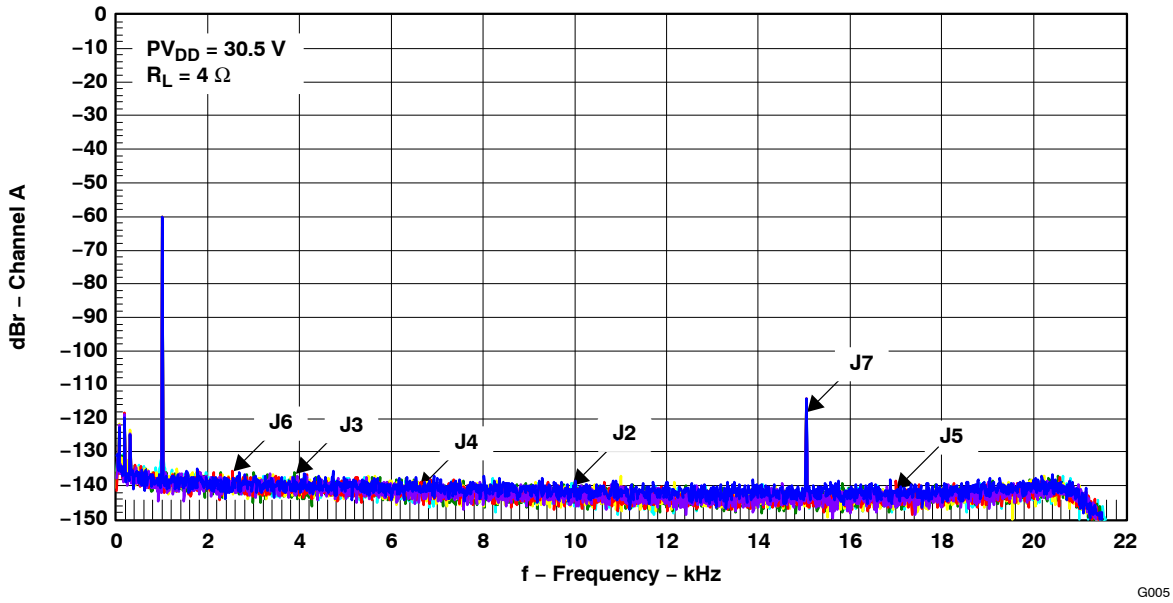
4.3 FFT

Figure 4–4. FFT, 1-kHz Sine Wave at 0 dB



4.4 FFT at –60 dB (Dynamic Range and Integrated Noise)

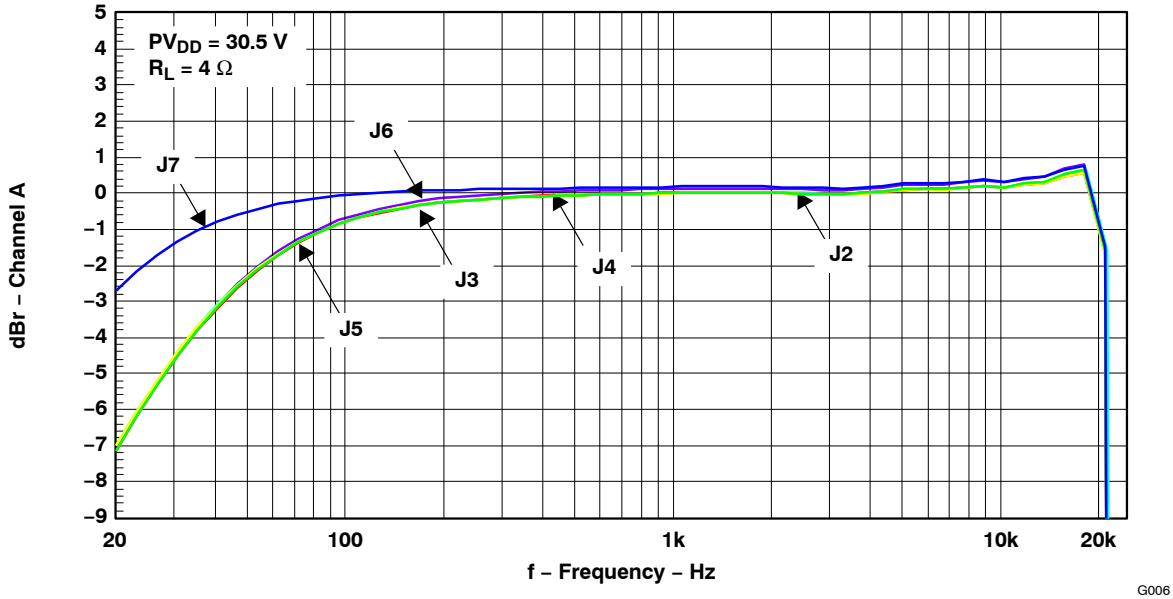
Figure 4–5. FFT, i-kHz Sine Wave at –60 dB



The 15-kHz tone will be significantly reduced in systems using the improved TAS5086.

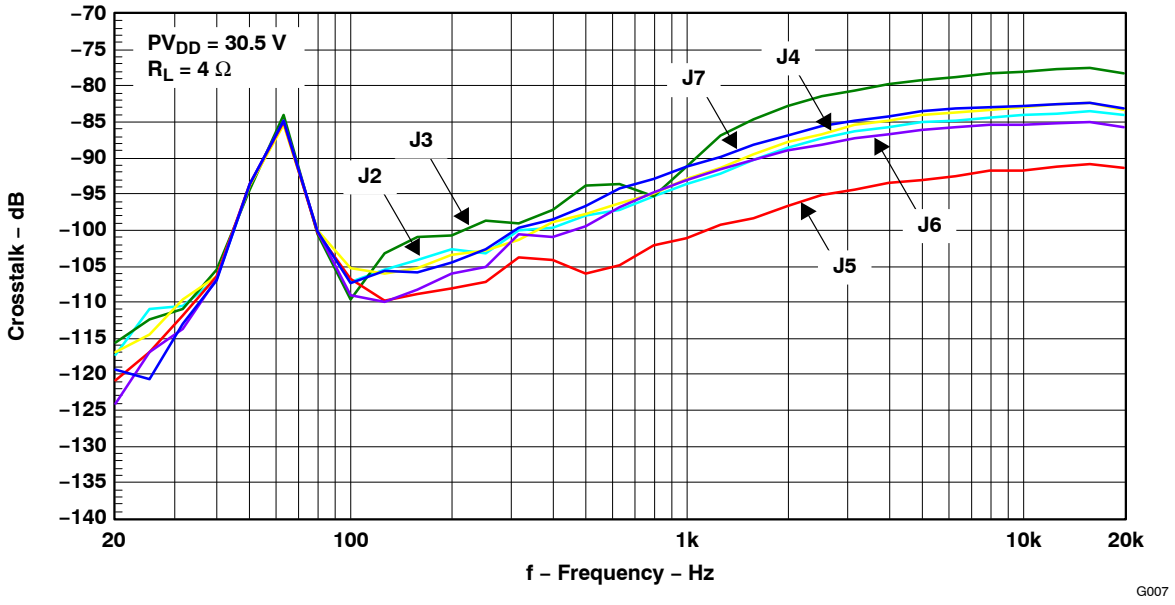
4.5 Frequency Response

Figure 4–6. Frequency Response



4.6 Crosstalk vs Frequency

Figure 4–7. Crosstalk vs Frequency



Chapter 5

System Setup and Debugging

This chapter provides information on setting up the DAVREF633 hardware for operation and on loading and configuring the PC software to run the board. There is also troubleshooting information for use in the event of a hardware malfunction.

Topic **Page**

5.1 Hardware Setup

1) Make sure all power supplies are in the off position.
2) Insert flat flex cable from DAVREF633 to DAVMC003 (S/PDIF–I^2S–I^2C) board.
3) Connect J2–J7 to appropriate speakers.
4) Connect S/PDIF optical source to DAVMC003 S/PDIF optical input.
5) Connect 5-V power supply to DAVMC003.
6) Connect J8 to 30-V and 12-V power supplies.
7) Connect J9 to 3.3-V power supply (optional, because 3.3 V is provided via DAVMC003).
8) Perform software setup (see Section 5.2).

5.2 Software Setup

1) Copy the TAS5086 GUI zip file from the CD supplied with this reference design to a temporary directory on the PC hard drive and unzip it.
2) Double-click on the setup executable file and follow instructions. Using the default settings is suggested.
3) Copy the TAS5086_DAVREF633_48KHz.cfg and TAS5086_ DAVREF633_44.1KHz.cfg files (located on the included CD) to the TAS5086 GUI directory (C:\Program Files\Texas Instruments Inc\ TAS5086 GUI 1.0).
4) Plug in a USB cable from a PC with Windows operating system to the DeVaSys USB-I^2C board.
5) When the USB driver is prompted by the Windows OS, direct the OS to the C:\Program Files\Texas Instruments Inc\TAS5086 GUI 1.0 directory. The USB driver for the DeVaSys board was loaded in this directory by GUI setup (Step 2).
6) By now, the USB interface board should be communicating with the Windows OS. Connect the 8-pin DIN (I^2C) connector from the USB interface board (DeVaSys) to DAVMC003.
7) Turn on the power supplies in the following sequence: 3.3-V (optional), 5-V, 12-V and 30-V.
8) Run the TAS5086 GUI.
9) When the GUI is loaded, select the file pulldown menu and then select File→Load→Config File. Select the appropriate configuration file (48 KHz and 44.1 KHz refer to sampling frequency). The TAS5086 must be receiving the appropriate clocks (SCLK, LRCLK, and MCLK) and the input sample frequency must match the configuration file, i.e., if you use 48-kHz Fs, you must select TAS5086_DAVREF633_48KHz.cfg. **IMPORTANT NOTE: To prevent possible system failure, the configuration file should not be loaded a second time without first resetting both hardware and software.**
10) On the GUI, adjust to desirable volume.
11) On the S/PDIF source, start streaming audio.
12) If the audio does not get to the speaker, push the RESET button on the DAVMC003.
13) On the TAS5086 GUI, click on RESET. Then follow Step 9 above.

5.3 Debugging

For troubleshooting purposes, the tables of this section provide information on the proper voltage/signal at specific locations and suggestions as to the possible cause if the observed condition is incorrect.

Check the J1 interface using Table 5−1.

Table 5−1. Debugging the DAVREF633 Digital Interface

Pin	Name	Check For	Possible Cause
1	LRCLK	44.1− or 48−kHz clock at 3.3 V	There should be a clean 3.3-V, 44.1-kHz clock (CD), 48-kHz clock (DVD), or other clock rate (MP3). If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
2	$\overline{\text{SHUTDOWN}}$	3.3 V	Ensure there are no faults, i.e., OTE or OC.
3	SCLK	≈3-MHz clock at 3.3 V	There should be a clean 3.3-V, ≈3-MHz clock. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
4	GND	0 V	If it is not at 0 V, power and ground may be shorted.
5	SDIN2	3.3-V data	There should be I^2S data at 3.3 V. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
6	GND	0 V	If it is not at 0 V, power and ground may be shorted.
7	SDIN3	3.3-V data	There should be I^2S data at 3.3 V. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
8	GND	0 V	If it is not at 0 V, power and ground may be shorted.
9	SDIN1	3.3-V data	There should be I^2S data at 3.3 V. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
10	GND	0 V	If it is not at 0 V, power and ground may be shorted.
11	MCLK	12.288 MHz at 3.3 V	MCLK is a 3.3-V master clock input. There should be a clock of 12.288 MHz at 48-kHz Fs. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
12	GND	0 V	If it is not at 0 V, power and ground may be shorted.
13	SCL	3.3-V clock	Move the volume control on the TAS5086 GUI. The serial waveform should be present on this pin.
14	GND	0 V	If it is not at 0 V, power and ground may be shorted.
15	SDA	3.3-V data	Move the volume control on the TAS5086 GUI. The serial waveform should be present on this pin.
16	GND	0 V	If it is not at 0 V, power and ground may be shorted.
17	$\overline{\text{MUTE}}$	3.3 V	Make sure that this signal is not asserted. Make sure the pin is not shorted. There should be a pullup resistor to the 3.3-V supply.
18	GND	0 V	If it is not at 0 V, power and ground may be shorted.
19	$\overline{\text{RESET-IN}}$	3.3 V	Make sure that this signal is not asserted. Make sure the pin is not shorted. There should be a pullup resistor to the 3.3-V supply.
20	3.3V	3.3 V	If 3.3-V level is not present, ensure power supply is on and check for voltage regulator malfunction on DAVMC003.

Check the TAS5086 pins using Table 5–2.

Table 5–2. Debugging the TAS5086

Pin	Name	Check For	Possible Cause
1	VR_ANA	1.8 V	If 1.8 V is not present, device may be damaged.
2	AVDD	3.3 V	If 3.3-V is not present, ensure power supply is on and check for voltage regulator malfunction on DAVMC003.
3	AVSS	0 V	If it is not at 0 V, power and ground may be shorted.
4	AVSS_GR	0 V	If it is not at 0 V, power and ground may be shorted.
5	PLL_FLTM	0 V	If it is not at 0 V, power and ground may be shorted.
6	PLL_FLTP	≈0.9 V	If this voltage is not present, device may be damaged.
7	AVSS	0 V	If it is not at 0 V, power and ground may be shorted.
8	MCLK	12.288 MHz at 3.3 V	MCLK is a 3.3-V clock master clock input. There should be a clock of 12.288 MHz at 48-kHz Fs. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
9	$\overline{\text{RESET}}$	3.3 V	Make sure that this signal is not asserted. Make sure the pin is not shorted. There should be a pullup resistor to the 3.3-V supply.
10	$\overline{\text{PDN}}$	3.3 V	Make sure that this signal is not asserted. Make sure the pin is not shorted. There should be a pullup resistor to the 3.3-V supply.
11	DVDD	3.3 V	If 3.3 V is not present, check to see if power supply is on or if voltage regulator on DAVMC003 is not functioning. Also check for possible shorts between power and ground.
12	DVSS	0 V	If it is not at 0 V, power and ground may be shorted.
13	DVSS_OSC	0 V	If it is not at 0 V, power and ground may be shorted.
14	OSC_RES	≈1 V	Oscillator trim resistor. If 1 V is not present, device may be damaged.
15	VR_OSC	1.8 V	If 1.8 V is not present, device may be damaged.
16	$\overline{\text{MUTE}}$	3.3 V	Make sure that this signal is not asserted. Make sure the pin is not shorted. There should be a pullup resistor to the 3.3-V supply.
17	SDA	3.3-V data	Move the volume control on the TAS5086 GUI. The serial data should be present on this pin.
18	SCL	3.3-V clock	Move the volume control on the TAS5086 GUI. The serial waveform should be present on this pin.
19	LRCLK	44.1- or 48-kHz clock at 3.3 V	There should be a clean 3.3-V, 44.1-kHz clock (CD), 48-kHz clock (DVD), or other clock rate (MP3). If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
20	SCLK	≈3-MHz clock at 3.3 V	There should be a clean 3.3-V, ≈3-MHz clock (depending on Fs). If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
21	N/A	N/A	Reserved pin
22	SDOUT	N/A	It is not used on this reference design.
23	SDIN4	N/A	It is not used on this reference design.

Table 5–2. Debugging the TAS5086 (continued)

Pin	Name	Check For	Possible Cause
24	SDIN3	3.3-V data	There should be I^2S data at 3.3 V. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
25	SDIN2	3.3-V data	There should be I^2S data at 3.3 V. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
26	SDIN1	3.3-V data	There should be I^2S data at 3.3 V. If not, check for shorts or possible damage to DIR1703 on DAVMC003 board.
27	$\overline{\text{BKND\_ERR}}$	3.3 V	Make sure this signal is not asserted. If it is asserted, check for a power-stage error. See power-stage debugging, Table 5–3.
28	$\overline{\text{VREG\_EN}}$	0 V	If it is not at 0 V, power and ground may be shorted.
29	DVSS_ESD	0 V	If it is not at 0 V, power and ground may be shorted.
30	VR_DIG	1.8 V	If 1.8 V is not present, device may be damaged.
31	VALID2	3.3 V	Make sure this signal is high (3.3 V). If not, check for possible power-stage errors or the system is in RESET or PDN.
32	VALID1	3.3 V	Make sure this signal is high (3.3 V). If not, check for possible power-stage errors or the system is in RESET or PDN.
33	PWM_ 6	3.3–V PWM	There should be PWM signal switching at 3.3 V. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
34	PWM_ 5	3.3–V PWM	There should be PWM signal switching at 3.3 V. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
35	PWM_ 4	3.3–V PWM	There should be PWM signal switching at 3.3 V. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
36	PWM_ 3	3.3–V PWM	There should be PWM signal switching at 3.3 V. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
37	PWM_ 2	3.3–V PWM	There should be PWM signal switching at 3.3 V. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
38	PWM_ 1	3.3–V PWM	There should be PWM signal switching at 3.3 V. If not, check for power-tage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.

Check the TAS5111 pins using Table 5–3 (TAS5112A is similar to TAS5111).

Table 5–3. Debugging the Power Stage

Pin	Name	Check For	Possible Cause
1	PWM_BP	3.3-V PWM	PWM switching input from TAS5086 at 3.3-V swing. On TAS5086: check for mute signal if it is 50% duty cycle; check for reset, power-down signals if it is 0 V.
2	GND	0 V	If it is not at 0 V, power and ground may be shorted.
3	$\overline{\text{RESET}}$	3.3 V	Make sure that this signal is not asserted. Make sure the pin is not shorted.
4	DREG_RTN	0 V	If it is not at 0 V, power and ground may be shorted.
5	GREG	12 V	If it is not at 12 V, check power-supply connection. Also check to see if power and ground are shorted.
6	M3	3.3 V	SE configuration. If the voltage is not there, this pin may be grounded by mistake. This pin should be pulled up to 3.3 V.
7	DREG	≈3.3 V	If it is not at 3.3 V, device may be damaged.
8	DGND	0 V	If it is not at 0 V, power and ground may be shorted.
9	M1	0 V	Set for autorecovery with M2 = 0 V
10	M2	0 V	Set for autorecovery with M1 = 0 V
11	DVDD	3.3 V	If 3.3 V is not present, check to see if power supply is on or if voltage regulator on DAVMC003 is not functioning. Also check for possible shorts between power and ground.
12	$\overline{\text{SD}}$	3.3 V	Make sure there is no fault, i.e., OTE or OC.
13	DGND	0 V	If it is not at 0 V, power and ground may be shorted.
14	$\overline{\text{OTW}}$	3.3 V	Check for high temperature if this signal is asserted.
15	GND	0 V	If it is not at 0 V, power and ground may be shorted.
16	PWM_AP	3.3-V PWM	PWM switching input from TAS5086 at 3.3-V swing. On TAS5086: check for mute signal if it is 50% duty cycle; check for reset, power–down signals if it is 0 V.
17	GVDD	12 V	If it is not at 12 V, check power-supply connection. Also check to see if power and ground are shorted.
18	GND	0 V	If it is not at 0 V, power and ground may be shorted.
19	BST_A	12 V + 30-V PWM	External PCB connections incorrect or problem with integrated circuit.
20	PVDD_A	30 V	If it is not at 30 V, check power supply connection. Also check to see if power and ground are shorted.
21	PVDD_A	30 V	If it is not at 30 V, check power supply connection. Also check to see if power and ground are shorted.
22	OUT_A	30-V PWM	There should be PWM signal switching at 30-V swing. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
23	OUT_A	30-V PWM	There should be PWM signal switching at 30-V swing. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
24	GND	0 V	If it is not at 0 V, power and ground may be shorted.
25	GND	0 V	If it is not at 0 V, power and ground may be shorted.

Table 5–3. Debugging the Power Stage (continued)

26	OUT_B	30-V PWM	There should be PWM signal switching at 30-V swing. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
27	OUT_B	30-V PWM	There should be PWM signal switching at 30-V swing. If not, check for power-stage errors, system in reset, power down, or mute. When mute, the PWM is switching at 50% duty cycle.
28	PVDD_B	30 V	If it is not at 30 V, check power supply connection. Also check to see if power and ground are shorted.
29	PVDD_B	30 V	If it is not at 30 V, check power supply connection. Also check to see if power and ground are shorted.
30	BST_B	12 V + 30-V PWM	External PCB connections incorrect or problem with integrated circuit.
31	GND	0 V	If it is not at 0 V, power and ground may be shorted.
32	GVDD	12 V	If it is not at 12 V, check power supply connection. Also check to see if power and ground are shorted.

Chapter 6

Bill of Materials, Layout, and Schematics

This chapter contains the bill of materials required to build the DAVREF633, the layout information for its circuit board, and the schematics needed for construction and use of the design reference.