Application Report
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LVPECL and LVDS Power Comparison

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ABSTRACT

Emitter-coupled logic (ECL) (including, positive ECL (PECL), and low voltage PECL (LVPECL)) interfacing, often the first solution considered when a high-speed interface is needed, suffers from high power consumption. TIA/EIA-644 low voltage differential signaling (LVDS) provides a low-power alternative to ECL when selecting a high-speed interface solution. This paper compares the power consumption of LVPECL and LVDS, using representative parts operating from 50 Mbps to 600 Mbps.

Introduction

This paper compares the power consumption of LVPECL and LVDS devices. The devices tested are an LVPECL 10-channel clock driver (MC100LVEP111) and an LVDS 16-channel repeater (SN65LVDS116). The results of the LVPECL and LVDS testing show the dynamic nature of the LVDS power consumption and the static nature of LVPECL power consumption over frequency. The results also reveal that LVDS considerably outperforms both the 2.5-V and 3.3-V operation of the LVPECL device in terms of power consumption.

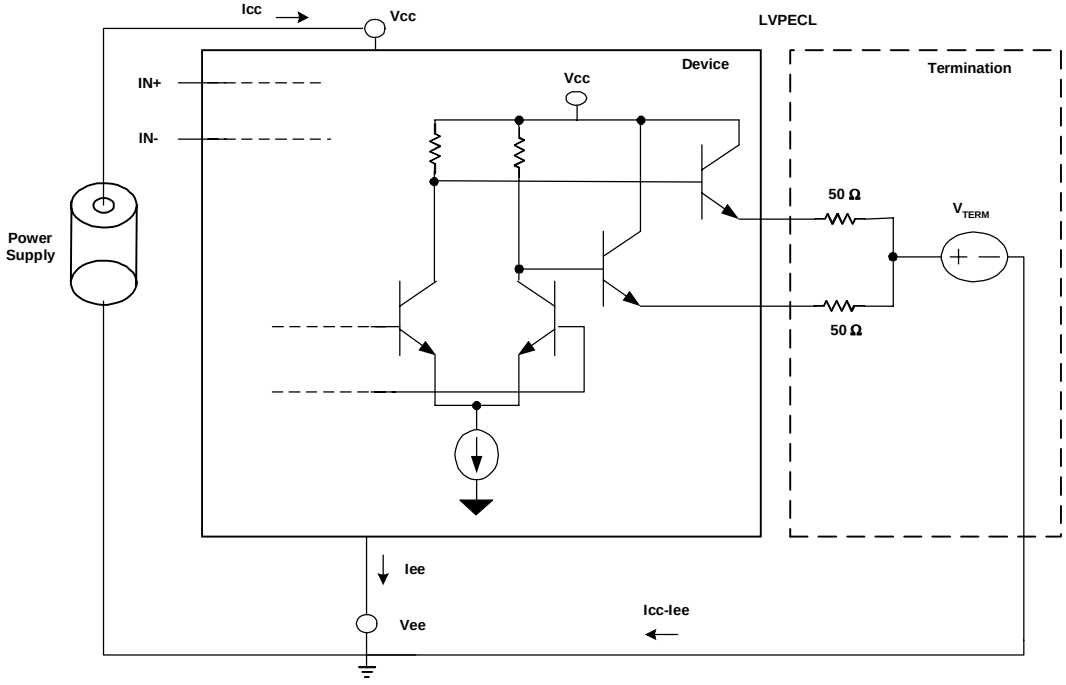

Figure 1. LVPECL Setup

Figure 1 shows the required power connections (Vcc and Vee) and the recommended termination for an LVPECL driver. Power dissipation within the device corresponds to the voltage drop and current from Vcc to Vee and Vcc to the Outputs. Power is also dissipated in the termination. The termination must be included when determining the power needed to move data or clock signals.

1:10 LVPECL and the 1:16 LVDS Repeater Measurements

The intention of the following measurements is to demonstrate the total power consumption of a transmission system. This total view of power gives the designer an accurate account of power budget allocation and cooling requirements in a system. Also, this testing is intended to reinforce one of the key benefits of LVDS: low power consumption. See Appendixes A and B for the test setups and table of results.

Figure 2 illustrates the measured power consumption versus signaling rate. The LVDS 16-channel repeater has a distinct power advantage over the LVPECL 10-channel repeater, and at some frequencies the power dissipation of LVPECL is three times that of LVDS.

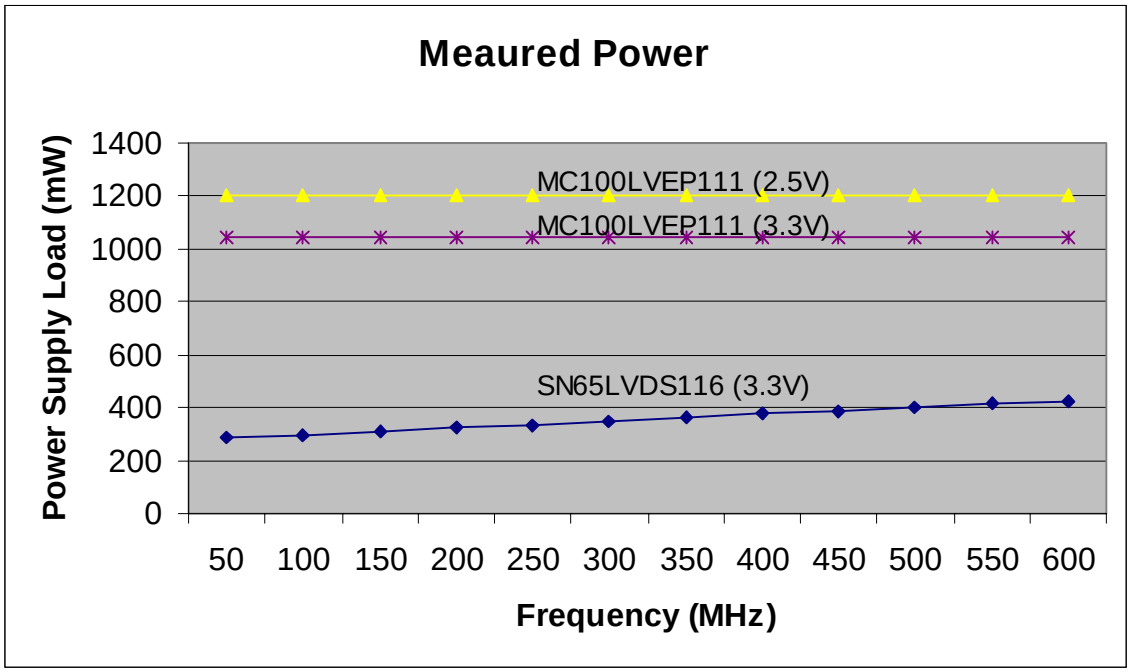

Figure 2. Measured Power

As shown in Figure 2, the power consumption of the LVPECL device is greater in 2.5-V operation than in 3.3-V operation. This result is due to the different terminations recommended in the data sheet for the 2.5-V and 3.3-V operation. The 3.3-V device outputs are terminated into Vcc-2V resulting in a 2-volt drop from Vcc to V_{TERM} (see Appendix A). The 2.5-V device is terminated into 0V (GND), which results in a larger voltage drop (2.5 V) between Vcc and V_{TERM}.

Conclusion

A comparison of power requirements for transmitting signals must include the termination. When included in a comparison between LVDS and LVPECL, LVDS provides more channels (16 versus 10) and requires less power than LVPECL when operating over 50 to 600 Mbps (20 to 300MHz clocks).

Appendix A. 1:10 LVPECL Repeater Test Setup and Results

Figure 3 shows the layout for testing the 1:10 LVPECL repeater. The input source is a high frequency synthesizer (HFS), which has an upper signaling rate limit of 630 Mbps. The recommended load, V_{TERM}, and input values are used to stimulate the device under test. Since the device offers two input channels, both input paths are tested, and the average power consumption is computed.

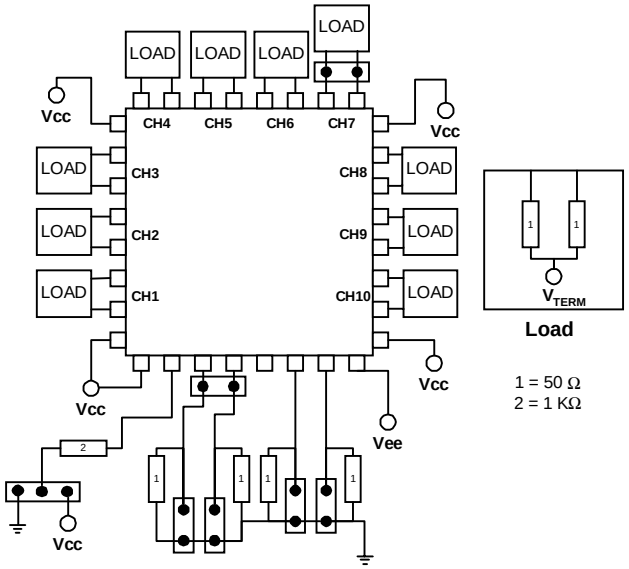

Figure 3. 1:10 LVPECL Test Setup

Table 1. LVPECL Test Results

V_{cc} (V)	V_{TERM}* (V)	Signaling Rate (Mbps)	I_{cc} (mA) CLK_SEL=0	I_{cc} (mA) CLK_SEL=1	Total Power (mW)
3.3	1.3	50	316	316	1043
3.3	1.3	300	316	315	1041
3.3	1.3	600	316	316	1043
2.5	0	50	480	480	1200
2.5	0	300	480	480	1200
2.5	0	600	480	480	1200

*V_{TERM} is the recommended value from the data sheet.

$$P_{TOTAL}(ECL) = Vcc * Icc \quad \text{.....Equation.1}$$

Appendix B. 1:16 LVDS Repeater Test Setup and Results

Figure 4 shows the test setup for the SN65LVDS116. The input stimulus is the same HFS device used on the LVPECL repeater and the inputs correspond to the recommended data sheet values.

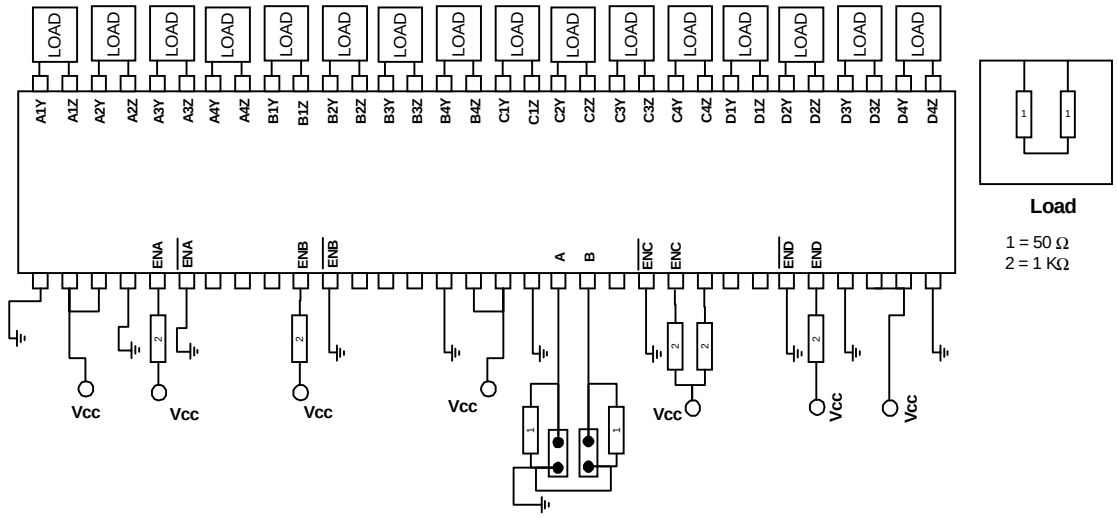

Figure 4. 1:16 LVDS Test Setup

Table 2. LVDS Test Results

Vcc (V)	Signaling Rate (Mbps)	Icc (mA)	Total Power (mW)
3.3	50	86	283
3.3	100	89	296
3.3	150	93	309
3.3	200	97	322
3.3	250	102	336
3.3	300	106	349
3.3	350	110	363
3.3	400	113	375
3.3	450	117	388
3.3	500	121	401
3.3	550	125	414
3.3	600	129	426

$$P_{TOTAL}(LVDS) = Vcc * Icc \quad \text{.....Equation.2}$$

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