Comparing the PCI2050B to the PCI2050

PCI Bus Solutions

ABSTRACT

This document discusses the differences between the PCI2050 and the PCI2050B. In general, the PCI2050 and the PCI2050B are very similar. They both support up to 9 masters on the secondary interface and they both support up to 3 delayed transactions. The main difference between the PCI2050 and the PCI2050B is that the PCI2050B supports 66MHz. Also, all errata of the PCI2050 are fixed in the PCI2050B.

Contents

List of Figures

List of Tables

1 PCI2050B Overview

The PCI2050B is a PCI-to-PCI bridge that provides a connection between two independent 32-bit PCI buses operating at a maximum bus frequency of 66MHz. The following clock frequency combinations are supported in PCI2050B:

- 66 MHz primary Bus, 66 MHz secondary bus
- 66 MHz primary Bus, 33 MHz secondary bus
- 33 MHz primary Bus, 33 MHz secondary bus

The PCI2050B does not support primary bus at 33 MHz and secondary bus at 66 MHz, where the secondary bus is running twice the frequency of the primary bus.

In addition to incorporating 66 MHz clock speed in PCI2050B, the following PCI2050 erratas are fixed.

- De-bounce of HS_SWITCH#
- JTAG TAP controller
- Master Discard Timer Errata

The PCI2050B device is compatible with the Intel 21150-BC device, and can be used as a drop-in replacement for 32-bit 33MHz/66MHz 21150-BC applications. The PCI2050B is also compatible with PCI Local Bus Specification 2.2.

An advanced CMOS process is used to achieve low system-power consumption. PCI2050B is available in the 208 LQFP, and is designed to meet industrial specifications.

2 Symbolization Difference

Part Name	Symbol	Revision ID	Description
PCI2050	PCI2050PDV	00h	Up to 33MHz capable
PCI2050B	PCI2050BPDV	01h	Up to 66MHz capable

3 Input/Output Changes

The 66 MHz clocking requires three terminals P_M66ENA, S_M66ENA and CONFIG66. S_M66ENA is already present on PCI2050. It was implemented as an output that is always driven low to indicate secondary bus speed is 33MHz. The functionality associated with this pin will change per section 3.1 for the PCI2050B. P_M66ENA and CONFIG66 were implemented as no-connects in PCI2050.

Table 1. PCI2050B Terminals that Differ from PCI2050

PDV	Terminal Name	Changes
102	P_M66ENA	P_M66ENA will change from NC
125	CONFIG66	CONFIG66 will change from NC

3.1 Terminal Functions

This section describes the PCI2050B terminal functions for terminals that differ from the PCI2050 device.

Name	PDV	Type	Function
CONFIG66	125	I	Configure 66 MHz Operation. This input-only pin is used to specify if PCI2050B is capable of running at 66 MHz. If this terminal is tied high, then device can be run at 66 MHz. If this pin is tied low, then PCI2050B can only function under the 33 MHz PCI specification.
P_M66ENA	102	I	Primary interface 66 MHz Enable. This input-only signal pin is used to designate the primary interface bus speed. This signal should be pulled low for 33MHz operation on the primary bus. In this case S_M66ENA signal will be driven low by the PCI2050B, forcing the secondary bus to run at 33 MHz. For 66 MHz operation, this signal should be pulled high.
S_M66ENA	153	I/O	Secondary 66 MHz Enable. This signal is used to designate the secondary bus speed. If the P_M66ENA is driven low, then this signal is driven low by the PCI2050B forcing secondary bus to run at 33MHz. If the primary bus is running at 66MHz (P_M66ENA is high), then S_M66ENA is an input and should be externally pulled high for the secondary bus to operate at 66 MHz or pulled low for secondary bus to operate at 33 MHz. Please note that S_M66ENA is an open drained output.

3.2 Input/Output Cells

The S_M66ENA is a shared terminal on the secondary bus and can be driven by more than one agent on the secondary bus. It is implemented as open drain output on the PCI2050B.

4 66MHz Operation

To enable 66 MHz operation, the signal CONFIF66 must be tied high on the board. This would set the 66 MHz capable bit in the primary and secondary status register. To be compliant with Intel's 21150 part, P_M66ENA and S_M66ENA should never be pulled high unless CONFIG66 is also high.

The signals P_ M66ENA and S_ M66ENA indicate whether the primary or secondary interfaces are working at 66 MHz. This information is needed to control the frequency of the secondary bus. Note that PCI Local Bus Specification 2.2 restricts clock frequency changes above 33 MHZ to during reset only. The following frequency combinations are supported on the primary and secondary buses in PCI2050B:

Table 2. Frequency Truth Table

P_M66ENA	S_M66ENA	CONFIG66	Primary Bus Frequency	Secondary Bus Frequency
Low	Low	Low	33 MHz	33 MHz
Low	Low	High	33 MHz	33 MHz
High	Low	High	66 MHz	33 MHz
High	High	High	66 MHz	66 MHz

The PCI2050B does not support 33 MHz primary/66 MHz secondary bus operation. If CONFIG66 is high and P_M66ENA is low, the PCI2050B pulls down S_M66ENA to indicate that secondary bus is running at 33 MHz. The 2050B generates the clock signals S_CLKOUT[9:0] for the secondary bus devices and its own interface. It divides the P_CLK by two to generate the secondary clock outputs whenever the primary bus is running at 66 MHz and secondary bus is running at 33 MHz as shown below.

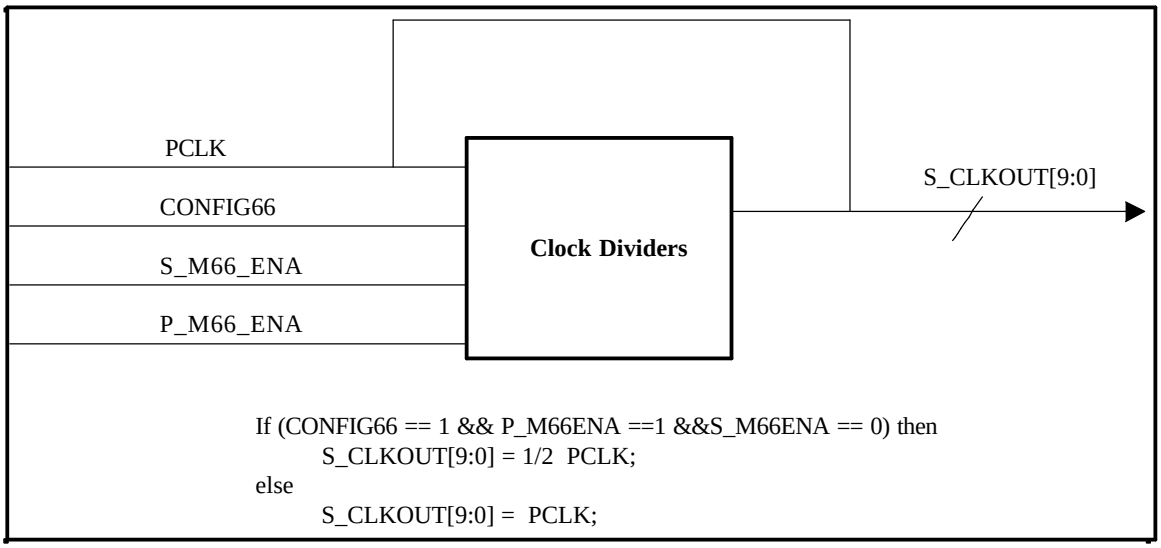

Figure 1. Clock Divider

Note that the bus drivers for 66 MHz meet the same DC characteristics and AC drive points as the 33 MHz PCI bus drivers. However 66 MHz drivers require the faster timing parameters and redefined conditions. Please consult PCI Local Bus Specification Rev. 2.2 for more details.

5 Configuration Space Register Changes

This section describes the changes in the configuration registers from the PCI2050 data sheet.

5.1 Primary Status Register – PCI Register 06h

Table 3. Bit Descriptions – Primary Status Register

Bit	Field Name	Access	Description
15:6	See 2050 Data Sheet	R & R/W	Same as PCI2050. No change required.
5	66-MHz capable	R	66-MHz capable. Indicates whether the primary interface is 66 MHz capable. Reads as 0 when CONFIG66 is tied low to indicate that PCI2050B is not 66 MHz capable. Reads as 1 when CONFIG66 is tied high to indicate that the primary bus is 66 MHz capable.
4:0	See 2050 Data Sheet	R	Same as PCI2050. No change required.

5.2 Revision ID Register – PCI Register 08h

The default value for the Revision ID register is 01h for PCI2050B. The Revision ID for the PCI2050 is 00h.

5.3 Secondary Status Register – PCI Register 1Eh

Table 4. Bit Descriptions – Secondary Status Register

Bit	Field Name	Access	Description
15:6	See 2050 Data Sheet	R & R/W	Same as PCI2050. No change required.
5	66-MHz capable	R	66-MHz capable. Indicates whether the primary interface is 66 MHz capable. Reads as 0 when CONFIG66 is tied low to indicate that PCI2050B is not 66 MHz capable. Reads as 1 when CONFIG66 is tied high to indicate that the primary bus is 66 MHz capable.
4:0	See 2050 Data Sheet	R	Same as PCI2050. No change required.

5.4 TI Diagnostics Register – PCI Register F0h

Table 5. Bit Descriptions – TI Diagnostics Register

Bit	Field Name	Access	Description
15:1	See 2050 Data Sheet	R	Same as PCI2050. No change required.
0	DISABLE_PW_COMBINE	R/W	DISABLE_PW_COMBINE 0: Enable write combining feature (Default) 1: Disable write combining feature

5.5 Primary FIFO BIST Register – PCI Register F8h

This register is used for internal testing of FIFOs.

Table 6. BIT Descriptions – Primary FIFO BIST Register

Bit	Field Name	Access	Description
31	BIST_EN	R/W	Built In Self Test Enable. When set the BIST function is enable. This bit is self clearing when the BIST completes.
25:24	FAILURE_CODE	R	Pass Fail Code. This two bit field is used to communicate the results of BIST. 00 - Pass 01 - Failed Initialization Pattern 10 - Failed Test Pattern Write Verification 11 - Failed Inverted Test Pattern Verification
10:8	SRAM_SELECT	R	SRAM Select. This three bit field is used to communicate which of the four SRAM's have failed BIST. 000 - Delay Posted Write FIFO 001 - Completion 0 FIFO 010 - Completion 1 FIFO 011 - Completion 2 FIFO 100 - Delay Posted Write Parity FIFO
7:0	OFFSET	R	Offset Address. This field contains the 2 Kbyte address that is currently being accessed by the BIST logic. After a failure, this field will contain the address of the failing DWord.

5.6 Secondary FIFO BIST Register – PCI Register FCh

This register is used for internal testing of FIFOs.

Table 7. BIT Descriptions – Secondary FIFO BIST Register

Bit	Field Name	Access	Description
31	BIST_EN	R/W	Built In Self Test Enable. When set the BIST function is enable. This bit is self clearing when the BIST completes.
25:24	FAILURE_CODE	R	Pass Fail Code. This two bit field is used to communicate the results of BIST. 00 - Pass 01 - Failed Initialization Pattern 10 - Failed Test Pattern Write Verification 11 - Failed Inverted Test Pattern Verification
10:8	SRAM_SELECT	R	SRAM Select. This three bit field is used to communicate which of the four SRAM's have failed BIST. 000 - Delay Posted Write FIFO 001 - Completion 0 FIFO 010 - Completion 1 FIFO 011 - Completion 2 FIFO 100 - Delay Posted Write Parity FIFO
7:0	OFFSET	R	Offset Address. This field contains the 2 Kbyte address that is currently being accessed by the BIST logic. After a failure, this field will contain the address of the failing DWord.

6 Fixed Errata From PCI2050

6.1 De-Bounce HS_SWITCH ERRATA

The PCI2050B's HS_SWITCH# terminal incorporates de-bounce logic to have minimum of 2ms of de-bounce. This de-bounce logic was not implemented in PCI2050.

6.2 JTAG TAP Controller Errata

In PCI2050, the JTAG Test Access Port controller makes an improper transition after writing to the instruction register. The TAP controller should transition to Data Register on 1'b1 on JTAG Test Mode Select (TMS) input (The TMS input causes state transitions in the Test Access Port controller) but instead it transitioned back to the instruction register. Three signals, P_SERR#, HS_ENUM# and HS_LED, were also left out of the boundary scan chain. This errata is fixed in the PCI2050B.

6.3 Master Discard Timer Errata

The PCI2050 asserts SERR#, if enabled, to the master after a target retries it for 2^{24} times. The Intel's 21150 not only asserts SERR# but will also issue a target abort on the originating bus. The PCI2050B is fixed to depict the latter behavior i.e., Target abort issued by the bridge immediately after the assertion of SERR#.

7 PCI2050B Enhancements

7.1 Posted Write Performance

Multiple back-to-back posted writes caused the PCI2050 to stop pipelining data if it took less time to initiate a transaction on one PCI interface than it took for the posted write processor to initiate on the other PCI interface. Hence PCI2050 stopped pipelining and used store and forward. The PCI2050B will not exhibit this behavior.

7.2 Target Disconnects the PCI2050

After a target disconnects PCI2050 before it has finished a posted write transaction, the PCI2050 samples two idle cycles before asserting FRAME# for the next transaction even though it has the GNT#. The PCI2050B will sample only one idle clock cycle before asserting FRAME#.

7.3 Bus Arbitration Logic Enhancement

There are two main arbitration enhancements. The first deals with requesting the bus when a second transaction is received and the second deals with requesting the bus for a transaction continuation when the latency timer has expired.

7.3.1 Second Pending Request in the FIFO

When a second transaction is received in the PCI2050B's FIFO, the primary or secondary bus arbitration logic should assert REQ# as soon as possible after receiving the transaction. This will help to eliminate delays caused by arbitration and allow the bridge to do Fast Back-to-Back memory write transactions. The PCI2050 bridge waits until the previous transaction is completed before asserting REQ#.

7.3.2 Latency Timer Expiration

When the latency timer expires and a write transaction has not completed, the PCI2050B will assert REQ# at the same time as it de-asserts FRAME# since the bridge should know at this point that it will not be able to transfer all of the pending data with the current transaction. The PCI2050 waits two clocks after finishing the first part of the burst before asserting REQ#.

7.4 FIFO Enhancement

Another enhancement that is implemented in the PCI2050B is Posted Write Combining. This feature is used to combine separate sequential memory write transactions into a single burst transaction. This feature can only be used if the address of the next memory write transaction is the next sequential address after the address of the last double word of the previous memory write transaction.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265