White Paper
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Solving CMOS Transition Rate Issues Using Schmitt Triggers

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This white paper focuses on understanding the importance of transition rate for CMOS (Complementary Metal Oxide Semiconductors) inputs for logic and translation devices. The implications of violating the transition rate along with the discussion of Schmitt trigger devices as a solution to overcome slow transition rate inputs are discussed.

Contents

1 What is Transition Rate and How is it Defined in a TI Data Sheet? 2
2 Negative Implications of Slow Transition Rates 3
3 Overcoming Slow Transition Issue 7
4 Conclusion 11
5 References 11

List of Figures

1 Supply Current as a Function of Input Voltage for AC and AHC Family 4
2 Parasitic lead Inductances associated with the package 4
3 Oscillations With Slow Inputs 5
4 Common Switching Input and Output Levels 5
5 Two-Stage Shift Register 6
6 Incorrect Operation of a Shift Register 6
7 RC Delay Circuit 7
8 Basic Schmitt Trigger Circuit 7
9 RC Circuit With Schmitt Trigger 8
10 Waveforms Without Schmitt Trigger- SN74AUP1G04 8
11 Waveforms Without Schmitt Trigger- SN74AUP1G04 8
12 Waveforms Without Schmitt Trigger- SN74LVC1G34 9
13 Start of Oscillation SN74AVC4T774 9
14 Lab Setup Comparison With Schmitt Trigger SN74AUP1G14 10
15 Lab Setup Comparison With Schmitt Trigger SN74AUP1G14 10
16 Lab Setup Comparison With Schmitt Trigger SN74LVC1G14 10

List of Tables

1 Typical Transition Rate by Logic Family 2
2 Required Minimum Input Rise/Fall Rates for Logic Families 3

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1 What is Transition Rate and How is it Defined in a TI Data Sheet?

Many parameters, such as V_{CC}, I_{CC}, leakage currents, and output drive strength, are typically the most important considerations for designers. However, considering and controlling input transition rate can be just as critical to the intended operation of a system. There is no formal definition offered by JEDEC on this, however, TI describes input transition rate as the rate of change of input voltage during a logic low-to-high or logic high-to-low transition. The transition time is specified in ns/V, which is the inverse of slew rate, defined as V/nS or V/uS. Furthermore, the maximum transition rate specified in the data sheet can be interpreted as the slowest acceptable rise time on logic inputs to ensure proper operation of the device.

Table 1 summarizes the input transition time based on TI logic families. For precise values of transition rate, see the *Recommended Operating Conditions* table of the data sheet for each device.

Table 1. Typical Transition Rate by Logic Family

				MIN	MAX	UNIT
Δt/Δv	Input transition rise or fall rate	ABT octals			5	ns/V
		ABT Widebus™ and Widebus+™			10	
		AHC, AHCT			20	
		FB			10	
		LVT, LVC, ALVC, ALVT			10	
		LV			100	
		TXS			10	
		TXB			30	
		LV-A	V_{CC} = 2.3 V to 2.7 V		200	
			V_{CC} = 3 V to 3.6 V		100	
			V_{CC} = 4.5 V to 5.5 V		20	
t_t	Input transition (rise and fall) time	HC, HCT	V_{CC} = 2 V		1000	ns
			V_{CC} = 4.5 V		500	
			V_{CC} = 6 V		400	

The input transition time for the HC, HCT is specified in ns and not in ns/V. To convert to ns/V , assume that the rise and fall times are measured from 10% to 90% and 90% to 10% respectively, of the full scale amplitude i.e V_{CC}. The conversion from the rise time or fall time into transition rate represented in ns/V can be calculated by following Equation 1:

$$dt/dv = t_{RF}/(0.9 \times V_{cc}) - (0.1 \times V_{CC}) \quad (1)$$

where

- t_{RF} can be either the rise time or fall time

For example, using the HC device from Table 1, for V_{CC} of 6 V, calculate the transition rate as:

$$dt/dv = 400ns/[(0.9 \times 6) - (0.1 \times 6)] \quad (2)$$

This comes to about 83 ns/V which is listed in Table 2 as 80 ns/V.

Common issues associated with transition rate violations are discussed in the following sections.

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2 Negative Implications of Slow Transition Rates

2.1 Surge current and Power Consumption

A typical CMOS (Complementary Metal Oxide Semiconductor) inverter has a PMOS (P-Channel Metal Oxide Semiconductor) and NMOS (N-Channel Metal Oxide Semiconductor) stage connected with a common drain output. The PMOS conducts when a static low is applied to the gate and the NMOS conducts when a static high is applied to the gate. During steady-state operation, there is no path for the current to flow from the V_{CC} to ground which is the reason CMOS devices are highly power conservative.

During a transition from a high to low or low to high state, the transistors will conduct momentarily from V_{CC} to ground. Table 2 shows the logic families for various V_{CC}, along with V_T (threshold voltage) and transition time.

V_{IL} is the maximum voltage below which input is considered as low.

V_{IH} is the minimum voltage above which an input is considered as logic high.

V_T is the threshold of the device where the output switches state when there is a change in input. The threshold voltage V_T is centered around V_{IH} and V_{IL} voltage.

Table 2. Required Minimum Input Rise/Fall Rates for Logic Families

SERIES	V_{CC} (V)	$V_{IL(max)}$ (V)	$V_{IH(min)}$ (V)	V_T (V)	dt/dv (ns/V)
SN74	4.75-5.25	0.8	2	1.4	15
SN74LS	4.75-5.25	0.8	2	1.4	15
SN74S	4.75-5.25	0.8	2	1.4	15
SN74ALS	4.5-5.5	0.8	2	1.4	15
SN74AS	4.5-5.5	0.8	2	1.4	15
SN74F	4.5-5.5	0.8	2	1.4	15
SN74HC	2	0.3	1.5	1.4	625
	4.5	0.9	3.15	2.25	110
	6	1.2	4.2	3	80
SN74HCT	4.5-5.5	0.8	2	1.4	125
74AC	3	0.9	2.1	1.5	10
	4.5	1.35	3.15	2.25	10
	5.5	1.65	3.85	2.75	10
74ACT	4.5-5.5	0.8	2	1.4	10
SN74BCT	4.5-5.5	0.8	2	1.4	10
SN74ABT	4.5-5.5	0.8	2	1.4	5/10
SN74LV	2.7-3.6	0.8	2	91.5	100
SN74LVC	2.7-3.6	0.8	2	91.5	5/10
SN74LVT	3.0-3.6	0.8	2	1.4	10

When an input is between V_{IL} and V_{IH} and close to V_T, both of the transistors are conducting partially. If the input transition is from high to low, the NMOS is conducting and trying to turn off while the PMOS is trying to turn on; likewise when input transition is from low to high, the PMOS is trying to turn off while the NMOS is trying to turn on. Slower input signal transitions cause the device to remain in this conductive state for a longer period of time, increasing current flow and thereby power consumption. This momentary increase in current during the transition is termed *surge current* or *shoot-through current* and is not a static or quiescent behavior but dynamic behavior of the device. The higher the number of inputs and outputs switching simultaneously, the higher the current consumption is and greater the potential to damage the device due to surge current. Figure 1 shows comparison of typical surge currents for SN74AHC and SN74AC family of devices. The current consumption for the AC family of devices is higher than AHC. Usually, given similar transistor technologies, the higher the speed, the higher is the current consumption. See *CMOS power calculation and Cpd Calculation* to learn more on static and dynamic power calculation.

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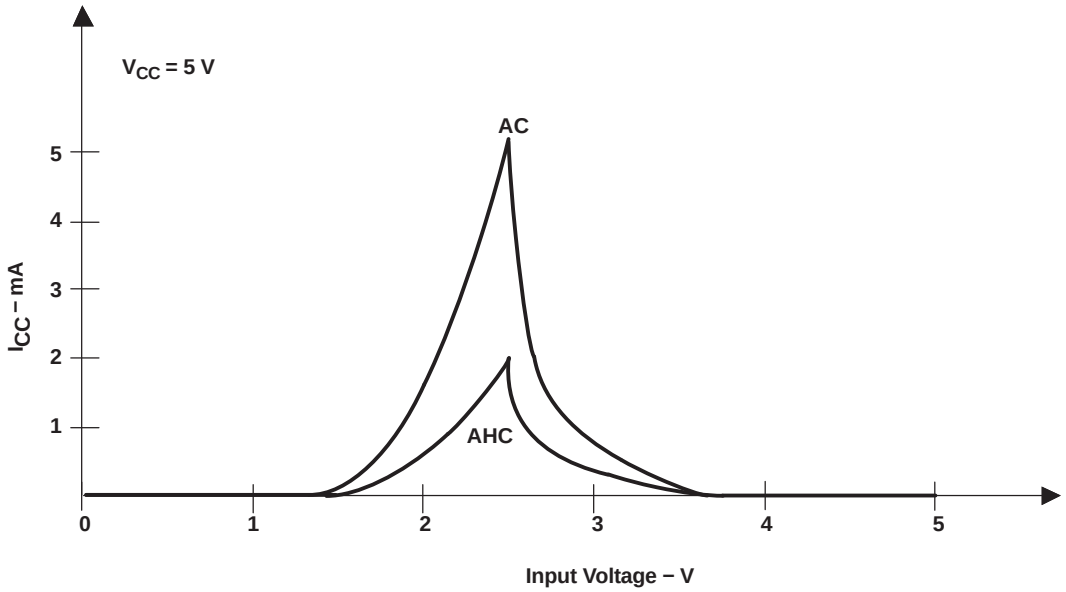

Figure 1. Supply Current as a Function of Input Voltage for AC and AHC Family

2.2 Unwanted Oscillations

The Integrated circuit device comes in different packages with the die at the center and internal bond wires connecting the die pad with the external leads. The leads are connected to other devices through PCB traces which contributes to the parasitic capacitance at the output, while the leads contribute to the parasitic inductances as shown in Figure 2.

During normal operation, the input switches from high to low or low to high and after a certain propagation delay t_{PD}, the output changes from low to high or high to low respectively. However, when there is a slow changing input (from low to high), the output changes from high to low at the threshold voltage V_T and along with it discharges the output load capacitance. There is a voltage drop at the parasitic package inductance at the ground due to the discharge current (see *surge current*) which raises the internal ground potential of the integrated circuit. The voltage difference between the input and the internal ground potential decreases, essentially giving an impression of a decreased input voltage below the threshold voltage. The circuit immediately changes the state from low to high. There is a similar effect of supply droop when input switches from high to low causing the output to switch from low to high which charges the external capacitance. This process repeats continuously until the input is sufficiently high enough to overcome the ground shift and cross the V_{IH} or low enough to cross the V_{IL} of the device. This phenomenon is termed as ground bounce. The oscillations can be higher or it could start at lower transition rates when multiple inputs and outputs are switching as compared to a single channel switching. This may be seen typically with multi channel buffers and transceivers. This oscillation is harmful to the device as well as for the whole system potentially creating multiple triggering events as shown in Figure 3.

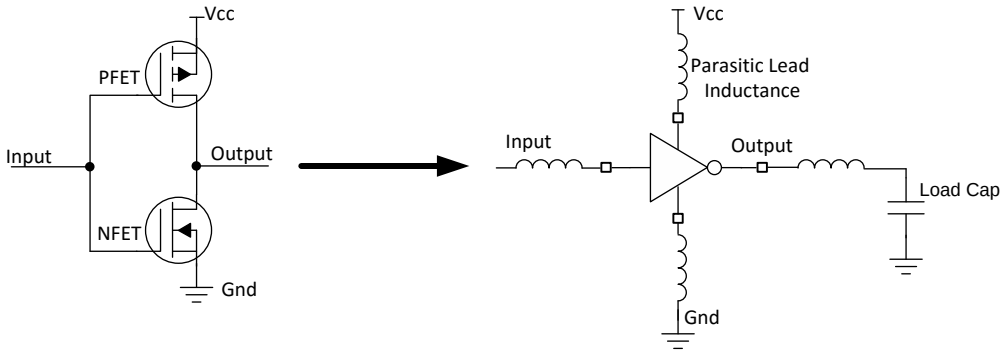

Figure 2. Parasitic lead Inductances associated with the package

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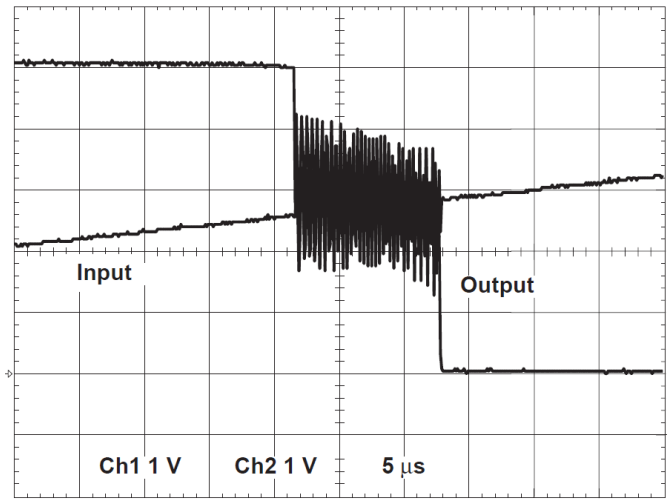

Figure 3. Oscillations With Slow Inputs

2.3 False triggering

Figure 4 shows the transition rate along with the threshold voltage V_T, V_{IL}, and V_{IH} information for common voltage node levels.

The V_{IL} is the maximum voltage below which the input is considered low.

The V_{IH} is the minimum voltage above which the input is considered to be high.

The V_T is the level at which the output changes state from high to low or low to high and it is midway between V_{CC} and ground for CMOS process and is about 1.5 V for TTL input compatible devices.

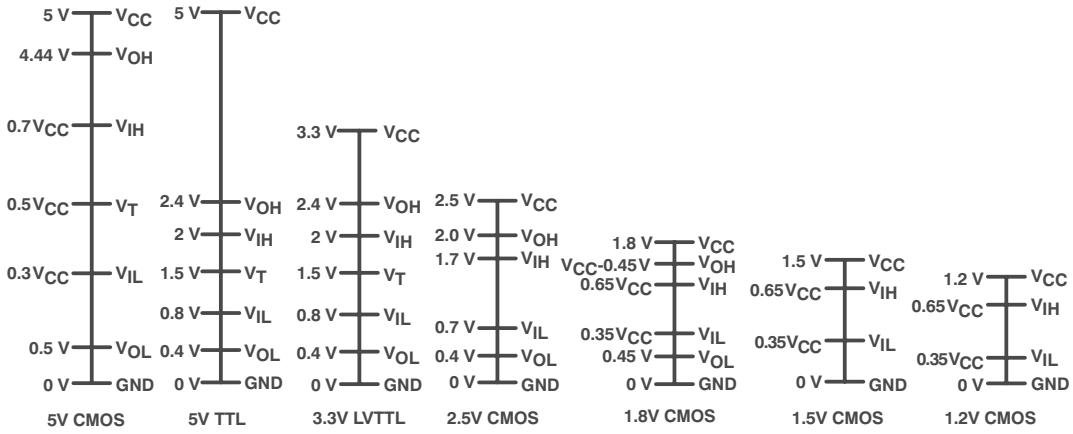

Figure 4. Common Switching Input and Output Levels

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Consider the interconnected devices in a system as shown in Figure 5, each with two different threshold voltages. The first device is considered to have a lower threshold voltage at 1.5-V (5-V-TTL compatible) and the second device is considered to have a higher threshold voltage than the first being a 5-V-CMOS device.

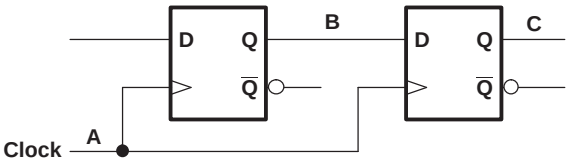

Figure 5. Two-Stage Shift Register

The normal operation of the shift register is when the clock signal clocks in the state at the D input and after the typical propagation delay t_{PD}, appears at the output Q denoted as B. The same output is the input to the second D flip flop which at the second rising edge of the clock signal shifts the data out (C) while at the same instant the second bit of data is passed out from the first D flip flop for the same clock signal. The cycle continues under normal operation as the shift register.

Now, consider the abnormal operation when there is a slow rising edge clock input as shown in Figure 6. As the clock input reaches the threshold voltage at 1.5 V, the first D flip flop goes high after the typical propagation delay and presents at the input of the second D flip flop. Meanwhile, the clock is still rising slowly with a rise time greater than the propagation delay of the first stage, it reaches the threshold level of the second shift register. The second shift register output goes high after the typical propagation delay at the same clock edge resulting in incorrect intended operation.

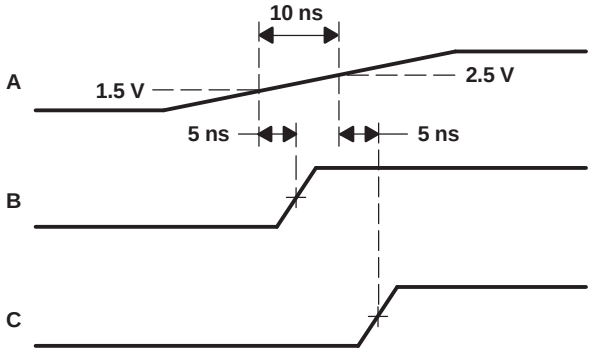

Figure 6. Incorrect Operation of a Shift Register

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3 Overcoming Slow Transition Issue

3.1 Schmitt-Trigger Inputs

The issues of slow rising input signals are so significant on the performance of the device, and ultimately to the system operation , a solution to mitigate these issues is required. The first and foremost is to prevent slow input signals generated unintentionally. Most often, they are unavoidable when there are long trace lengths due to the board parasitic, so appropriate layout considerations can avoid this to some extent.

Some of the application might require a delay introduced intentionally using RC circuit as shown in Figure 7, usually for control or enable signals during power-up sequence.

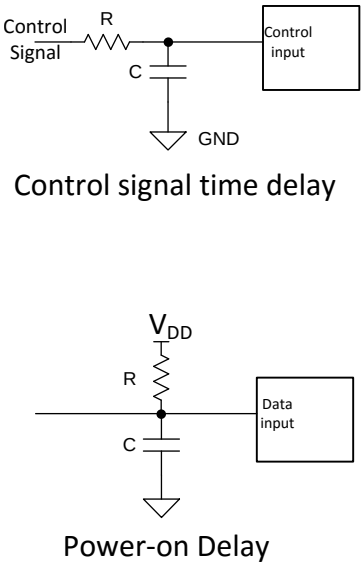

Figure 7. RC Delay Circuit

Schmitt trigger devices are best used after the RC circuit to provide a clean input into the control signal after the delay. The Schmitt trigger device has dual threshold for rising and falling edges. The Vt+ is the positive threshold and Vt– is the negative going threshold. The hysteresis is defined as the difference between the positive and negative threshold. The output is guaranteed to not switch for any value in between the positive and negative threshold. The basic configuration of the schmitt trigger circuit is as shown in Figure 8. For more information on Schmitt trigger, see *Understanding Schmitt triggers*.

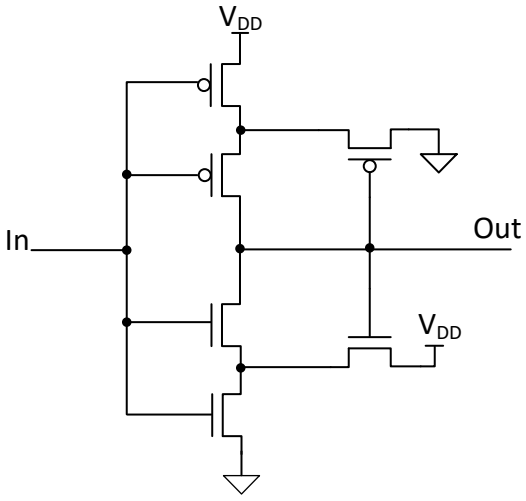

Figure 8. Basic Schmitt Trigger Circuit

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Schmitt trigger devices are ideal for converting slow edge rate inputs into fast edge rates outputs. They are ideal to also have a clean square wave output in noisy environments. As shown in Figure 9, the control signal has large time constant caused by the RC network. The control signal thus generated directly interfacing into a CMOS device can cause issues as described in the above sections. It is suggested to use a schmitt trigger buffer before the signal interfaces with the device. The schmitt trigger buffer produces a sharp rising edge square wave and includes the required delay of the RC time constant.

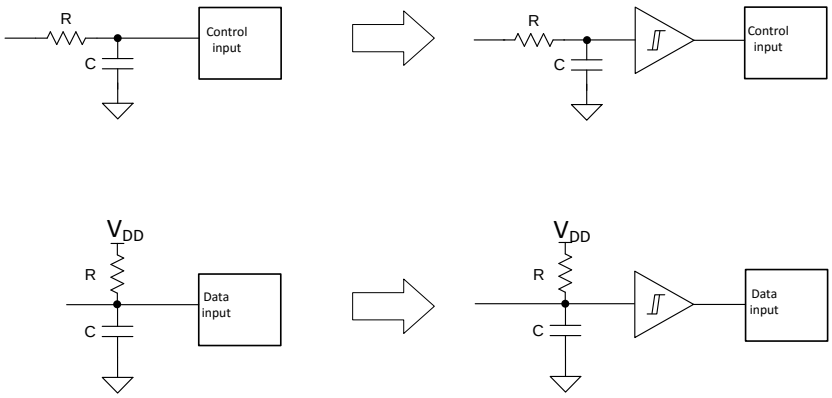

Figure 9. RC Circuit With Schmitt Trigger

The lab data collected on the SN74AUP1G04 and SN74LVC1G34 without schmitt trigger has oscillations with rise time set to 1 µs, see Figure 10 and Figure 12.

The Bipolar devices do not have transition rate specified in the data sheet indicating their greater tolerance for slower signals, however, the power consumption under normal operation for the BJT devices offsets the advantages.

Figure 10. Waveforms Without Schmitt Trigger- SN74AUP1G04

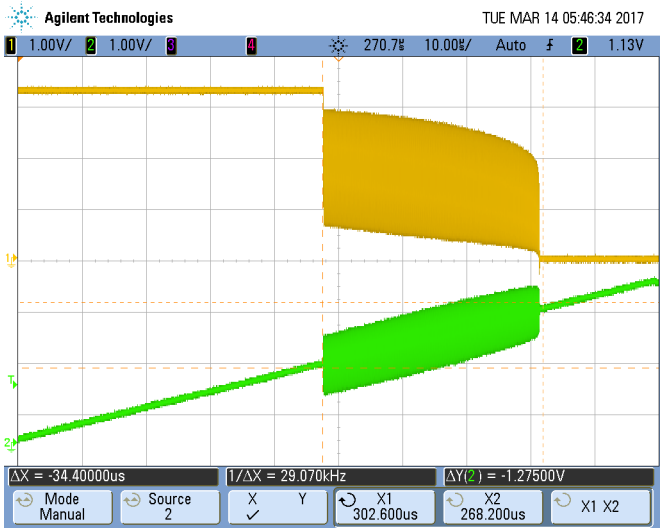

Figure 11. Waveforms Without Schmitt Trigger- SN74AUP1G04

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Figure 12. Waveforms Without Schmitt Trigger- SN74LVC1G34

Figure 13 shows the oscillations start at rise time as low as 38 ns on the SN74AVC4T774 device with 4 channels switching simultaneously. This roughly translates to transition rate as low as 25 ns/V.

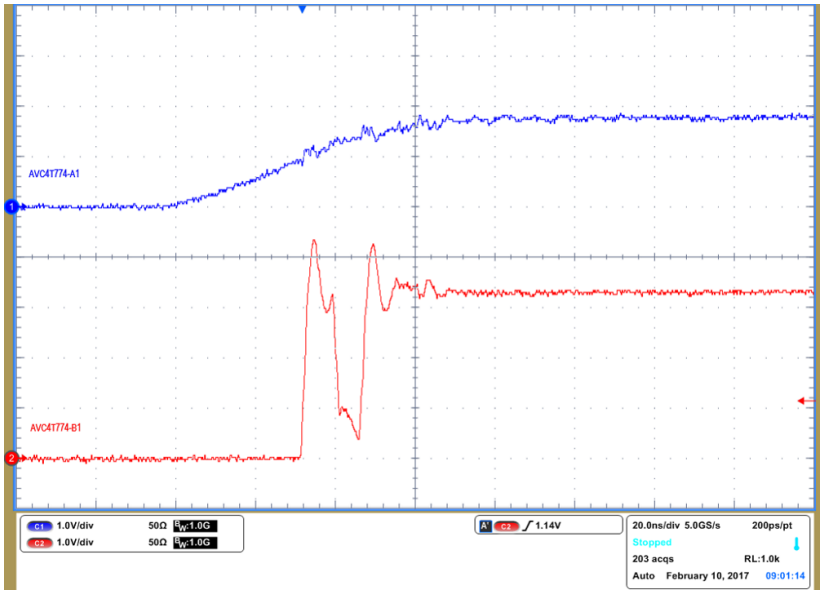

Figure 13. Start of Oscillation SN74AVC4T774

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The schmitt trigger inverter SN74AUP1G14 with the same rise time of 1 µs results in square wave as seen in Figure 14. Similarly, the schmitt trigger buffer SN74LVC1G14 results in a clean square wave, see Figure 16. The surge current involved with the slow signal is also associated even while using the schmitt trigger device. Although, the schmitt trigger is designed to handle slow signals, take care to not exceed the absolute maximum junction temperature through the surge current thus produced.

Figure 14. Lab Setup Comparison With Schmitt Trigger SN74AUP1G14

Figure 15. Lab Setup Comparison With Schmitt Trigger SN74AUP1G14

Figure 16. Lab Setup Comparison With Schmitt Trigger SN74LVC1G14

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4 Conclusion

The input transition rate for CMOS devices has been discussed. Additionally, implications of violating the transition rate specification, such as oscillations and false triggering, have been addressed. Devices with schmitt trigger inputs have been highlighted as a potential solution for ensuring slow input signals do not affect the system operation, and results of bench testing are provided to prove this benefit.

5 References

Slow and Floating CMOS Inputs

Bus Hold Circuits

Designing With Logic

Understanding and Interpreting TI Data Sheets

Understanding Schmitt Trigger

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2017) to A Revision	Page
• Deleted hanging transistor from figure: *Basic Schmitt Trigger Circuit*	7

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