Application Report
SLLA415–December 2018

TUSB1044 Configuration Guidelines

Undrea Fields

ABSTRACT

The TUSB1044 is a Type-C Alt Mode redriver supporting USB 3.2 Gen2 data rates up to 10 Gbps and DisplayPort 1.4 up to 8.1 Gbps over a USB Type-C interface. At these higher data rates, signal integrity issues place limitations on system trace length. The TUSB1044 provides several levels of receive linear equalization to compensate for cable and board loss due to inter-symbol interference (ISI). This document is intended to provide general guidelines on how to use the TUSB1044 in a source application. The information in this document can also be applied to the TUSB544.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The TUSB1044 is a Type-C bi-directional linear redriver which can be used in both source and sink applications to compensate for channel loss created by PCB trace and cable ISI. This channel loss can cause compliance failures when a receiver cannot recover channel data as the eye height and width may have been severely affected. The TUSB1044 provides equalization gain to compensate for the board trace and cable loss.

(1)

2 Equalization Selection

The TUSB1044 enables the system to pass both USB and DP 1.4 transmitter electrical compliance and receiver jitter tolerance compliance testing for USB3.2 Gen1/2 and DisplayPort 1.4. The TUSB1044 recovers incoming data by applying equalization that compensates for the channel loss. The equalization should be set based on the amount of insertion loss of the channel before the TUSB1044 receiver (Pre-Channel). The EQ value of each channel should be set independently based on the loss of the channel, the equalization selection is performed by configuring theDEQ[1:0] and UEQ[1:0] pins, or through programming the equivalent registers if the device is configured for I2C operation. The equalization values are detailed in Table 1. Typical FR4 trace losses are given in Table 2.

Table 1. TUSB1044 Equalization

	Downstream Facing Port using 100mV Linearity Setting				Upstream Facing Port using 100mV Linearity Setting			
EQ Setting#	DEQ1 Pin Level	DEQ0 Pin Level	EQ Gain 5 GHz (dB)	EQ Gain 4.05 GHz (dB)	UEQ1 Pin Level	UEQ0 Pin Level	EQ Gain 5 GHz (dB)	EQ Gain 4.05 GHz (dB)
0	0	0	-2.1	-1.4	0	0	-4.4	-3.3
1	0	R	0	0.4	0	R	-2.2	-1.5
2	0	F	1.5	1.7	0	F	0.7	0.0
3	0	1	3.0	3.2	0	1	0.9	1.4
4	R	0	4.0	4.1	R	0	1.9	2.4
5	R	R	5.0	5.2	R	R	3.0	3.5
6	R	F	5.9	6.1	R	F	3.8	4.3
7	R	1	6.7	6.9	R	1	4.7	5.2
8	F	0	7.4	7.7	F	0	5.4	6.0
9	F	R	8.0	8.3	F	R	6.0	6.6
10	F	F	8.5	8.5	F	F	6.5	7.2
11	F	1	9.0	9.4	F	1	7.1	7.7
12	1	0	9.4	9.8	1	0	7.5	8.1
13	1	R	9.8	10.3	1	R	7.9	8.6
14	1	F	10.1	10.6	1	F	8.3	9.0
15	1	1	10.5	11.0	1	1	8.6	9.4

Table 2. Example FR4 Trace Loss

4-mil Wide FR4 PCB Trace Length (Inches)	Loss at 2.5 GHz (dB)	Loss at 4.05 GHz (dB)	Loss at 5 GHz (dB)
1	0.5	0.7	0.9
2	1	1.5	1.7
3	1.5	2.2	2.6
4	2	2.9	3.5
5	2.5	3.7	4.3
6	2.9	4.4	5.2
7	3.4	5.1	6.1
8	3.9	5.9	7
9	4.4	6.6	7.8
10	4.9	7.3	8.7

3 VOD Linearity Range and DC Gain

The CFG0 and CFG1 pins can be used to adjust the TUSB1044 differential output voltage (VOD) swing linear range and receiver equalization DC gain for both downstream an upstream data path directions. Table 2 details the options available.

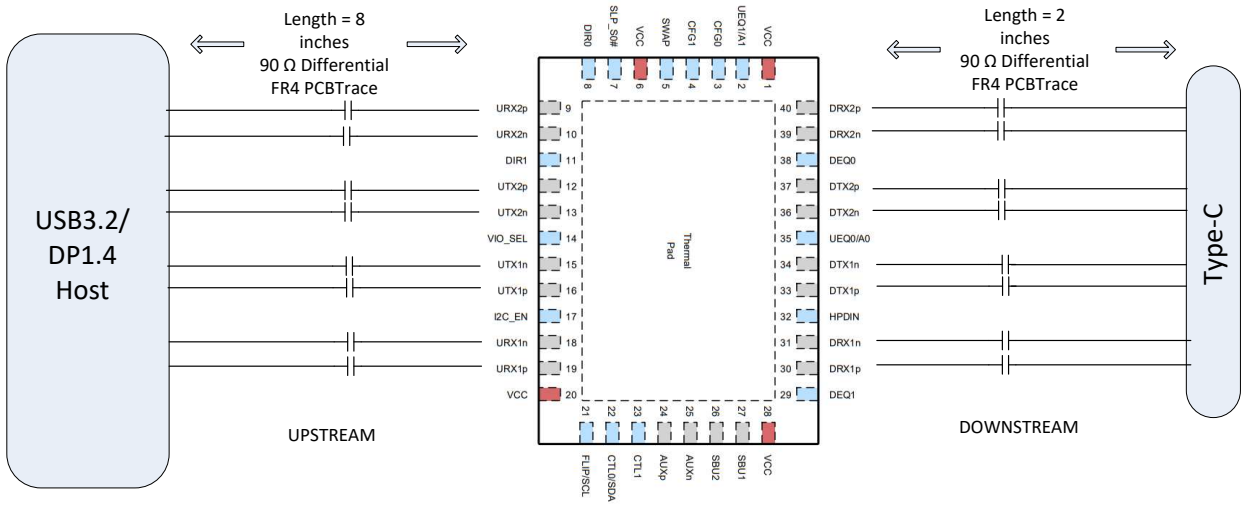
Table 3. VOD Linear Range and DC Gain

Setting#	CFG1 Pin Level	CFG0 Pin Level	Downstream DC Gain (dB)	Upstream DC Gain (dB)	Downstream VOD (mVpp)	Upstream VOD (mVpp)
0	0	0	1	0	900	900
1	0	R	0	1	900	900
2	0	F	0	0	900	900
3	0	1	1	1	900	900
4	R	0	0	0	1100	1100
5	R	R	1	0	1100	1100
6	R	F	0	1	1100	1100
7	R	1	2	2	1100	1100
8	F	0	Reserved	Reserved	Reserved	Reserved
9	F	R	Reserved	Reserved	Reserved	Reserved
10	F	F	0	0	1300	1300
11	F	1	Reserved	Reserved	Reserved	Reserved
12	1	0	Reserved	Reserved	Reserved	Reserved
13	1	R	Reserved	Reserved	Reserved	Reserved
14	1	F	Reserved	Reserved	Reserved	Reserved
15	1	1	Reserved	Reserved	Reserved	Reserved

4 Configuration Example

Figure 1 provides an example configuration of a host system using a USB3.1 Gen2 Host operating at 10 Gbps.

Figure 1. System Trace Length Example



Using the given trace lengths and data rate in this example, the method to select the equalization values for Upstream and Downtream EQ is to select the closest EQ gain value available to match the trace loss as follows.

- Host to TUSB1044 (Upstream) = 8 inches (7 dB loss at 5GHz). UEQ Setting #11 (7.1 dB).
- TUSB1044 to Type-C Connector (Downstream) = 2 inches (1.7 dB loss at 5 GHz). DEQ Setting #3 (3 dB).

Other factors such as layout quality and Host/Source/Sink driver and receiver quality may require the equalization settings to be adjusted higher or lower for best performance. The above method should be used for selecting initial configuration settings based on system board trace lengths.

5 Layout Guidelines

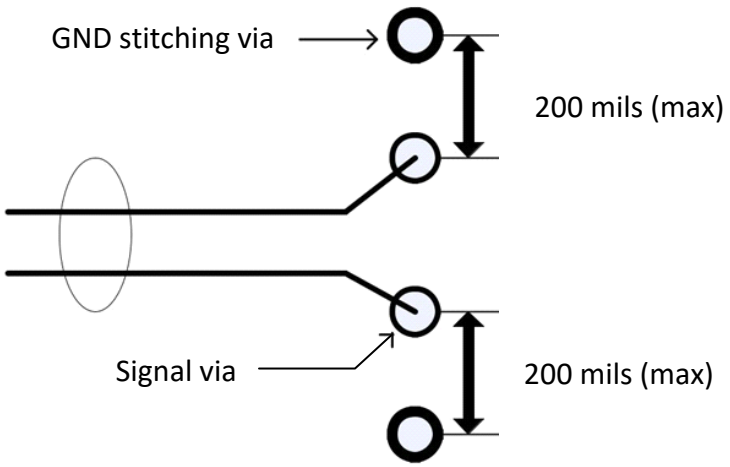
The following layout guidelines should be used in routing the high-speed USB and DisplayPort signals to and from the TUSB1064.

- RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (+/- 15%).
- Keep differential pairs away from other high-speed signals.
- Intra-pair routing should be kept to within 2 mils.
- DisplayPort lane inter-pair routing should be kept to within 50 mils.
- Differential pair length matching should be near the location of mismatch.
- Each pair should be seperated by at least 3x the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135º. This will minimize any length mismatch caused by the bends and minimize the impact bends have on EMI.
- Route all differential pairs on the same layer.
- Minimize the number of vias, it is recommended to keep the via count to 2 or less.
- Keep differential traces on layers adjacent to a ground plane.
- Do not route differential pairs over any split plane.
- If using a through-hole connector, route the high-speed signals on opposite side of the connector such that the connector pin does not create a stub in the transmission line.

6 GND Stitching

The entirety of any high-speed signal trace should maintain the same GND reference plane from origination to termination. If the same GND reference plane is not maintained, via-stitch both GND planes together to ensure continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200 mils (Center-to-center, closer is better) of the signal transition vias. See Figure 2 for an example of GND stitching vias.

Figure 2. GND Stitching Vias Example



7 AC-Coupling Capacitors

When placing AC-Coupling capacitors, the maximum component size used should be 0402. During layout, the AC-Coupling capacitors should be placed close to the transmitter pins of the device with symmetrical placement to ensure optimum signal quality and to minimize reflections. See Figure 3 for AC-Coupling capacitor placement and Figure 4 for AC-coupling capacitor layout symmetry.

Figure 3. AC-Coupling Capacitor Placement

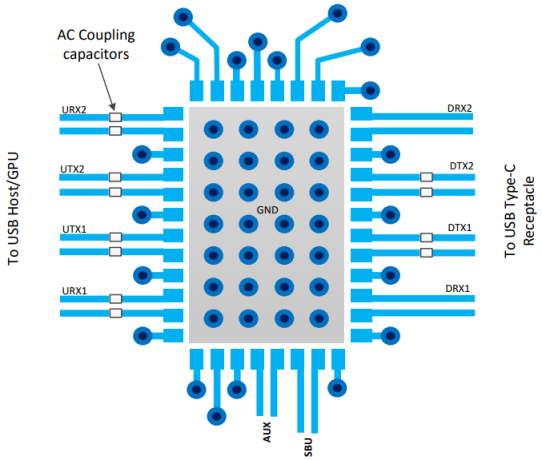
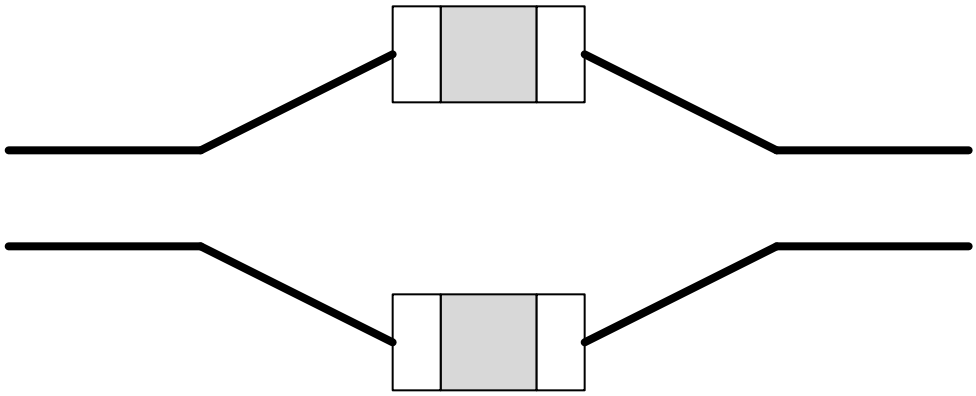


Figure 4. AC-Coupling Capacitor Layout Symmetry Example



NOTE: Adding test points to the high-speed traces can cause impedance discontinuity which negatively impacts signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the transmission line.

8 References

- Datasheet: TUSB1044 USB Type-C™ 10Gbps Multi-Protocol Bi-Directional Linear Redriver
- Datasheet: TUSB544 USB Type-C™ 8.1Gbps Multi-Protocol Linear Redriver
- VESA DisplayPort Alt Mode on USB Type-C Standard, Version 1.0a, August 5, 2015

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265