TUSB73x0 Board Design and Layout Guidelines

User's Guide

Literature Number: SLLU149E
June 2011–Revised February 2016

Contents

List of Figures

List of Tables

TUSB73x0 Board Design and Layout Guidelines

These guidelines are intended to provide developers with the resources needed to properly layout the TUSB7320/TUSB7340. They are intended as a follow-on document to the USB 2.0 Board Design and Layout Guidelines (SPRAAR7) which describes general PCB design and layout guidelines for the USB 2.0 differential pair (DP/DM). A layout for the TUSB7340 will seamlessly accommodate the TUSB7320.

This document is focused on the layout and routing of the USB 3.0 SuperSpeed USB and PCI Express. It is intended for developers familiar with high-speed PCB design and layout. Knowledge of the USB 3.0 and PCI Express specifications and protocols are required as well.

Trademarks

Related Documentation

TI Customer DEMO EVM Reference Schematic and Layout files

PCB Design and Layout Guidelines for the USB 2.0 Differential Pair (SPRAAR7)

PCI Express Card Electromechanical 2.0 Specification:
http://www.pcisig.com/specifications/pciexpress/base2

USB 3.0 Specification: http://www.usb.org/developers/docs

PCI Express Base Specification 2.1: http://www.pcisig.com/specifications/pciexpress

Typical System Implementation

1.1 Overview

The TUSB73x0 is an xHCI SuperSpeed USB host controller that interfaces to the PC host system via a PCIe x1 Gen 2 or PCIe Gen 1 interface, providing SuperSpeed, High-speed, Full-speed, or Low-speed connections on the downstream USB ports. The TUSB7340 supports up to four downstream ports, and the TUSB7320 supports up to two downstream ports.

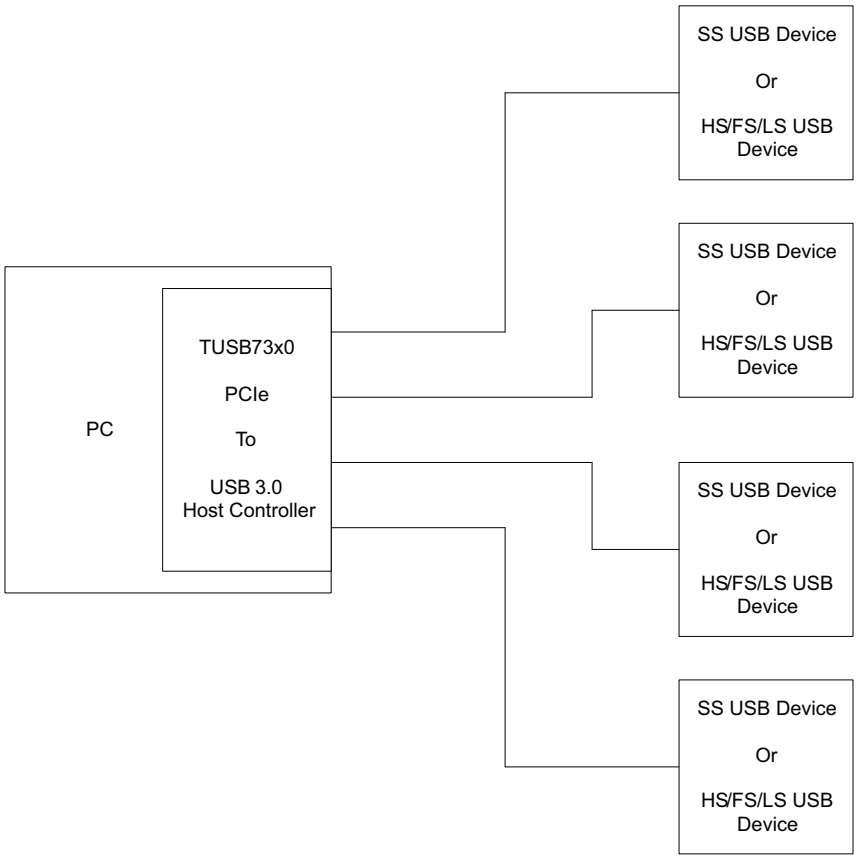


Figure 1-1. Typical Application

2.1 Overview

See Achieving_Lowest_Power_with_TUSB73X0.pdf for more information on the settings used to get these low power numbers.

TUSB7320 Power Consumption ASPM=1/P3_ENABLE=1					
	VCore		V I/O		
	1.05		3.3		
	mA	mW	mA	mW	Total mW
2 SuperSpeed Devices Connected (ACTIVE)	507.00	532.35	112.00	369.60	901.95
2 SuperSpeed Devices Connected (IDLE)	445.00	467.25	112.00	369.60	836.85
1 SuperSpeed Device Connected (ACTIVE)	392.00	411.60	112.00	369.60	781.20
1 SuperSpeed Device Connected (IDLE)	331.00	347.55	112.00	369.60	717.15
PCI D0 - No Device Connected (IDLE)	156.00	163.80	40.00	132.00	295.80
PCI D3 - No Device Connected	56.00	58.80	3.50	11.55	70.35
Hibernate (ACPI S5) - No Device Connected	56.00	58.80	3.50	11.55	70.35

Figure 2-1. TUSB7320 Power Consumption

TUSB7340 Power Consumption ASPM=1/P3_ENABLE=1					
	VCore		V I/O		
	1.05		3.3		
	mA	mW	mA	mW	Total mW
4 SuperSpeed Devices Connected (ACTIVE)	880	924.00	115	379.50	1303.50
4 SuperSpeed Devices Connected (IDLE)	790	829.50	115	379.50	1209.00
3 SuperSpeed Devices Connected (ACTIVE)	740	777.00	115	379.50	1156.50
3 SuperSpeed Devices Connected (IDLE)	658	690.90	115	379.50	1070.40
2 SuperSpeed Devices Connected (ACTIVE)	597	626.85	115	379.50	1006.35
2 SuperSpeed Devices Connected (IDLE)	518	543.90	115	379.50	923.40
1 SuperSpeed Device Connected (ACTIVE)	420	441.00	115	379.50	820.50
1 SuperSpeed Device Connected (IDLE)	376	394.80	115	379.50	774.30
PCI D0 - No Device Connected (IDLE)	168	176.40	42	138.60	315.00
PCI D3 - No Device Connected	63	66.15	4	13.20	79.35
Hibernate (ACPI S5) - No Device Connected	63	66.15	4	13.20	79.35

Figure 2-2. TUSB7340 Power Consumption

2.2 Digital Supplies

Both VDD1P1 and VDD3P3 supplies must have 0.1-µF bypass capacitors to VSS (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep the traces as short and wide as possible to the vias that are used to connect to the power planes. Smaller value capacitors like 0.01 µF are also recommended on the digital supply terminals.

When placing and connecting all bypass capacitors, high-speed board design rules must be followed.

2.3 Analog Supplies

Since circuit noise on the analog power terminals must be minimized, an appropriate LC type filter is recommended for each supply. For EMI concerns, appropriate ferrite beads should be used instead of inductors in the LC filter circuit.

Analog power terminals should have a 0.1-µF bypass capacitor connected to VSS (ground) in order for proper operation. Place the capacitor as close as possible to the terminal on the device and keep the traces as short and wide as possible to the vias that are used to connect to the power planes. Smaller value capacitors like 0.01 µF are also recommended on the analog supply terminals.

Analog power terminals should have a 0.1-µF bypass capacitor connected to VSS (ground) in order for proper operation. Place the capacitor as close as possible to the terminal on the device and keep the traces as short and wide as possible to the vias that are used to connect to the power planes. Smaller value capacitors like 0.01 µF are also recommended on the analog supply terminals.

2.4 Ground Terminal

The thermal pad is also the board ground connection. Care should be taken to make sure any traces or vias under the device are far enough away from the thermal pad to prevent shorts. As shown in Figure 2-3, it is recommended to have at least 16 vias connecting the thermal pad to the board ground plane.

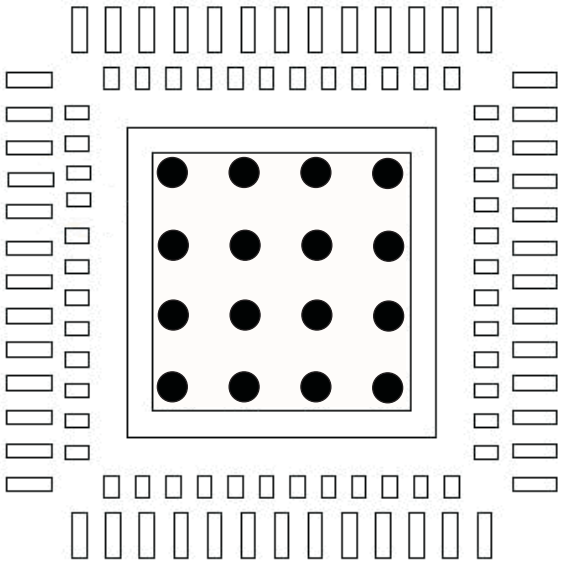


Figure 2-3. Board Ground Connection

2.5 Capacitor Selection Recommendations

When selecting bypass capacitors, X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and cost of these capacitors make them a logical choice for most computer systems.

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell “D” size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. Both of these bulk capacitor options significantly reduce low-frequency power supply noise and ripple.

2.6 USB VBUS

The TPS2560 is a dual channel power distribution switch that can handle high capacitive loads and short circuit conditions. The output current for each channel can be adjusted up to 2.8 A, making it ideal for SS USB ports.

Each channel can be seamlessly and independently controlled by the TUSB73x0. The TPS2560 also provides a seamless, per port fault indication. Refer to the datasheet for more information regarding this device.

More information can be found at: http://focus.ti.com/docs/prod/folders/print/tps2560.html

Device Reset

3.1 Overview

There is no GRST# timing constraint with respect to the power supplies, other than it should not be deasserted until the power supplies are stable.

However, extreme care must be taken if a passive reset is used, such as using the internal GRST# pull up or an external RC circuit, to ensure that the GRST# does not deassert until the 3.3-V and 1.1-V rails are within 10% of nominal. If the 3.3-V power ramps before the 1.1-V supply, and GRST# is deasserted, the device I/O is in an undefined state before the core logic is active. This allows the potential for the GRST# I/O cell to incorrectly configure as an output and drive the GRST# signal high until the core logic is powered on and correctly configures the cell.

It is highly recommended that the GRST# input be connected to a power good output from a power supply to ensure that it does not deassert until both the 3.3-V and 1.1-V power rails are within 10% of their nominal value. The recommended sequence is to have the 3.3-V feed a 1.1-V regulator and then use the 1.1-V Power Good signal to drive GRST# as outlined below.

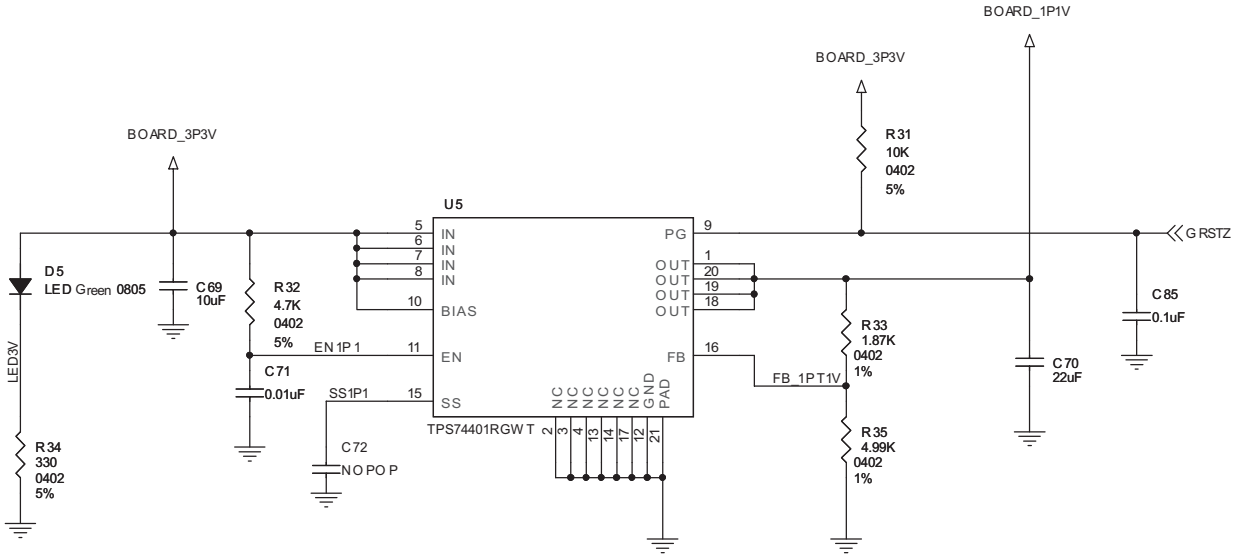


Figure 3-1. 1.1-V Regulator

General High Speed Layout Guidelines

4.1 Printed Circuit Board Stackup (FR-4 Example)

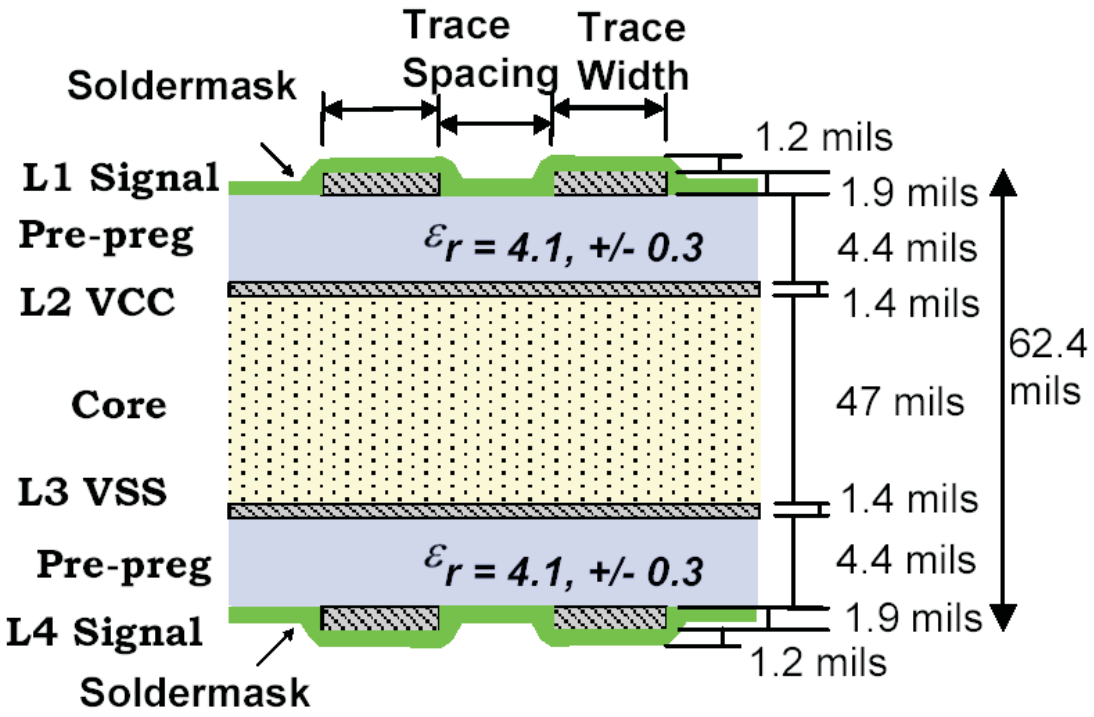


Figure 4-1. Nominal 4-Layer PCB Stackup

PCB layer configuration suggestions for stackup symmetry and signal integrity.

4 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(PWR)
Layer 4	(Bottom)

6 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(Signal)
Layer 4	(Signal)
Layer 5	(PWR)
Layer 6	(Bottom)

10 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(Signal)
Layer 4	(Signal)
Layer 5	(PWR)
Layer 6	(GND)
Layer 7	(Signal)
Layer 8	(Signal)
Layer 9	(GND)
Layer 10	(Bottom)

Figure 4-2. PCB Layer Configuration Suggestions

4.2 Return Current and Plane References

High frequency return signal/current is defined as the path that a signal follows back to its original source as all signals flow in a closed loop. Minimizing the loop area of the closed loop is beneficial for both EMI (Electro-Magnetic Interference) reduction and signal integrity.

The best way to minimize loop area is to always have a signal reference their nearest solid ground or power plane. Obstructions to the return signal will cause signal integrity problems like reflections, crosstalk, undershoot and overshoot.

Signals can reference either power or ground planes, but ground is preferred. Without solid plane references, single ended and differential impedance control is very hard to accomplish; crosstalk to other signals may happen as the return signals will have no other path. This type of crosstalk is difficult to troubleshoot.

Symmetric pairing of solid planes in the layer stackup can significantly reduce warping of the PCB during the manufacturing process. Warping of the PCB is crucial to minimize on boards that utilize BGA components.

4.3 Split Planes – What to Avoid

Never route signals over splits in their perspective reference planes.

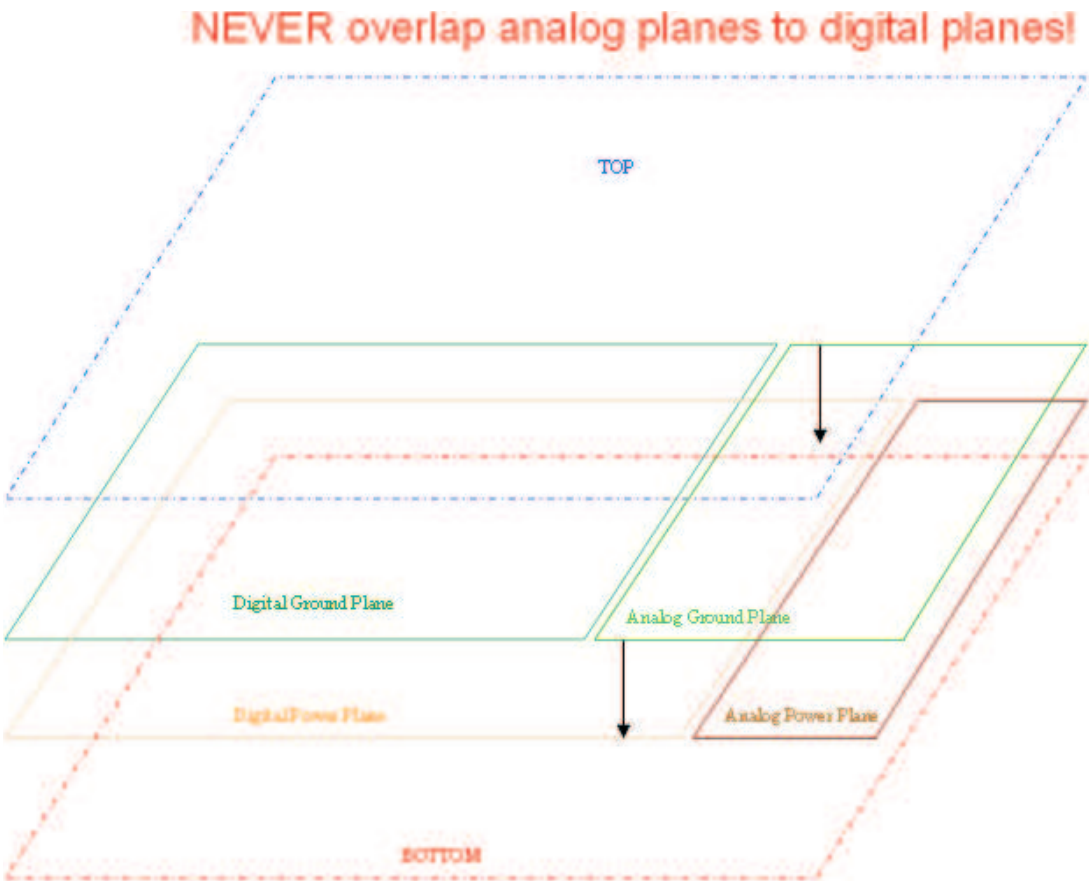


Figure 4-3. Overlapping Analog and Digital Planes

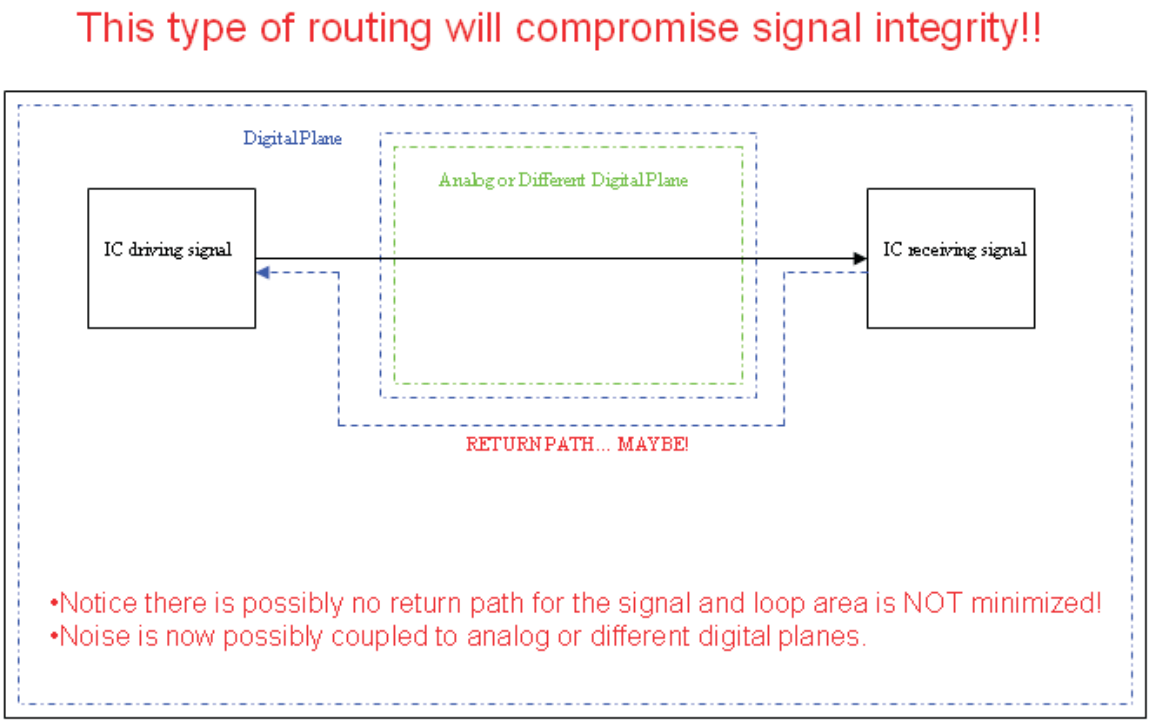


Figure 4-4. Incorrect Routing

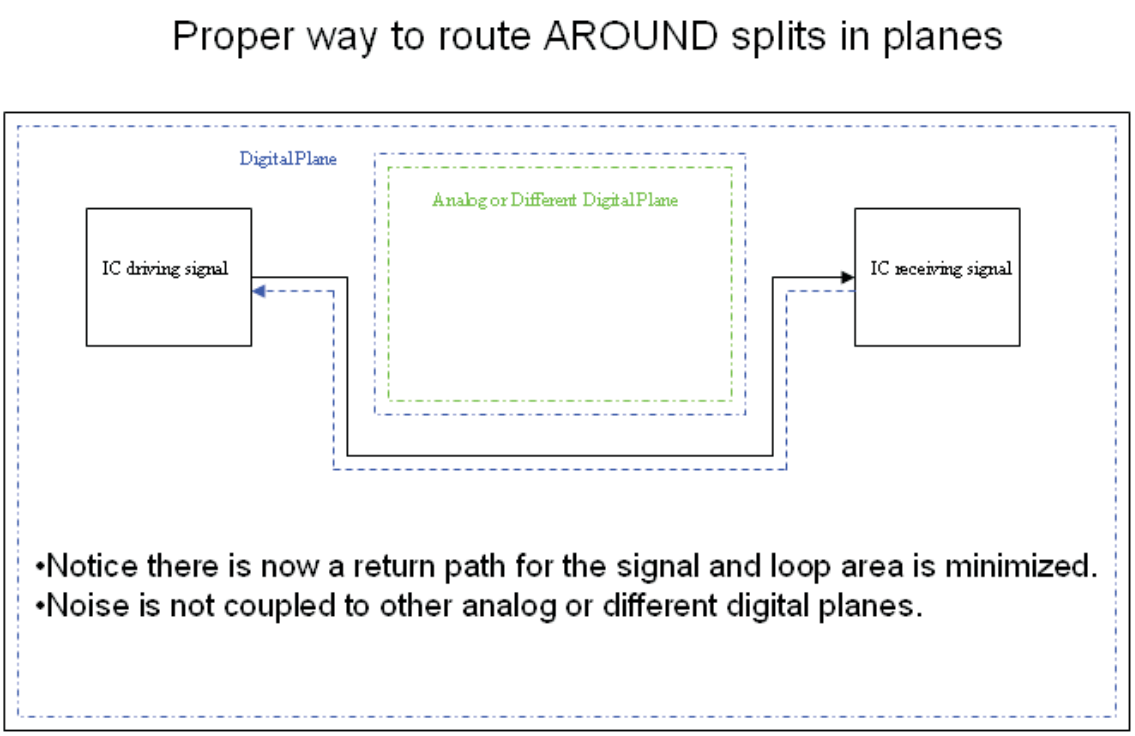


Figure 4-5. Proper Routing

4.4 Avoiding Crosstalk

Crosstalk is defined as interference from one trace to another by either or both inductive and capacitive coupling. Best ways to avoid crosstalk are:

- Provide stable reference planes for all high speed signals (as noted in previous sections).
- Use the 3W rule (3 times the width of trace for separation) where applicable on all signals, but absolutely use on clock signals.
- Use ground traces/guards around either “victim” or “aggressor” signals prone to crosstalk.
- When constrained and space limited on areas of the PCB to route parallel buses, series and/or end termination resistors can be used to route traces closer than what is normally recommended. However, calculations and simulations must be done to validate the use of series or end termination resistors to eliminate crosstalk.

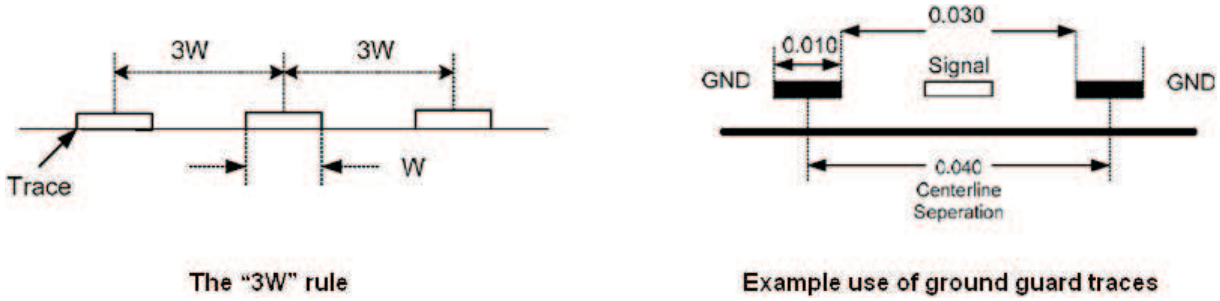


Figure 4-6. Ways to Avoid Crosstalk

USB Connection

5.1 Overview

There are three sets of differential pairs associated with each SuperSpeed USB port. One set for High-Speed and two sets for SuperSpeed.

WARNING

Do not connect the USB2 and SS USB connections on one USB3 connector to two different host chips. For instance, do not use the SS USB TX/RX from the TUSB73x0 and the USB2 DP/DM from another USB2 host.

Doing this may cause USB compliance failures and xHCI driver issues.

5.2 Internal Chip Trace Length Mismatch

Routing of the differential pair on the PCB will need to account for length mismatch in the package. This is due to offset pin and the associated bond wire mismatch.

Table 5-1. Length Mismatch

NetName	Bondwire Length (mil)	Difference (mil)
USB_SSTXN_DN1	96	20
USB_SSTXP_DN1	116	
USB_SSRXN_DN1	91	20
USB_SSRXP_DN1	111	
USB_DM_DN1	83	22
USB_DP_DN1	105	
USB_SSTXP_DN2	104	31
USB_SSTXN_DN2	73	
USB_SSRXP_DN2	67	27
USB_SSRXN_DN2	94	
USB_DM_DN2	127	34
USB_DP_DN2	93	
USB_SSTXP_DN3	73	30
USB_SSTXN_DN3	103	
USB_SSRXP_DN3	82	31
USB_SSRXN_DN3	113	
USB_DP_DN3	104	34
USB_DM_DN3	138	
USB_SSTXP_DN4	58	24
USB_SSTXN_DN4	82	
USB_SSRXP_DN4	58	22
USB_SSRXN_DN4	80	
USB_DM_DN4	86	26
USB_DP_DN4	60	

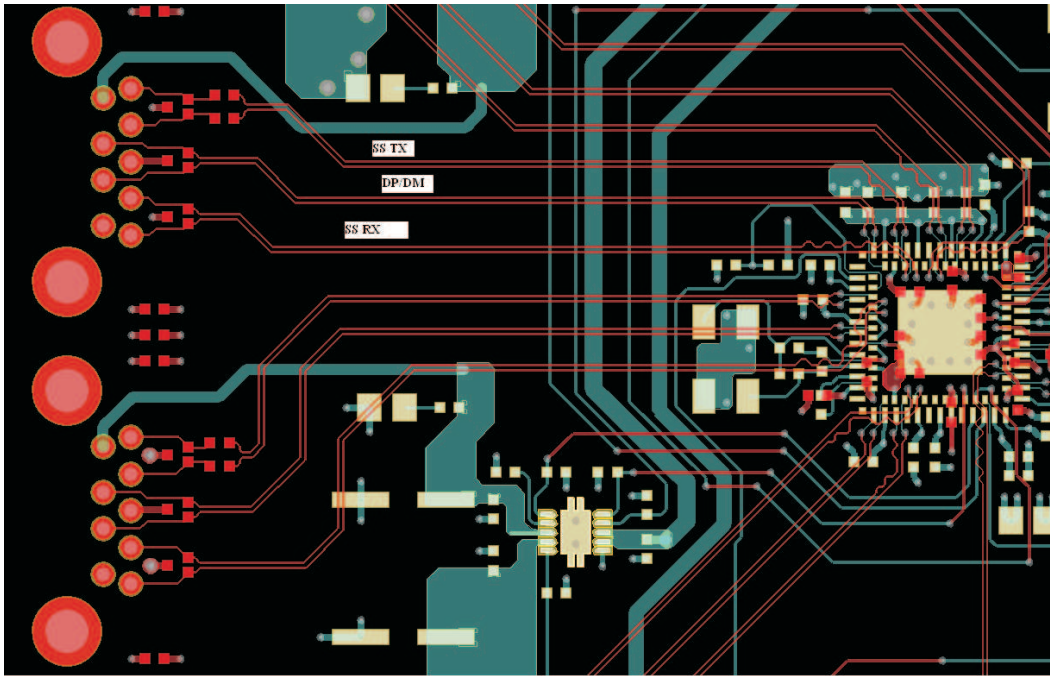


Figure 5-1. USB3 and USB2 Signals from the USB Connector to the Device

Figure 5-2 shows length matching at the device. Length matching must be done at the device side, not at the connector.

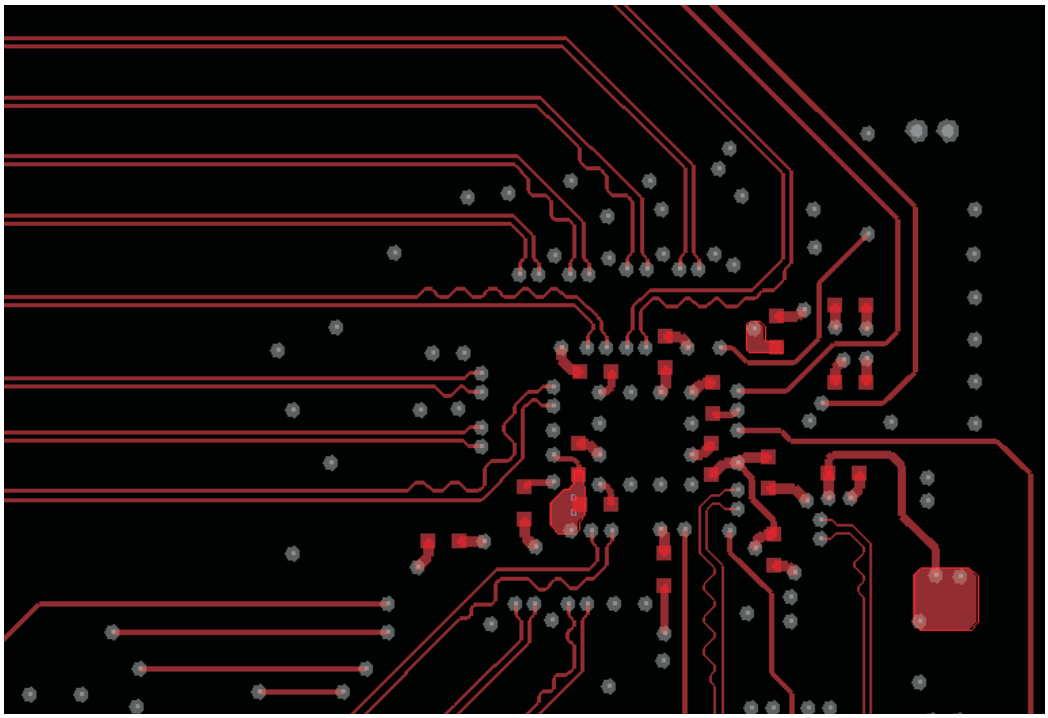


Figure 5-2. Length Matching

5.3 High-Speed Differential Routing

The high-speed differential pair (USB_DM and USB_DP) is connected to a type A USB connecter. The differential pair traces should be routed with 90 Ω ±15% differential impedance. The high-speed signal pair should be trace length matched. Max trace length mismatch between high speed USB signal pairs should be no greater than 150 mils. Keep total trace length to a minimum, if routing longer than eight inches contact TI to address signal integrity concerns.

Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. No termination or coupling caps are required. If a common mode choke is required then place the choke as close as possible to the USB connector signal pins. Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke).

For more detailed information, you may also see the USB 2.0 Board Design and Layout Guidelines (SPRAAR7) which describes general PCB design and layout guidelines for the USB 2.0 differential pair (DP/DM).

5.4 SuperSpeed Differential Routing

SuperSpeed consists of two differential routing pairs, a transmit pair (USB_SSTXM and USB_SSTXP) and a receive pair (USB_SSRXM and USB_SSRXP). Each differential pair traces should be routed with 90 Ω ±15% differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between SuperSpeed USB signal pairs should be no greater than 5 mils. The total length for each differential pair can be no longer than eight inches, this is based on the SS USB compliance channel spec, and should be avoided if at all possible. TI recommends that the SS diff pairs be as short as possible.

The transmit differential pair does not have to be the same length as the receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. The transmitter differential pair requires 0.1-µF coupling capacitors for proper operation. The package/case size of these capacitors should be no bigger than 0402. C-packs are not allowed. The capacitors should be placed symmetrically as close as possible to the USB connector signal pins.

If a common mode choke is required, then place the choke as close as possible to the USB connector signal pins (closer than the transmitter capacitors). Likewise, ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke and transmitter capacitors).

It is permissible to swap the plus and minus on either or both of the SuperSpeed differential pairs. This may be necessary to prevent the differential traces from crossing over one another. However it is not permissible to swap the transmitter differential pair with the receive differential pair.

It is recommended to use a 2010 pad for the inside pins provided no pad is used for adjacent pins. Instead use a pad on one of the inside pins then for the next pad route the trace between the outer pins to a via.

There is enough space to route a 3.78-mil trace between the outside pads while leaving 5-mil spacing between the trace and pad, it is then possible to increase the trace width to 4 mils after the breakout. In Figure 5-3 the red pads are USB_SS_RXP/USB_SS_RXN and the blue pads are USB_SS_TXP/USB_SS_TXN.

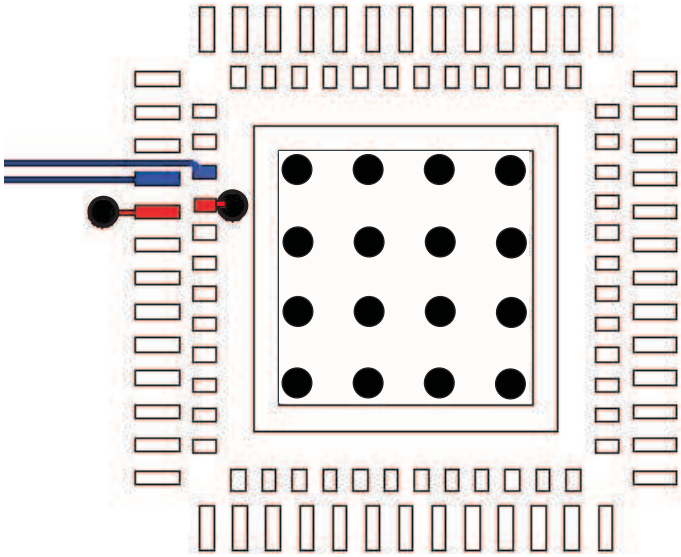


Figure 5-3. Differential Routing

In order to minimize cross-talk on the SS USB differential signal pair, it is recommended that the spacing between the TX and RX signal pairs for each interface be five times the width of the trace (5W rule). For instance, if the SS USB TX differential pair trace width is 5 mils, then there should be 25 mils of space between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

Package and Breakout

6.1 Package Drawing

See Mechanical Data for RKM package (MPQF258A).

6.2 Routing Between Pads

Figure 6-1 illustrates a 0.10-mm trace width and 0.125-mm space, with a 20-mil via pad with 0.10-mm gap to nearest metal.

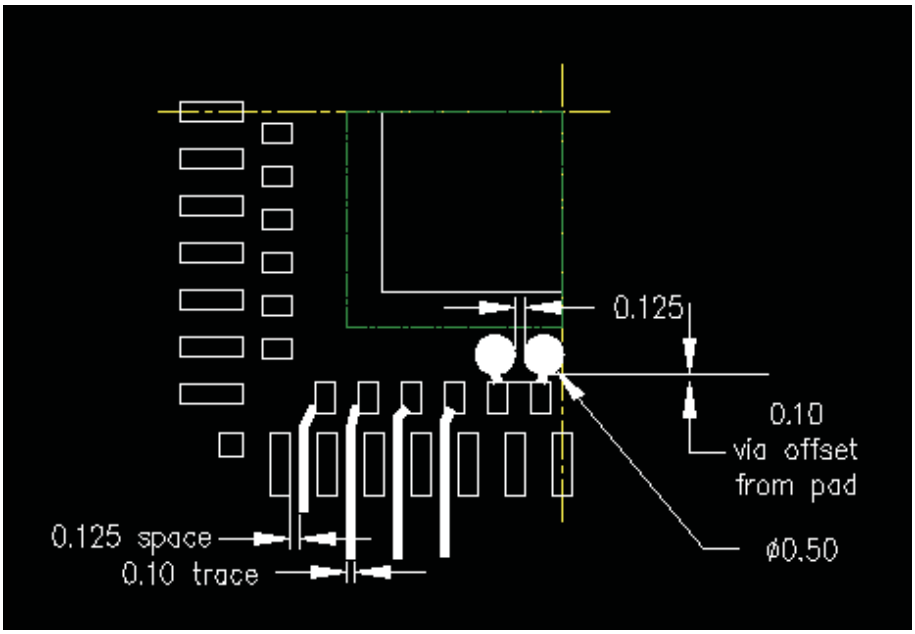


Figure 6-1. Routing Between Pads

6.3 Pads

It is recommended that a “Non Solder Mask Defined Pad” (NSMD) be used. This type of stencil will have an area greater than the actual pad size.

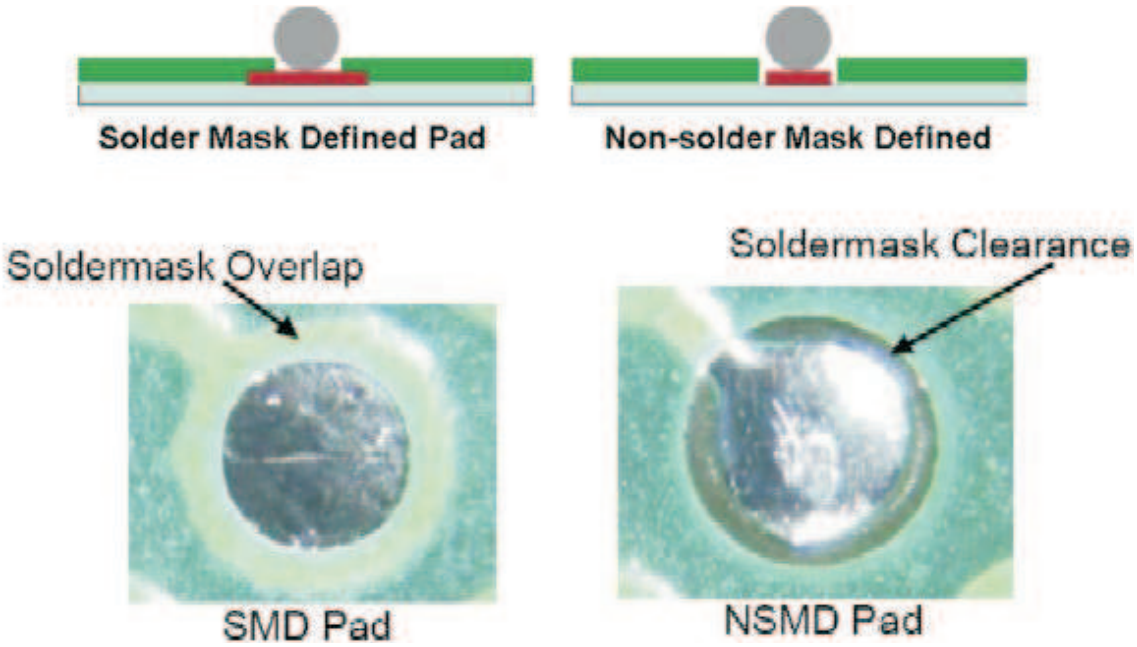


Figure 6-2. Pads

6.4 Land Pattern Recommendation

See Land Pattern for RKM package (LPPD235).

6.5 Solder Stencil

The solder mask is defined as a 1:1 ratio.

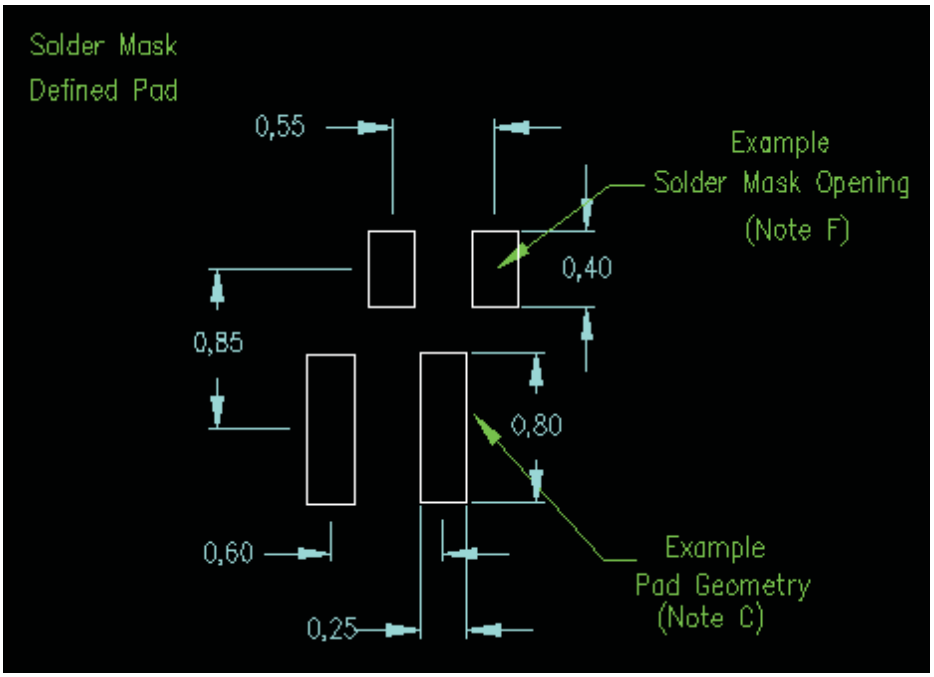


Figure 6-3. Solder Mask

For the thermal pad, a 0.10-mm stencil thickness is recommended. The actual package exposed pad is 5.5 mm x 5.5 mm.

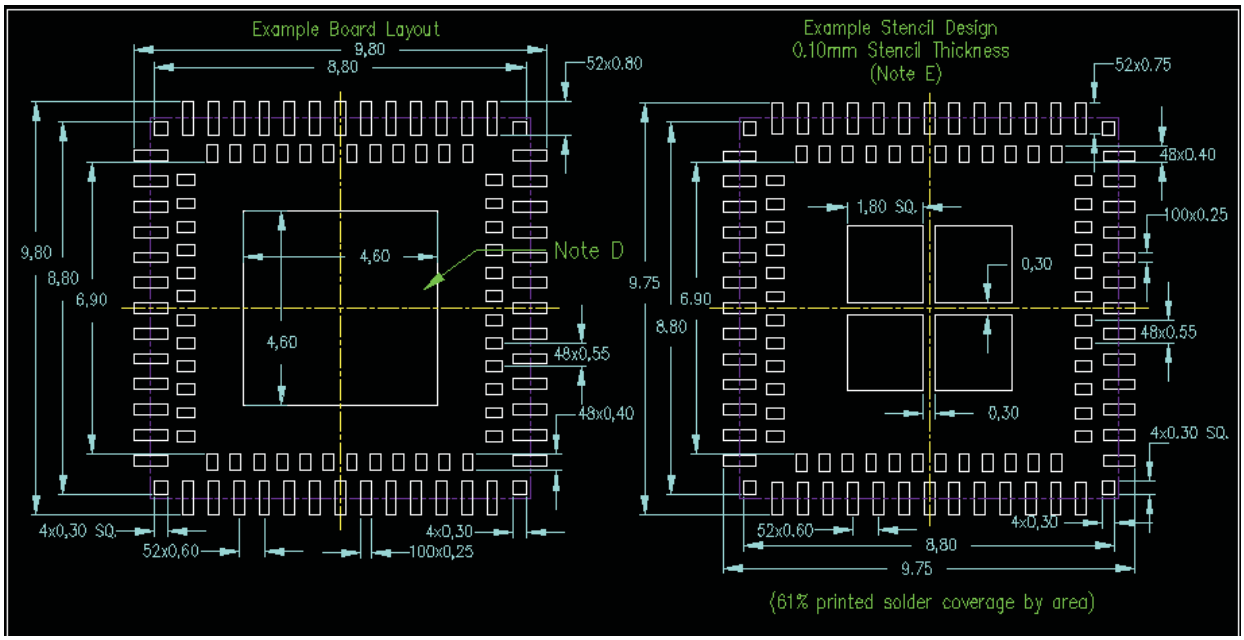


Figure 6-4. Thermal Pad Stencil Thickness

PCI Express Connection

7.1 Internal Chip Trace Length Mismatch

Routing of the differential pair on the PCB will need to account for length mismatch in the package. This is due to offset pin and the associated bond wire mismatch.

Table 7-1. Internal Chip Trace Length Mismatch

NetName	Bondwire Length (mil)	Difference (mil)
PCIE_TXN	118	28
PCIE_TXP	89	
PCIE_RXN	112	27
PCIE_RXP	85	
PCIE_REFCLKN	87	19
PCIE_REFCLKP	106	

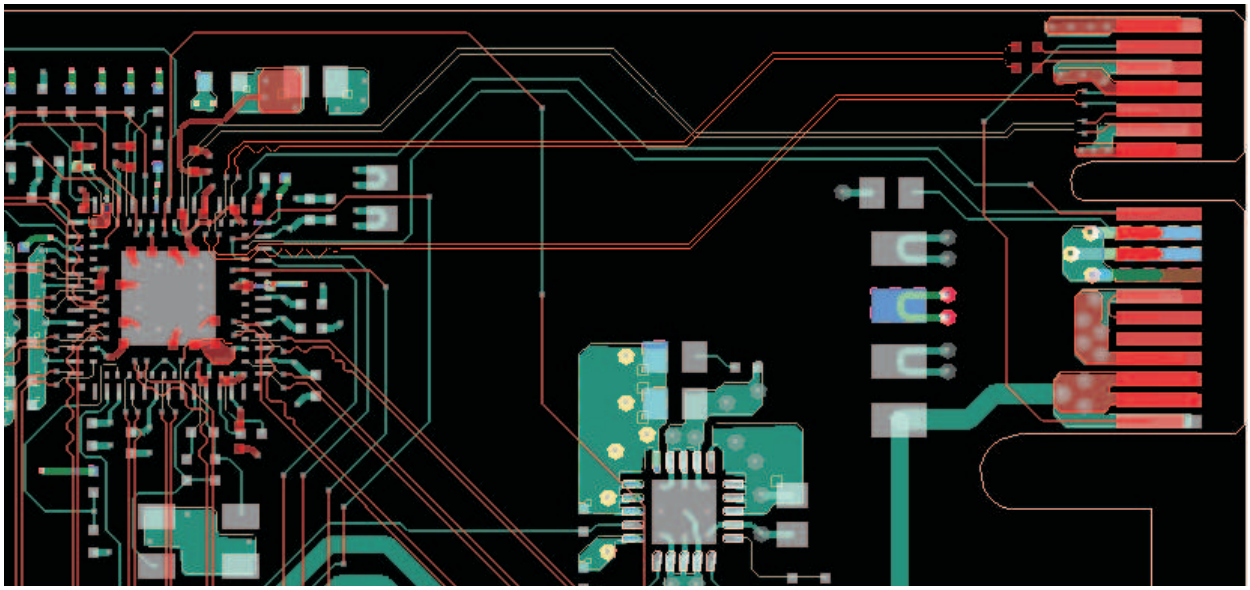


Figure 7-1. PCIe TX and RX Signals from the Edge Connector to the Device

Length matching must be done at the device side, not at the connector.

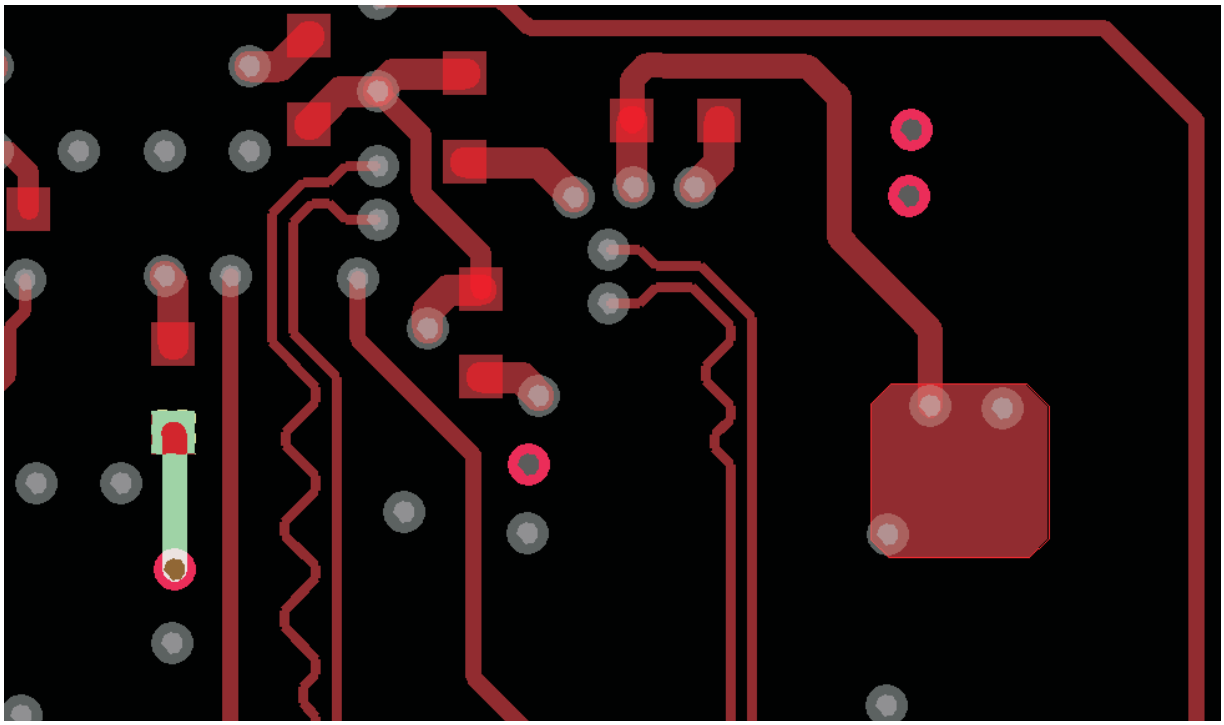


Figure 7-2. Length Matching at the Device

7.2 Transmit and Receive Links

The TUSB73x0 has an x1 PCI Express interface that runs at 5-Gb/s and is fully compliant to the PCI Express Base Specification, Revision 2.0.

The TUSB73x0 TX and RX terminals attach to the upstream PCI Express device over a 5-Gb/s high-speed differential transmit and receive PCI Express x1 Link. The connection details are provided in the following table.

It is permissible to swap the plus and minus on either or both of the PCIe differential pairs. This may be necessary to prevent the differential traces from crossing over one another. However it is not permissible to swap the transmitter differential pair with the receive differential pair.

In order to minimize cross-talk on the PCIe differential signal pair, it is recommended that the spacing between the TX and RX signal pairs for each interface be five times the width of the trace (5W rule). For instance, if the PCIe TX differential pair trace width is 5 mils, then there should be 25 mils of space between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

Table 7-2. Transmit and Receive Terminals

TUSB73x0 Terminal Name	Upstream PCIe Device Terminal Name	Description
TXP	RXP	TUSB73x0 transmit positive differential terminal connects to the upstream device receive positive differential terminal.
TXP	RXN	TUSB73x0 transmit negative differential terminal connects to the upstream device receive negative differential terminal.
RXP	TXP	TUSB73x0 receive positive differential terminal connects to the upstream device transmit positive differential terminal.
RXN	TXP	TUSB73x0 receive negative differential terminal connects to the upstream device transmit negative differential terminal.

The TUSB73x0 TXP and TXN terminals comprise a low-voltage, 100-Ω differential signal pair. The RXP and RXN terminals for the TUSB73x0 receive a low-voltage, 100-Ω differential signal pair. The TUSB73x0 has integrated 50-Ω termination resistors to VSS on both the RXP and RXN terminals eliminating the need for external components.

The TX lane of the differential signal pair must be ac-coupled. The recommended value for the series capacitor is 0.1 μF. To minimize stray capacitance associated with the series capacitor circuit board solder pads, 0402 sized capacitors are recommended.

When routing a 5-Gb/s low-voltage, 100-Ω differential signal pair, the following circuit board design guidelines must be considered:

1. The PCI-Express drivers and receivers are designed to operate with adequate bit error rate margins over a 20-inch maximum length signal pair routed through FR4 circuit board material.
2. Each differential signal pair must have a 100-Ω differential impedance, with each single-ended lane measuring in the range of 50-Ω to 55-Ω impedance to ground.
3. The differential signal trace lengths associated with a PCI Express high-speed link must be length matched to minimize signal jitter. This length matching requirement applies only to the P and N signals within a differential pair. The transmitter differential pair does not need to be length matched to the receiver differential pair. The absolute maximum trace length difference between the TXP signal and TXN signal must be less than 5 mils. This also applies to the RXP and RXN signal pair.
4. If a differential signal pair is broken into segments by vias, series capacitors, or connectors, the length of the positive signal trace must be length matched to the negative signal trace for each segment. Trace length differences over all segments are additive and must be less than 5 mils.
5. The location of the series capacitors is critical. For add-in cards, the series capacitors are located between the TXP/TXN terminals and the PCI-Express connector. In addition, the capacitors are placed near the PCI Express connector. This translates to two capacitors on the motherboard for the downstream link and two capacitors on the add-in card for the upstream link. If both the upstream device and the downstream device reside on the same circuit board, the capacitors are located near the TXP/TXN terminals for each link.
6. The number of vias must be minimized. Each signal trace via reduces the maximum trace length by approximately 2 inches. For example: if 6 vias are needed, the maximum trace length is 8 inches.
7. When routing a differential signal pair, 45° angles are preferred over 90° angles. Signal trace length matching is easier with 45° angles and overall signal trace length is reduced.
8. The differential signal pairs must not be routed over gaps in the power planes or ground planes. This causes impedance mismatches.
9. If vias are used to change from one signal layer to another signal layer, it is important to maintain the same 50-Ω impedance reference to the ground plane. Changing reference planes causes signal trace impedance mismatches. If changing reference planes cannot be prevented, bypass capacitors connecting the two reference planes next to the signal trace vias will help reduce the impedance mismatch.
10. If possible, the differential signal pairs must be routed on the top and bottom layers of a circuit board. Signal propagation speeds are faster on external signal layers.

7.3 PCI-Express Reference Clock Input

The TUSB73x0 requires an external reference clock for the PCI-Express interface. The PCI Express Base Specification and PCI Express Card Electromechanical Specification provide information concerning the requirements for this reference clock. The TUSB73x0 is designed to meet all stated specifications when the reference clock input is within all PCI Express operating parameters. This includes both standard clock oscillator sources or spread spectrum clock oscillator sources.

The TUSB73x0 supports a 100-MHz common differential reference clock. The PCI Express clock is typically a system-wide, 100-MHz differential reference clock. A single clock source with multiple differential clock outputs is connected to all PCI Express devices in the system. The differential connection between the clock source and each PCI Express device is point-to-point. This system implementation is referred to as a common clock design.

The TUSB73x0 is optimized for this type of system clock design. The REFCLK+ and REFCLK- terminals provide differential reference clock inputs to the TUSB73x0. The circuit board routing rules associated with the 100-MHz differential reference clock are the same as the 5-Gb/s TX and RX link routing rules itemized in Section 7.2. The only difference is that the differential reference clock does not require series capacitors. The requirement is a DC connection from the clock driver output to the TUSB73x0 receiver input. Electrical specifications for these differential inputs are included in the TUSB73x0 Data Manual.

Terminating the differential clock signal is circuit board design specific. But, the TUSB73x0 design has no internal 50-Ω to ground termination resistors. Both REFCLK inputs, at approximately 20 kΩ to ground, are high-impedance inputs.

7.4 PCI Express Reset

The TUSB73x0 PCI Express reset (PERST) terminal connects to the upstream PCI Express device's PERST output. The PERST input cell has hysteresis and is operational during both the main power state and V_{AUX} power state. No external components are required.

Please reference the TUSB73x0 Data Manual and PCI-Express Card Electromechanical Specification to fully understand the PERST electrical requirements and timing requirements associated with power-up and power-down sequencing. Also, the Data Manual identifies all configuration and memory-mapped register bits that are reset by PERST.

7.5 PCI Express WAKE/CLKREQ

7.5.1 Leakage Current on Pins WAKE# and CLKREQ#

WAKE# and CLKREQ# pins are high impedance (~4.5 MΩ) pins and a positive constant current of 1 µA flowing into the pins could develop 4.5 V at the pin. When the V_{DD33} is at 0 V the pin can be overstressed and cause permanent leakage.

Care should be taken on pins WAKE# and CLKREQ# when V_{DD33} is at 0 V. If a voltage over 4.6 V is applied to these pins when V_{DD33} = 0, the pins could be degraded causing a leakage current. 4.6-V is above the maximum rated voltage (V_{DD33} + 0.5) and above the maximum operating voltage of 3.3 V.

This stress condition does not occur in normal operation mode where the maximum voltage that could be seen at WAKE# is 3.6 V.

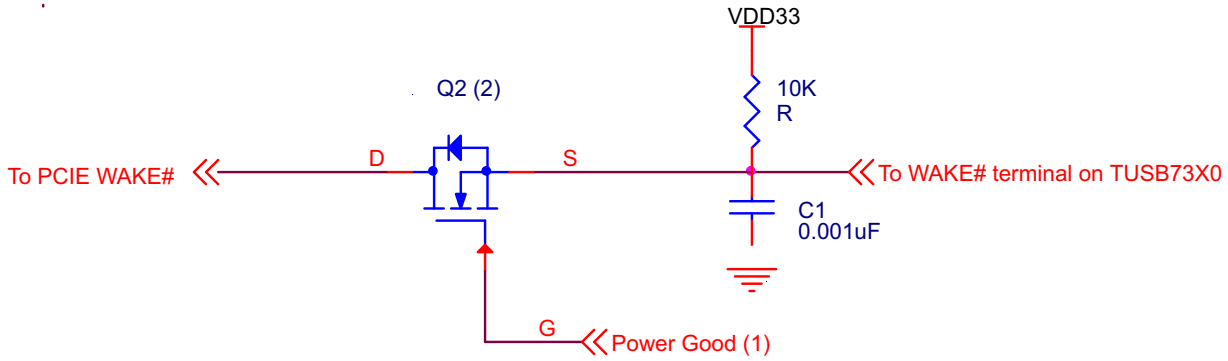
7.5.2 Recommendations

Care should be taken during 'Bed of Nail' or 'In Circuit Test' so that a constant current source is not used to test continuity on the WAKE# pin. A negative current test is recommended as there is a ground diode on the device that will clamp the voltage at the WAKE# and CLKREQ# pins.

Avoid using a handheld multimeter to test continuity of the WAKE# and CLKREQ# pins. Many multimeters use a constant current source that could be as high as 1 mA which could expose WAKE# and CLKREQ# pins to the high voltage.

On running projects that are already in production, if the stress voltage on the WAKE# pin of TUSB7320 < 4.6 V when V_{DD33} is zero, there is no risk on the shipping platform.

On new projects in design or projects that are not in mass production yet, TI suggests ODMs adding a FET (make sure parasitic diode is reversed bias) and 10-kΩ pull up resistor on WAKE# to prevent overstress (see Figure 7-3). Also, due to an erratum on TUSB73x0, a 0.001-µF capacitor to ground is required on the WAKE# and CLKREQ# signals. The rise time must be greater than 450 ns. See the errata (SLLZ067) for a more detailed explanation.



(1) Power Good is a 3.3-V signal asserted high when VDD33 is at its valid operating voltage (see Recommended Operating Conditions table in the Data Manual, SLLSE76).

(2) N-Channel MOSFET 2N7002 or 2N7002K are suitable devices for use in the circuit.

Figure 7-3. Connection of WAKE#

In all projects going forward, do not use constant current during 'In Circuit Test'. If that is not possible, omit WAKE# and CLKREQ# pins from the 'ICT'.

Wake from S3

8.1 Overview

WAKE is an open-drain output from the TUSB73x0 that is driven low to re-activate the PCI Express link hierarchy's main power rails and reference clocks. This PCI Express side-band signal is connected to the WAKE input on the upstream PCI Express device. WAKE is operational during both the main power state and V_{AUX} power state.

Since WAKE is an open-drain output, a system side pullup resistor is required to prevent the signal from floating. The drive capability of this open-drain output is 4 mA. Therefore, the value of the selected pullup resistor must be large enough to assure a logic low signal level at the receiver. A robust system design will select a pullup resistor value that de-rates the output driver current capability by a minimum of 50%. At 3.3 V with a de-rated drive current equal to 2 mA, the minimum resistor value is 1.65 kΩ. Larger resistor values are recommended to reduce the current drain on the V_{AUX} supply.

Hardware requirements for supporting wake from S3:

1. All power rails on the TUSB73x0 must remain powered.
2. AUX_DET terminal must be pulled high.
3. WAKE# terminal must be connected to PCIe bus wake signal.
4. A 0.001-µF capacitor should be placed on WAKE# terminal to ground.
5. VBUS must remain powered such that power can be applied to attached keyboard/mouse during S3.

The conditions for WAKE# to assert are:

1. The PME enable bit must be set (PME status bit must be cleared).
2. The PCIe link must be in D3.
3. PERST# must be asserted.
4. The TUSB73x0 has to receive the RESUME command from the attached USB peripheral.

Device Input Clock

9.1 Overview

The TUSB73x0 supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, it must be a 1.8-V clock source, XO should be left open and VSSOSC is connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below.

In Figure 9-1, XY1 is a dual crystal/oscillator footprint. To use a crystal only populate R13, C16, and C18. To use an oscillator only populate C17, R74, R75, and R76.

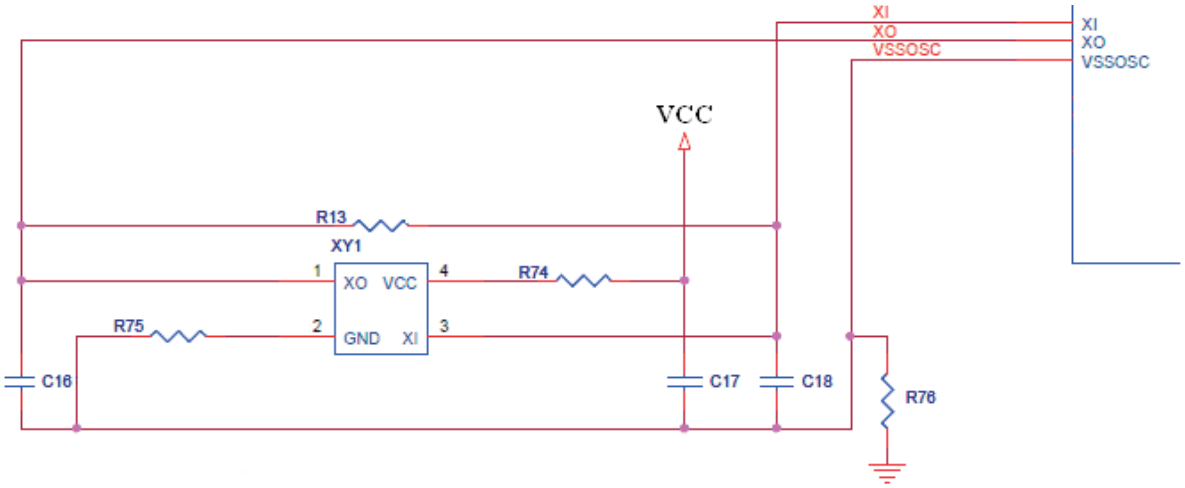


Figure 9-1. Dual Crystal/Oscillator Footprint

Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground if using a crystal.

Load capacitance (Cload) of the crystal varying with the crystal vendors is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors CL1 and CL2. The trace length between the decoupling capacitors and the corresponding power pins on the TUSB73x0 needs to be minimized. It is also recommended that the trace length from the capacitor pad to the power or ground plane be minimized.

See the TUSB73x0 Data Sheet for input clock parameters.

JTAG Interface

10.1 Overview

The TUSB73x0 supports JTAG (IEEE 1149.1 and 1149.6) for board level test. Contact TI for BSDL files.

The JTAG TRST signal must be pulled to ground for proper device operation.

Differential Pair ESD Protection

11.1 Overview

If more protection is required then the TPD2EUSB30 can be used, the device meets or exceeds IEC61000-4-2 (Level 4) requirements. This device can be used on any of the differential pairs and can be placed on a single layer and causes no signal distortion due to layout mismatch. Place the device as close as possible to the signal pins of the connector. Refer to the datasheet for more information regarding this device.

More information can be found at: http://focus.ti.com/docs/prod/folders/print/tpd2eusb30.html

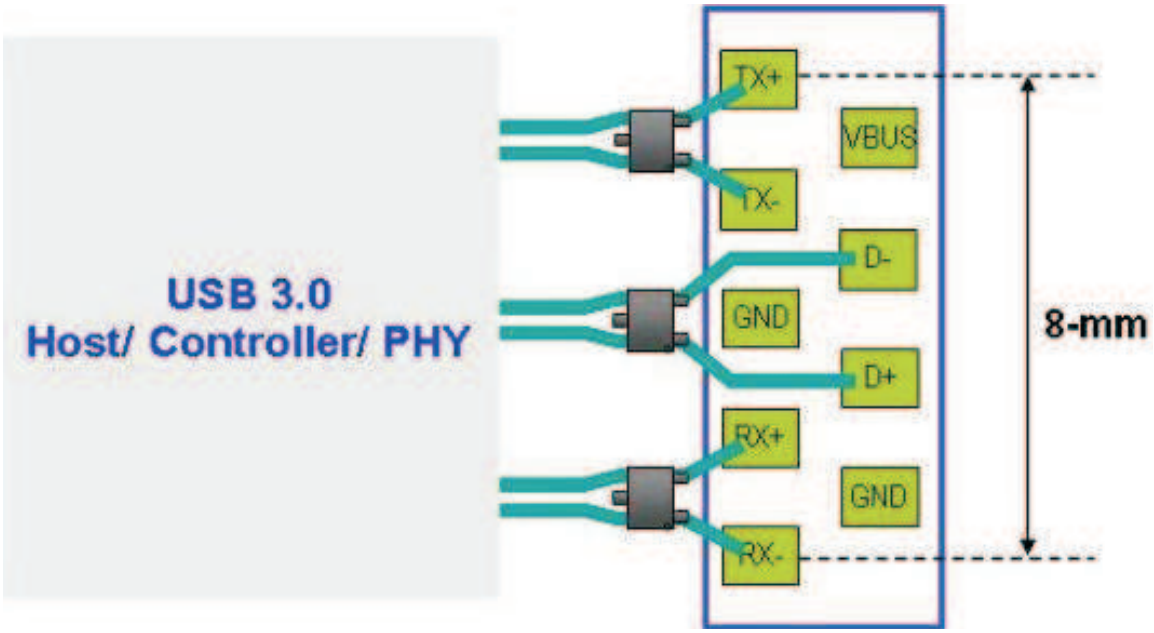


Figure 11-1. TPD2EUSB30 ESD Protection

SuperSpeed Redriver

12.1 Overview

The SN65LVPE502 USB SuperSpeed redriver (does not support the High Speed signals) can be used if the SuperSpeed differential pairs must be driven longer than eight inches, through connectors, or over less than desirable cables. This device makes “bad signals good” again. Refer to the datasheet for more information regarding this device.

More information can be found at: http://focus.ti.com/docs/prod/folders/print/sn65lvpe502.html

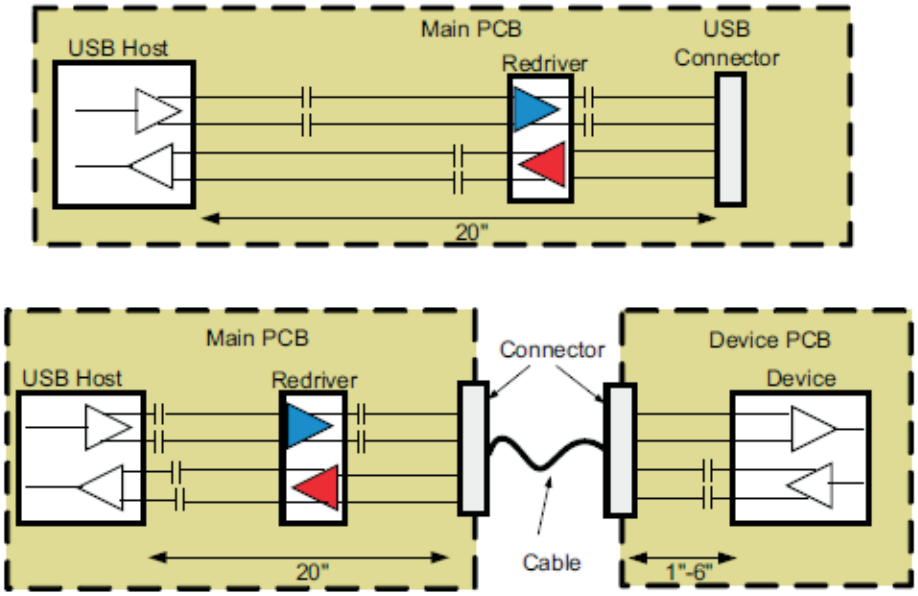


Figure 12-1. Typical Application of SuperSpeed Redriver

SMI Pin Implementation

13.1 Overview

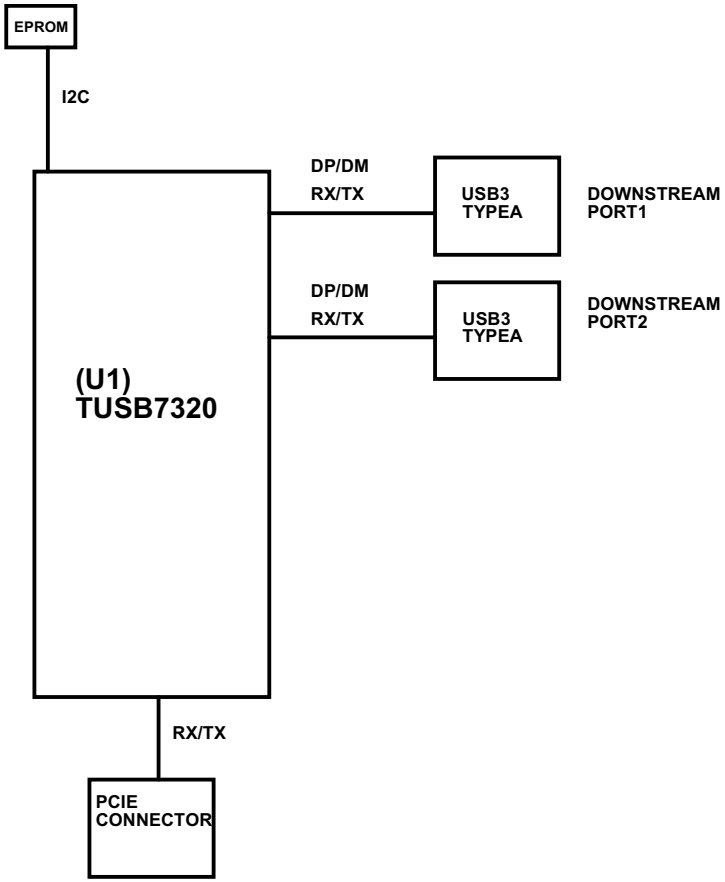
The SMI pin is actively driven by the TUSB73x0. It should not have a pull up resistor. To guarantee that no interrupts are generated when power is removed from the TUSB73x0, a pull down can be used. This is not required as long as the TUSB73x0 has a ground connection.

Schematics

14.1 Overview

The following pages contain schematics for the TUSB7320 and TUSB7340.

14.2 TUSB7320 DEMO EVM REVB Schematics



VIA AND TRACE REQUIREMENTS:
- MIN VIA PAD SIZE 20mils
- MIN spacing between trace and pad is 5mils
- MIN spacing between VIA and pad is 5mils
- MIN width of trace is 4mils

IMPEDANCE REQUIREMENTS:
- USB_DP/M must be 90-ohm differential (+/-15%)
- USB_SSTXP/N must be 90-ohms differential (+/-15%)
- USB_SSRXP/N must be 90-ohms differential (+/-15%)
- PCIE_TXP/N must be 100-ohms differential (+/-10%)
- PCIE_RXP/N must be 100-ohms differential (+/-10%)
- PCIE_REFCLKP/N must be 100-ohms differential (+/-10%)

LENGTH MATCHING REQUIREMENTS:
- USB_DP/M within 25mils.
- USB_SSTXP/N within 5mils
- USB_SSRXP/N within 5mils
- PCIE_TXP/N within 5mils
- PCIE_RXP/N within 5mils
- PCIE_REFCLKP/N within 25mils.

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TUSB7320 DEMO REVB_48		
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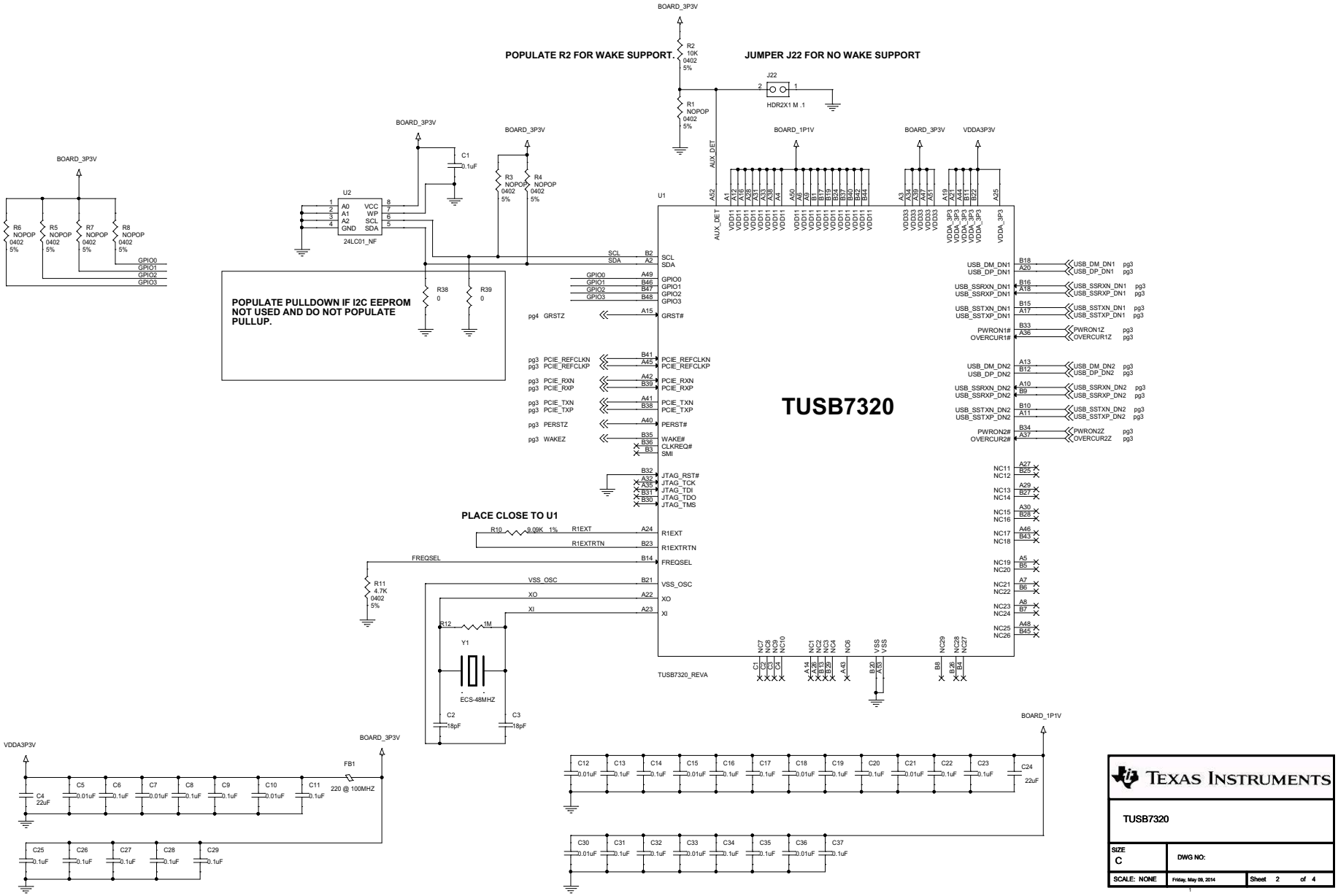
SCALE: NONE	Friday, May 09, 2014	Sheet 1 of 4



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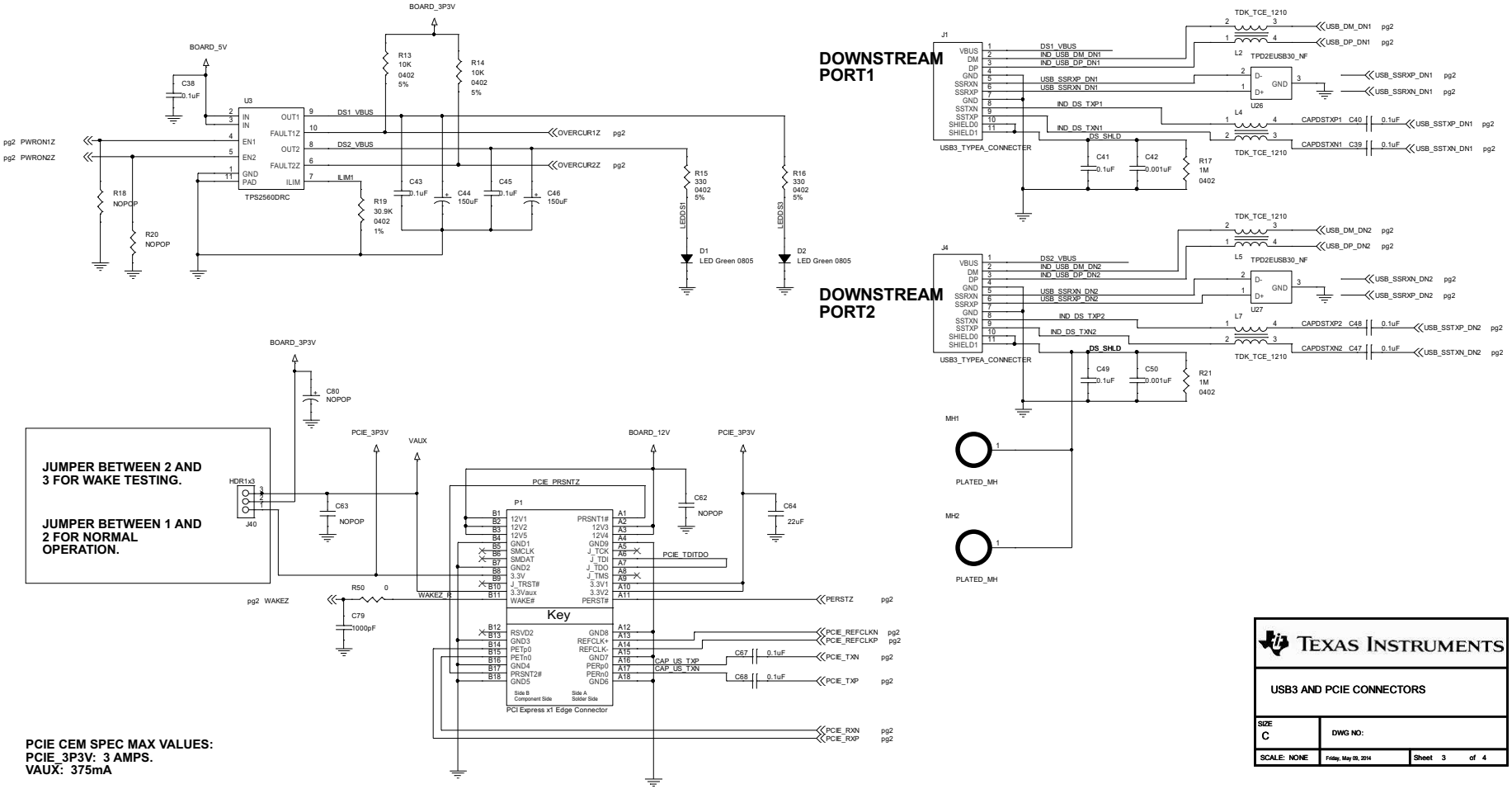
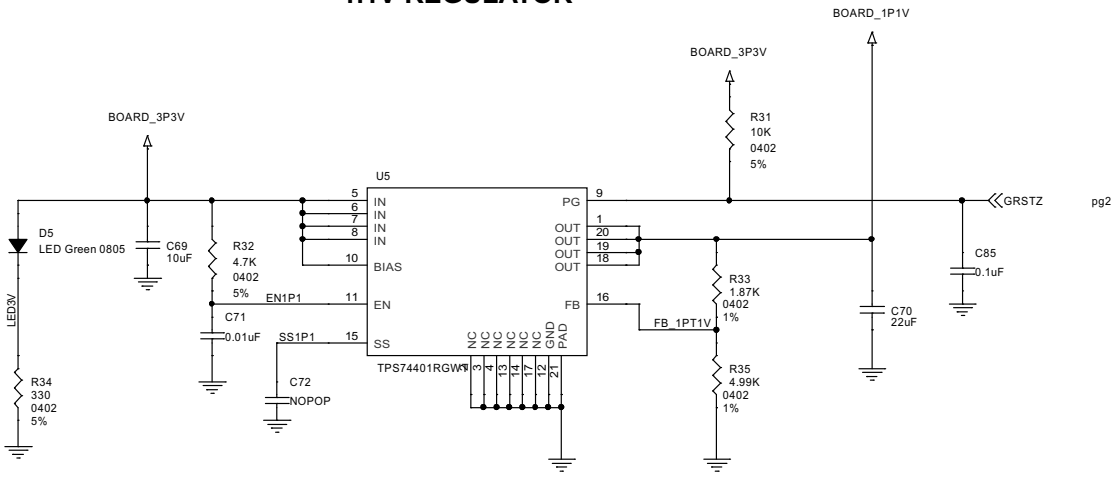


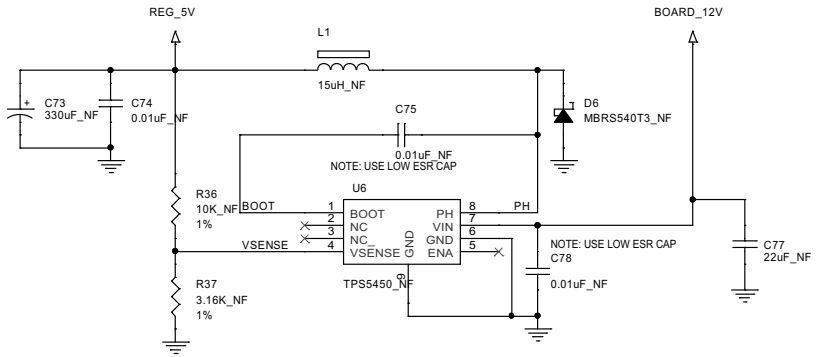
1.1V REGULATOR



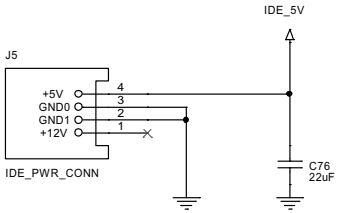
R33	R35	OUTPUT
1.13K	4.53K	1.0V
1.37K	4.42K	1.05V
1.87K	4.99K	1.1V (DEFAULT)
2.49K	4.99K	1.2V

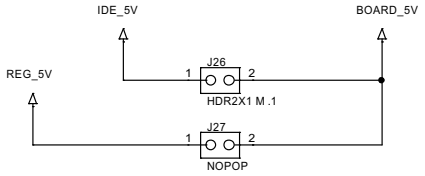
5V VBUS OPTIONS

OPTION 1: 5V REGULATOR



OPTION 2: 5V FROM IDE CONNECTOR





NOTE: ONLY POPULATE ONE OPTION

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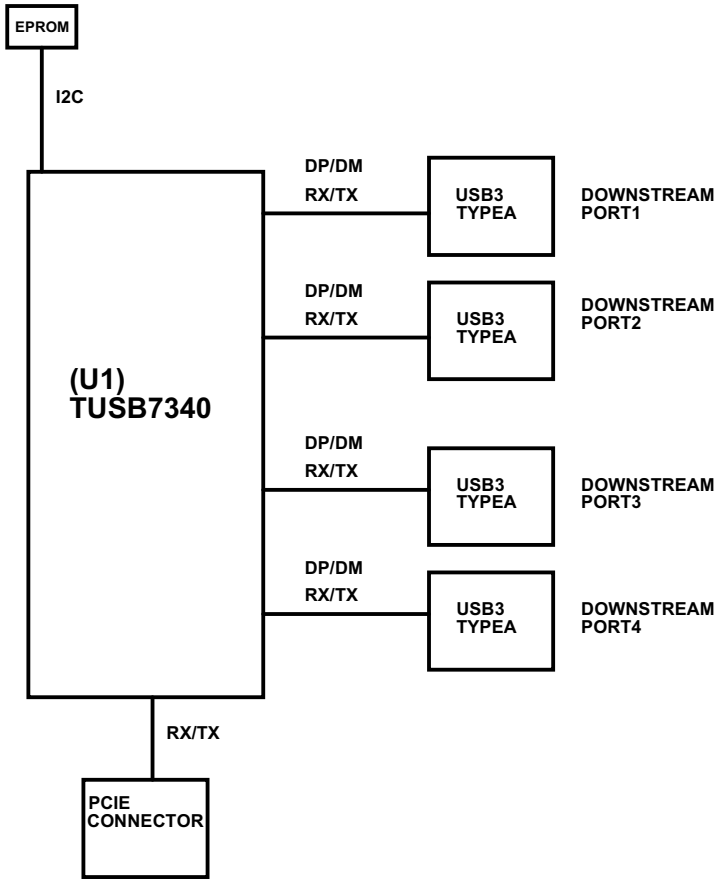
14.3 TUSB7340 DEMO EVM REVB Schematics



VIA AND TRACE REQUIREMENTS:
- MIN VIA PAD SIZE 20mils
- MIN spacing between trace and pad is 5mils
- MIN spacing between VIA and pad is 5mils
- MIN width of trace is 4mils

IMPEDANCE REQUIREMENTS:
- USB_DP/M must be 90-ohm differential (+/-15%)
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- USB_SSRXP/N must be 90-ohms differential (+/-15%)
- PCIE_TXP/N must be 100-ohms differential (+/-10%)
- PCIE_RXP/N must be 100-ohms differential (+/-10%)
- PCIE_REFCLKP/N must be 100-ohms differential (+/-10%)

LENGTH MATCHING REQUIREMENTS:
- USB_DP/M within 25mils.
- USB_SSTXP/N within 5mils
- USB_SSRXP/N within 5mils
- PCIE_TXP/N within 5mils
- PCIE_RXP/N within 5mils
- PCIE_REFCLKP/N within 25mils.

TEXAS INSTRUMENTS

TUSB7340_DEMO_REVB_48

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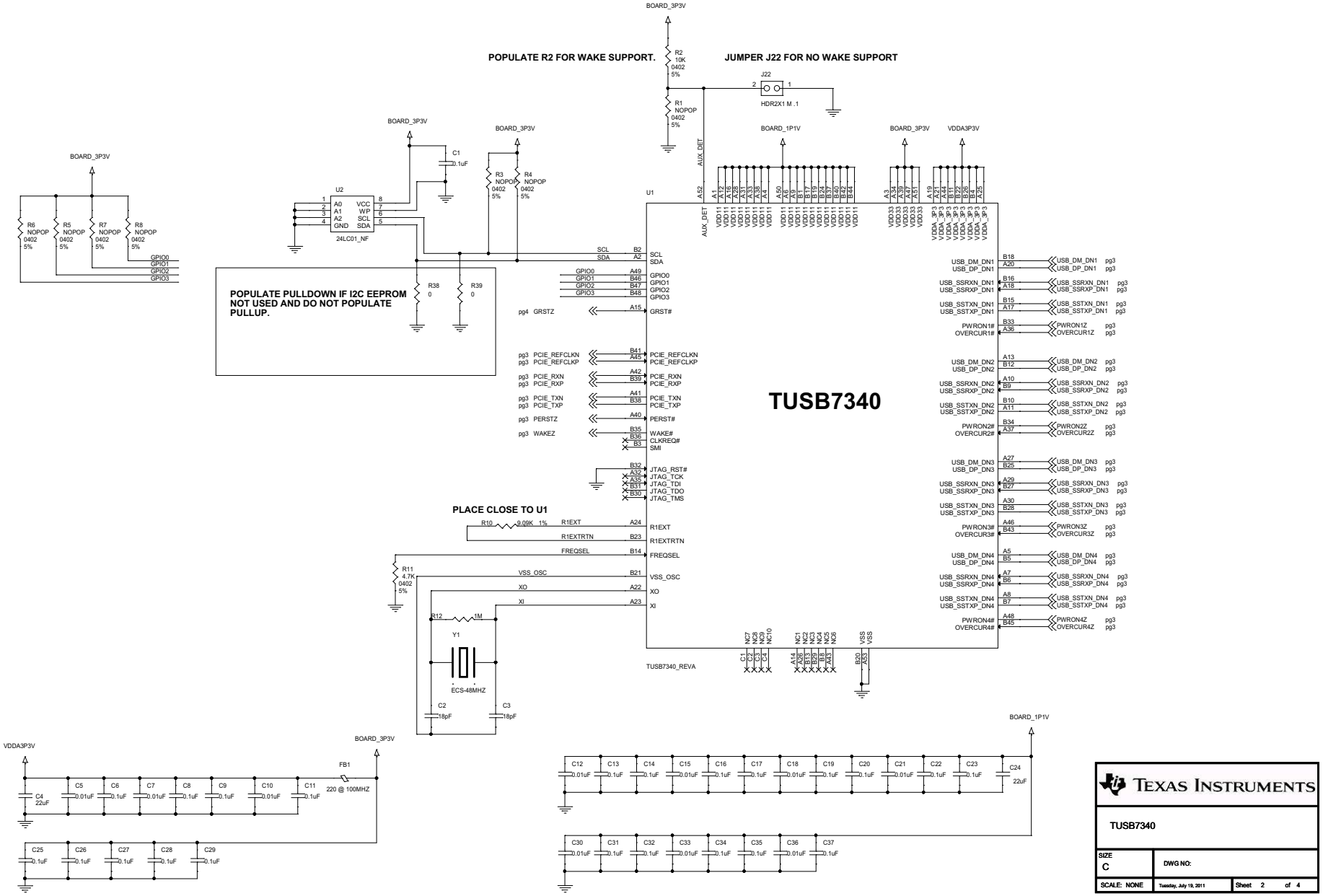
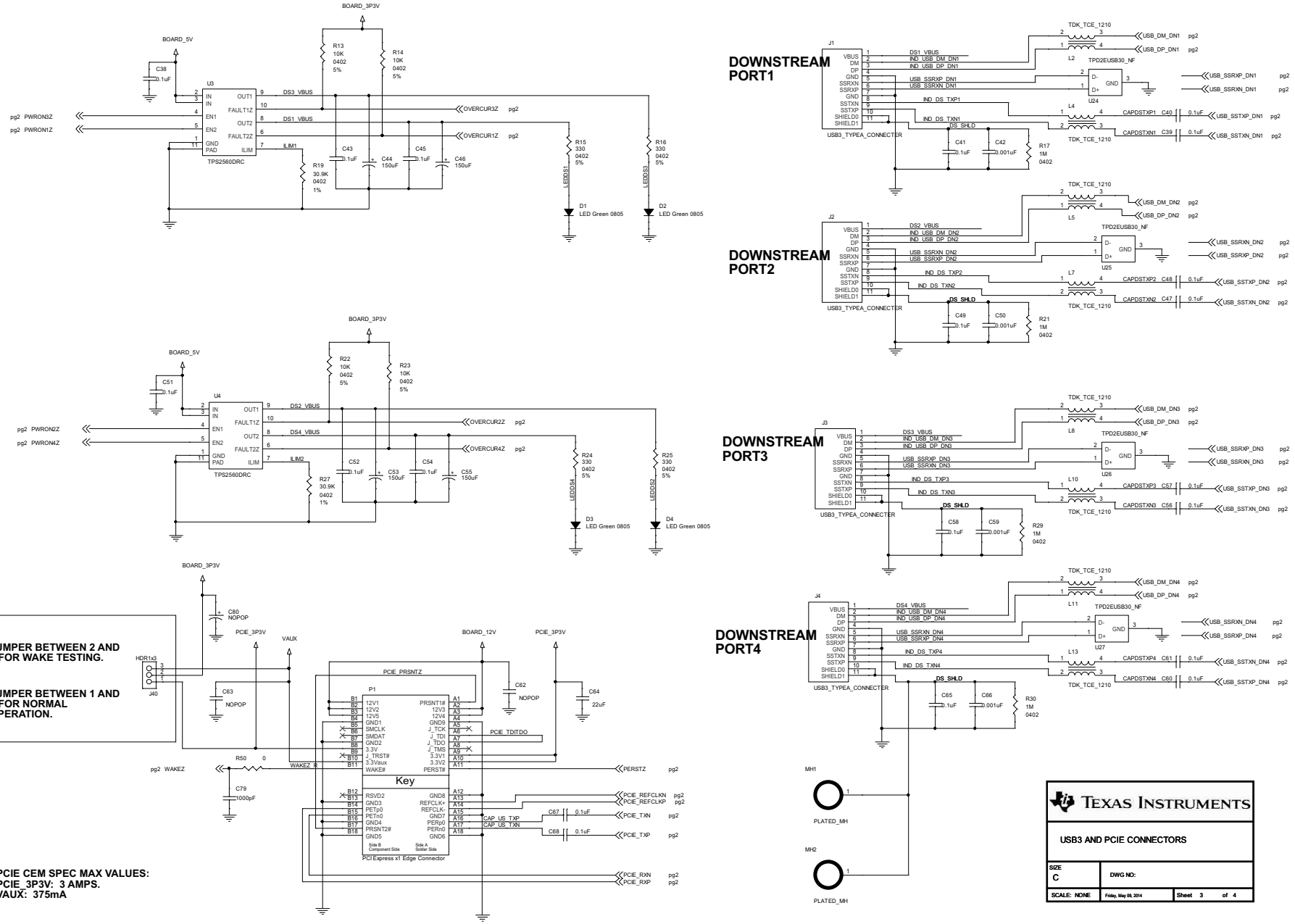
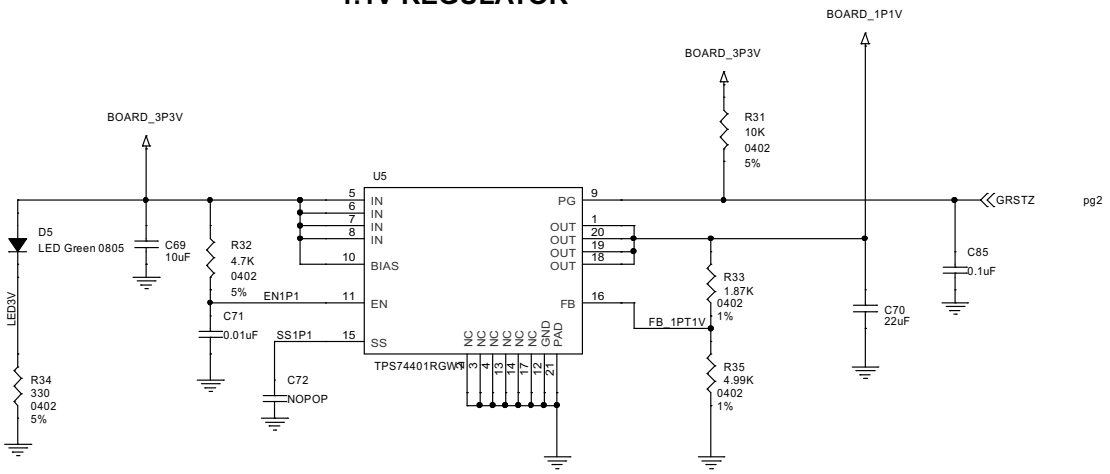




1.1V REGULATOR



R33	R35	OUTPUT
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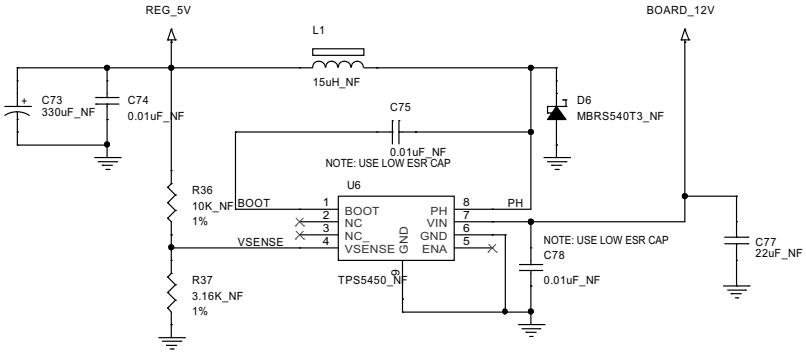
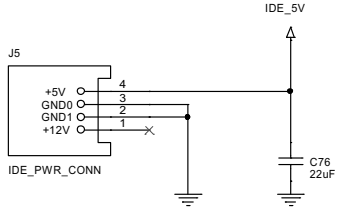
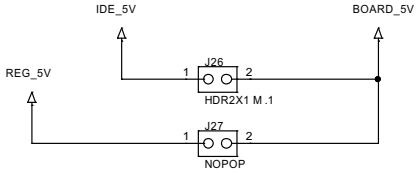
5V VBUS OPTIONS

OPTION 1: 5V REGULATOR



OPTION 2: 5V FROM IDE CONNECTOR





NOTE: ONLY POPULATE ONE OPTION

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from D Revision (May 2014) to E Revision **Page**

- Changed text in Chapter 1 From: "PC host system via a PCIe x1 Gen 2 interface" To: "PC host system via a PCIe x1 Gen 2 or PCIe Gen 1 interface" 7
- Changed TUSB7320 schematic. 37
- Changed TUSB7340 schematic. 41

Revision History

Changes from C Revision (October 2013) to D Revision **Page**

- Replaced - Chapter 15: Schematics with Rev. B_48 35

Revision History

Changes from B Revision (October 2013) to C Revision **Page**

- Deleted - Chapter 14: Failsafe IO 34

Revision History

Changes from A Revision (June 2012) to B Revision **Page**

- Replaced - Chapter 15: Schematics 35

Revision History

Changes from Original (June 2011) to A Revision **Page**

- Changed text in High-Speed Differential RoutingFrom: "if routing longer than six inches contact TI to address signal integrity concerns." To: "if routing longer than eight inches contact TI to address signal integrity concerns." 19
- Changed text in SuperSpeed RedriverFrom: "differential pairs must be driven longer than 11 inches" To: "differential pairs must be driven longer than eight inches." 33

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