# *SN65LV1021/SN65LV1212- SN65LV1023/SN65LV1224 10:1 Serializer/Deserializer Evaluation Board (EVM)*

**ABSTRACT**

This application report focuses the use and construction of a Serializer/Deserializer evaluation module (EVM) constructed to evaluate the characteristics of SN65LV1021/SN65LV1212 Serializers, and SN65LV1023/SN65LV1224 Deserializer devices. This document provides guidance on proper use by showing possible device configurations and test modes. It also provides design, layout, and schematic information, including specific construction recommendations. Information in this guide can be used to assist the customer in choosing the optimal design methods and materials in designing a complete system.

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**EVM DESCRIPTION**

The BLINK EVM provides a vehicle to evaluate the operation and conduct characterization measurements of Texas Instruments SN65LVDS1021/1023 Serializer and SN65LVDS1212/1224 Deserializer devices.

The board is setup to permit the independent evaluation of either Serializer or Deserializer devices through the use of external equipment to match the requirements of each device.

Design of the board provides for easy configuration changes that permit joining the devices at either their parallel ports or serial ports thus providing a vehicle for the evaluation of that interface between the two devices.

Standard SMA and RJ45 female connectors are provided to permit the serializing and data recovery evaluation utilizing standard interface cables of various lengths. A patch resistor network is permits selection of either set of connectors as it might be appropriate for evaluation and measurement of these signals.

Standard board shorting jumpers and be used to interconnect Deserializer to Serializer devices through the use of standard board-pin headers. These same headers provide a vehicle to interface with logic analyzers and pattern generators for the purpose of evaluating these devices.

Other configuration jumpers within the board permit the establishment of independent measurements loops for supply currents and or injection of separate external supplies sources.

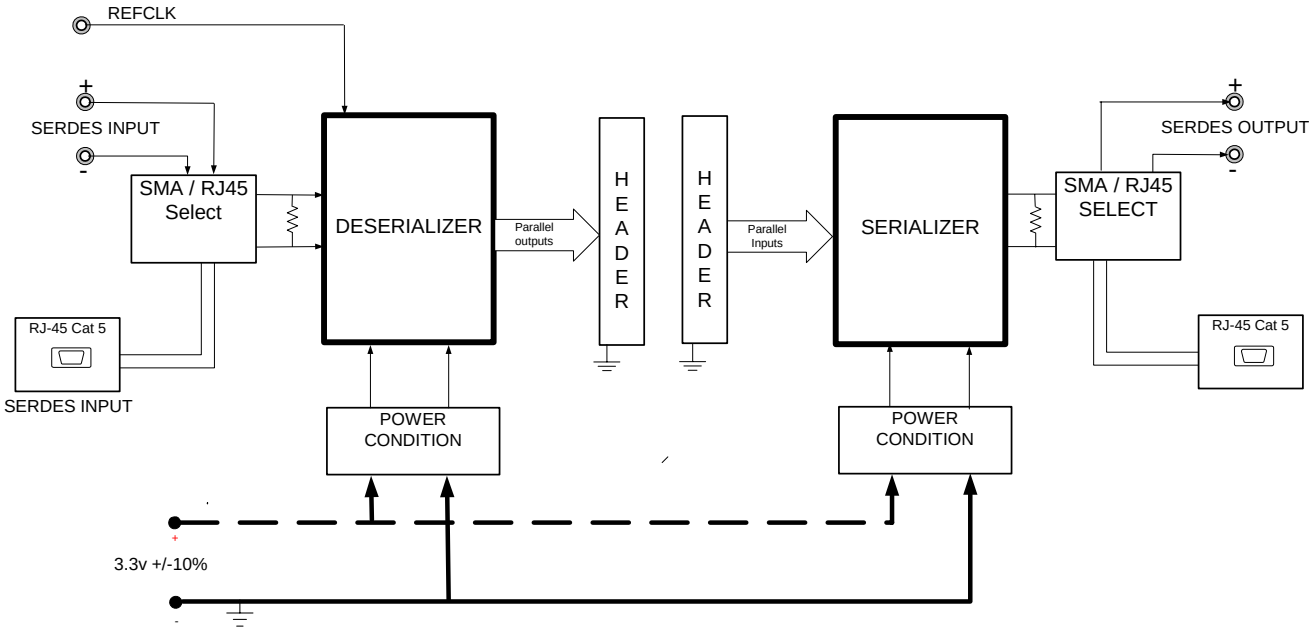



**Figure 1- B LINK Evaluation Board Block Diagram**

**Board Configuration**

The B LINK evaluation board can be configured to permit independent evaluation of either Serializer or Deserializer devices or joined in cooperation with each other as a pair. It is possible, through jumper configurations, to set up the board to perform DC and AC measurements such that only one of the devices is active while the other is taken totally out of the circuit without being an influence on the other. Both devices can be easily interfaced with the other by joining their high-speed side through cables or their low speed side through jumpers. This feature can be used to evaluate how each device interfaces with the other or each device as a stand alone through the use of external laboratory test equipment.
Table 1, corresponds to the way the board was configured prior to shipment from TI.
Figure 2, provides a simplified pictorial representation of the EVM and can be used to rapidly locate the jumper locations on the board.

Deserializer receive outputs and Serializer receive inputs are routed to terminal blocks BS3 and BS4, respectively. Figure 3 provides a additional information that may be used to identify signal distribution on the BS3 and BS4 terminal blocks. These terminal blocks provide a mechanism for connection to stimulus and measurement systems for parallel data timing control and evaluation. These terminal blocks provide a means for a simple interconnection of Deserializer and Serializer devices. The signals on these headers are set such that all pins on the outer edges of the header-group are grounds, while all signals output from the Deserializer and input to the Serializer are contained in the inner rows. This setup is easily connected to stimulus measurement s and data pattern generation hardware and it also allows for the easy interconnect of the parallel busses through standard 0.1 inch shorting jumpers.

**EVM Board Preparation**

Prior to applying power to the board verify that jumpers are properly installed as shown in Table 1-Jumpers Installation Table. Figure 2, provides a simplified top view of the EVM that can be used to assist in rapidly locating these jumpers on the board.

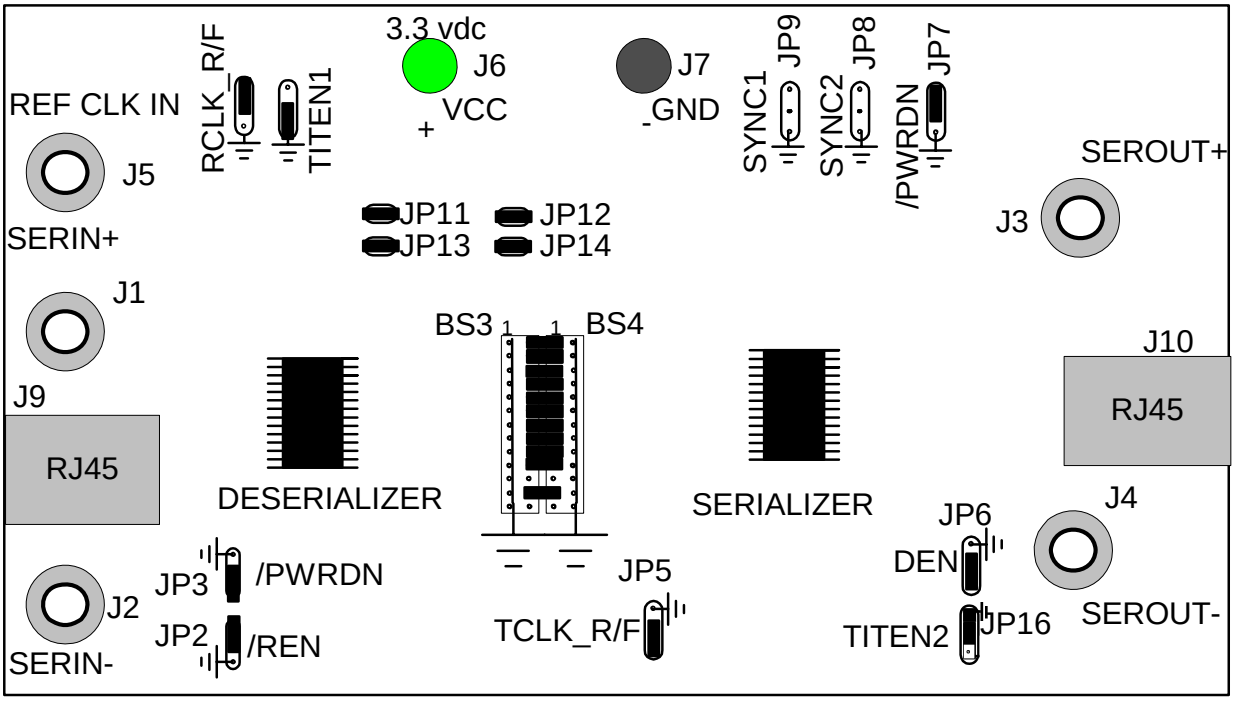



**Figure 2- B LINK EVM Default Jumpers Setup**

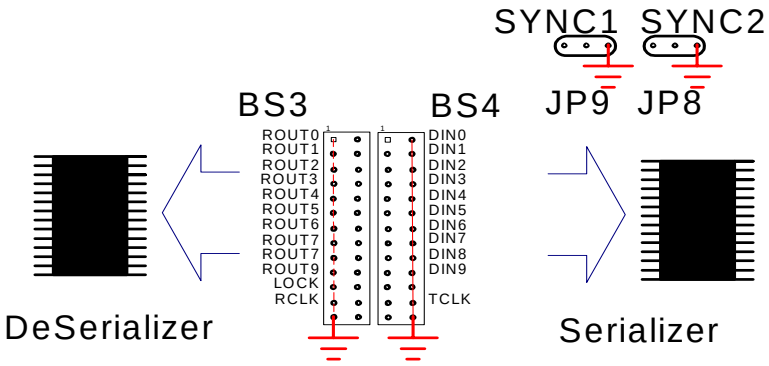



**Figure 3 – Deserializer-Serializer Interconnect Detail**

| Jumper | Default | Pin # | Function | Description |
|---|---|---|---|---|
| JP1 | Installed | 2-3 | RCLK_R/F | Deserializer's RCLK strobe edge selection (high selects rising edge) |
| JP2 | Installed | 2-3 | REN | Logic high input enables Deserializer's parallel output bus and RCLK into Lo-Z states |
| JP3 | Installed | 2-3 | /PWRDN | Deserializer Power-down control. Set to high input to maintain device active |
| JP5 | Installed | 2-3 | TCLK_R/F | Serializer's TCLK strobe edge selection (high selects rising edge ) |
| JP6 | Installed | 1-2 | DEN | Serializer output bus tri-state control. Set high enables serializer's output pair |
| JP7 | Installed | 1-2 | /PWRDN | Deserializer Power-down control. Set to high input to maintain device active. |
| JP8 | OFF | | SYNC2 | Logic high initiates serializer's 1024 sync patterns for rapid synchronization. May be connected to the Serializers LOCK to speed synchronization. |
| JP9 | OFF | | SYNC1 | |
| JP11 | Installed | 1-2 | Power | Digital Power In. to Deserializer pins12 and 23 |
| JP12 | Installed | 1-2 | Power | Digital Power In to Serializer pins 27 and 28 |
| JP13 | Installed | 1-2 | Power | Analog Power In to Deserializer pins 4 and 11 |
| JP14 | Installed | 1-2 | Power | Analog Power In to Serializer pins 17 and 26 |
| JP15 | Installed | 1-2 | TITEN1 | TI Factory Test Enable 1 |
| JP16 | Installed | 2-3 | TITEN2 | TI Factory Test Enable 2. |
| BS3>BS4 | Installed | BS3-26>BS4-1 | Data0 | ROUT0 > DIN0 |
| BS3>BS4 | Installed | BS3-25>BS4-2 | Data1 | ROUT1 > DIN0 |
| BS3>BS4 | Installed | BS3-24>BS4-3 | Data2 | ROUT2 > DIN0 |
| BS3>BS4 | Installed | BS3-23>BS4-4 | Data3 | ROUT3 > DIN0 |
| BS3>BS4 | Installed | BS3-22>BS4-5 | Data4 | ROUT4 > DIN0 |
| BS3>BS4 | Installed | BS3-21>BS4-6 | Data5 | ROUT5 > DIN0 |
| BS3>BS4 | Installed | BS3-20>BS4-7 | Data6 | ROUT6 > DIN0 |
| BS3>BS4 | Installed | BS3-19>BS4-8 | Data7 | ROUT7 > DIN0 |
| BS3>BS4 | Installed | BS3-18>BS4-9 | Data8 | ROUT8 > DIN0 |
| BS3>BS4 | Installed | BS3-17>BS4-10 | Data9 | ROUT9 > DIN0 |
| BS3>BS4 | OFF | BS3-16>BS4-11 | Lock | Deserializer LOCK test point |
| BS3>BS4 | Installed | BS3-15>BS4-12 | Clock | ROUT0 > DIN0 |
| BS3>BS4 | OFF | BS3-14>BS4-13 | Ground | Ground |

**Table 1- Jumpers Installation Table**

**Power Connections**

The B LINK EVM can be powered from an ordinary DC laboratory bench power supply through the assist of a pair of power supply cables with standard plug banana jacks.

- Set the power supply at 3.3 Vdc +/- 10%
- It is recommended that before making the power supply connections, the power supply be turned off
- Apply 3.3 volt jumper plug to EVM connector J6
- Apply Ground connection to EVM connector J7
- Application of power is indicated by an LED between the terminal posts.

It is advisable to maintain the power supply off until all SMA connections are made to preclude accidental shorting of coaxial connectors with power jacks.

**Basic Evaluation Setup**

As shipped, the board is ready for operation. Jumpers interconnecting BS3 and BS4 have been installed, which connect the parallel output bus from the Deserializer to the parallel input bus on the Serializer. Jumpers J11-J14 provide digital and analog power to both devices. The board is configured to be in the active powered state with all data outputs enabled, and jumpers installed for selecting the rising edge of the strobe clock . Once interconnected with test equipments as shown in Figure 4, the board is ready for power application and evaluation.

The basic setup takes serial data applied through a serial BERT at the J1-J2 SMA connectors (or alternately RJ45 connector at J6)[1]; data and clock , recovered at the Deserializer device, are output on the BS3 header. Jumpers interconnecting BS3 and BS4 provide parallel data and clock to the Serializer device, where data will is serialized and output at J3-J4 SMA connectors.

An optional jumper wire, interconnecting the Deserializer's LOCK output available at BS3-12 to pin 2 on JP8 or JP9 might be used to activate the rapid sync pattern generation option in the Serializer, the LOCK signal will go active low indicating that the Deserializer has locked onto the input data stream and command the Serializer to resume with normal data transmission.

Care should be taken to use matched electrical length cables for matched pair signals from and to a BERT or Scope to ensure the quality of measurements.

This setup can be used to verify the functional integrity and operation of the devices, evaluate lock time, jitter transfer and most timing parameters. The setup can with little modification be converted to effect other jitter evaluation and timing measurements for both serializer and deserializer devices.

[1] Zero Ohm steering resistors installed R2, R4, R19 and R21 steer data to SMA connectors while moving these resistors to R1, R2, R19&R20 makes serial data available at RJ45 connectors. Installing shorting bars in all resistor positions will make the signal available at both; however reflections may occur on serial data streams due to stub effects.

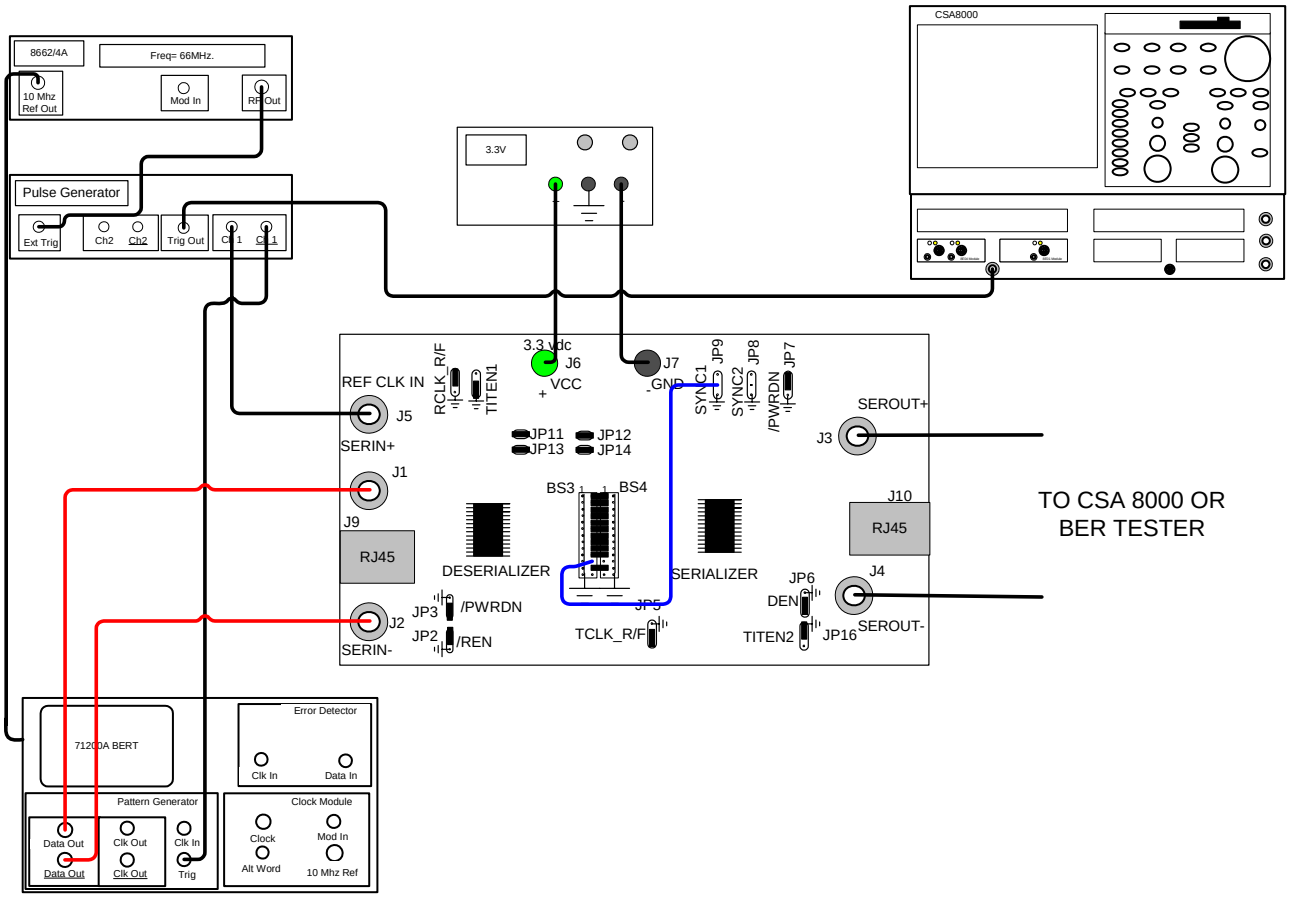



**Figure 4 - Basic Evaluation Setup**

**Optional Configurations and Measurements**

The fact that each of the devices operational pins are accessible at test pins or connectors facilitates the evaluation of each device as stand alone unit under test to evaluate other devise parameters such as setup, hold, Lock time etc. without influence from the other device.

**Parallel Input and Output Data**

The jumpers that interconnect the parallel busses of Deserializer and Serializer devices in the "as shipped configuration" are removed. Parallel data inputs to the Serializer device are provided at the BS4 header by an external parallel data generator. Data is serialized by the Serializer device and externally directed to the Deserializer inputs through SMA or RJ45 connections. The verification loop is completed by monitoring the parallel output of the Serializer at the BS3 header through a pattern verification unit that compares sent and received data.

- Jumpers that connect BS3 to BS4 are removed.
- BS4 parallel input data to the Serializer connected to a parallel pattern generator,
- BS3 Parallel outputs are connected to A parallel pattern verification unit, Set-up /Hold Setup
- Loopback of serial ports is effected by connecting J3-J1 and J4-J2 through matched length 50 Ohm cables.[2]

[2] Optionally J10 can loop the serial stream to J9 RJ45 connectors through the use of a standard Ethernet 10/100BASE-TX NIC-to-Hub cable

**Serializer Jitter Measurements**

Patterns can be introduced in several ways to provide input to the serializer.

- In the EVM's default configuration setup, a serial data stream can be provided to create these patterns.
- If all the jumper interconnecting the BS3 BS4 headers are removed data and clock can be provided at BS4.
- An alternate method of generating fixed patterns when a Parallel data generation capability is not available is to utilize jumpers from the data input connection to the adjacent ground posts on the BS4 Header. Since all data inputs to the serializer are pulled-up, only those bits where a jumper is installed to the adjacent ground become zero.

**Average Current Measurements**

Power is individually steered to Serializer and Deserializer devices by installed Jumpers JP11-JP14 as described in Table 1. In order to make individual device current measurements , jumpers could be replaced with current probes or replaced with a small value resistors to facilitate the current calculation. These jumpers are located on top of the board immediately below the power connectors to the EVM. Once jumpers are replaced with current measurement replacements, appropriate data patterns and speed selection need to be provided to validate those measurements.

## PC Board Physical Layout Recommendations

Serializer and De-Serializer devices should be provided with separate analog and digital power planes; these can co-exist within the same PWB layer and share a common ground where the analog and digital ground pins of each device may be joined.

In order to provide good power supply bypass and provide for the demand currents whose harmonics may reach into the many gigahertz region an appropriate power distribution system should be designed consisted of tantalum capacitors, high quality local capacitors should be placed in the immediate vicinity of power pins. Good interplane capacitance should be provided on this system utilizing power cores 0.005 inches or less.

All active signals should be laid out as 50 ohm characteristic impedance traces utilizing high speed layout techniques.

Serial data pairs should be electrically matched to within .050 inches, and laid out to provide 100 Ohm differential common mode impedance. A 100 Ohm termination resistor should be placed as close as to the sourcing pins on the serializer and to the receiving pins of the deserializer devices.

Figure 7 provides a graphical representation of the layout requirements for these devices.

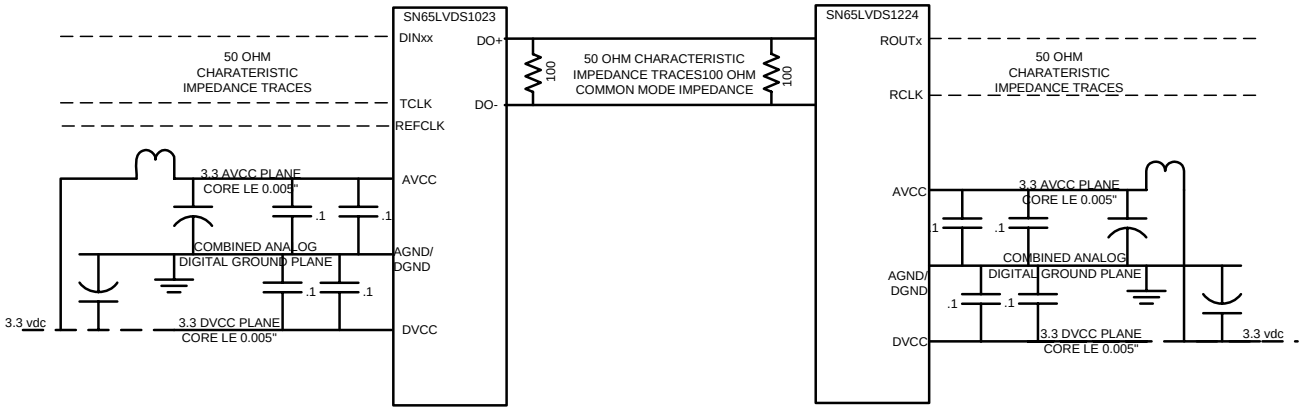
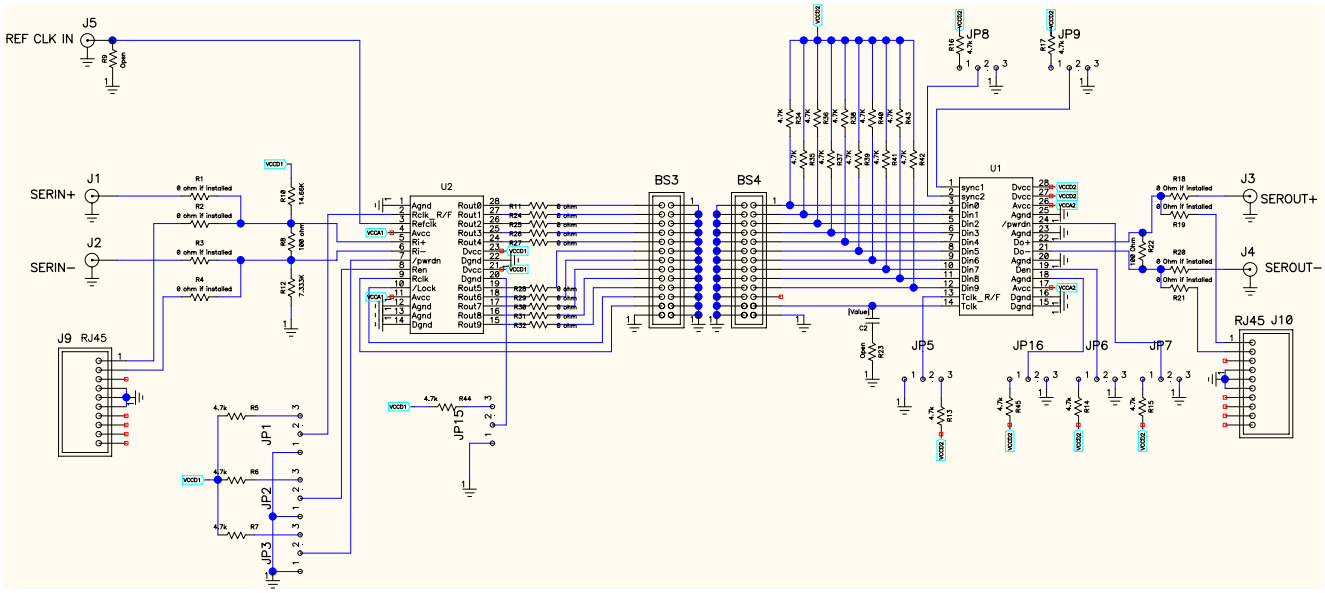
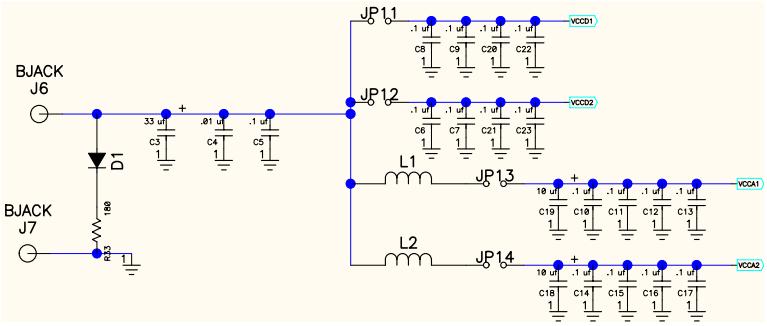



**Figure 7 - SN65LVDS1023/SN65LVDS1224 Layout Requirements Diagram at a Glance**

Appendix A

## BLINK Schematics



**Appendix B**

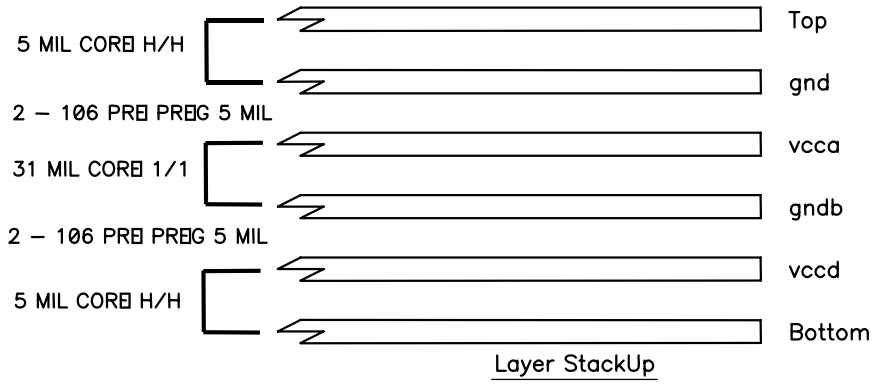
**EVM Board Design Stackup**

General Notes:

1 All Fabrication Items must meet or exceed best industry practice.
2 Laminate Material, copper clad GETEK, $E_r$ 3.9
3 Copper weight: 1 oz
4 Finished board thickness 0.060"+/-0.005"
5 Position Accuracy: +/- 0.0015"
6 Warp & Twist not to exceed 0.020"
7 Controlled impedance layer 1: 50 Ohm+/-5%
8 Controlled impedance trace width: 8.6 mils

Process Notes

1 Copper plating to be 0.001"minimum in plated through holes
2 Circuitry on outer layers to be plated with 7-12 uin gold over 50-80 uin nickel
3 Soldermask both sides: green enthoine
4 Apply white silkscreen on top and bottom side of board using separate artwork

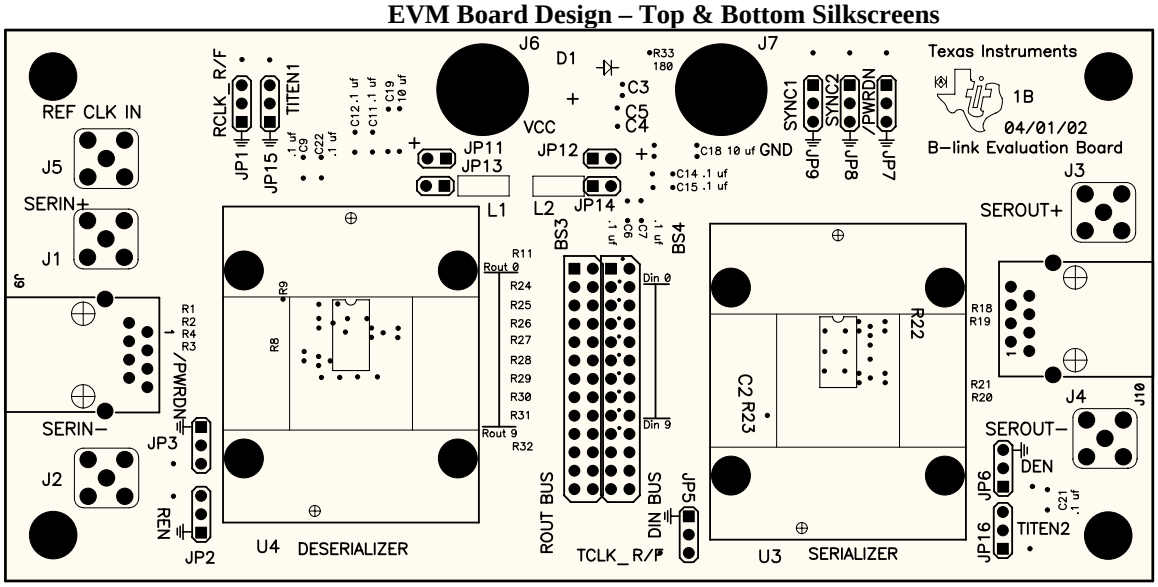


Layer StackUp

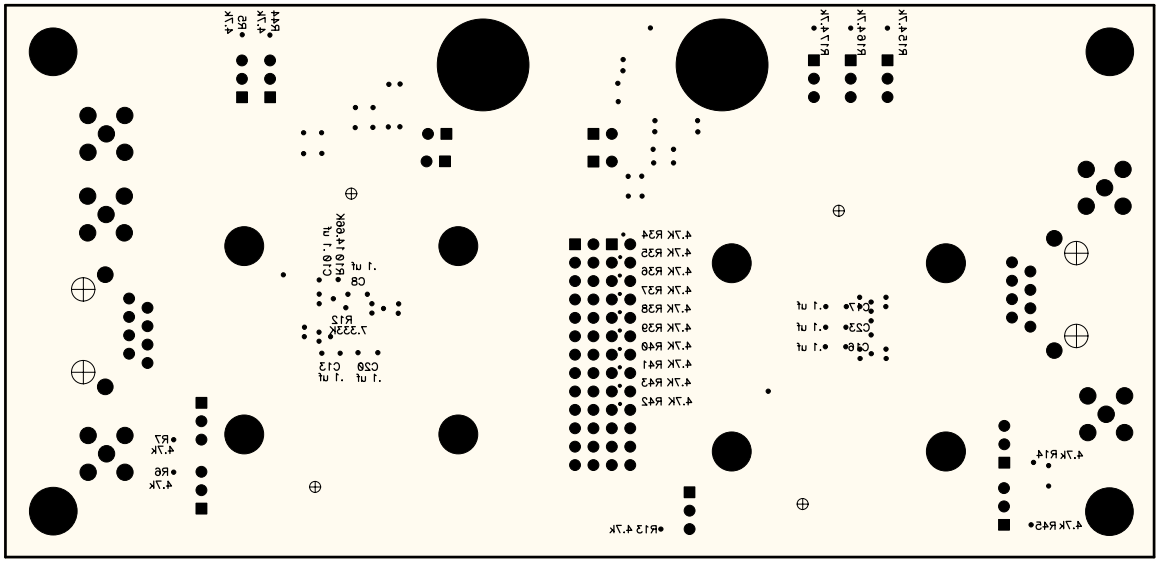
1 Top layer(Layer 1) 50Ohm trace using GETEK, 5 mil thick ½ oz copper. W1=10 mil, w=9.5 mil
2 Trace calculations contained in this drawing are solely for design purposes to establish a starting point for board requirements.
3 Board shop may adjust trace width to account for process and maintain controlled impedance where required

**Appendix B (contd)**

**EVM Board Design – Top & Bottom Silkscreens**



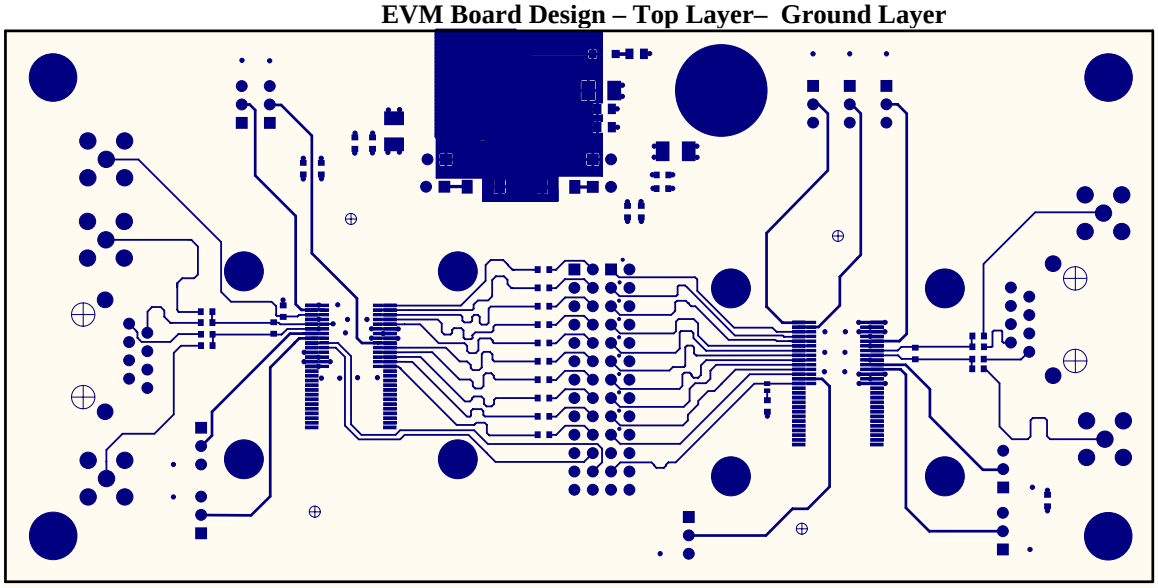

Top Silkscreen



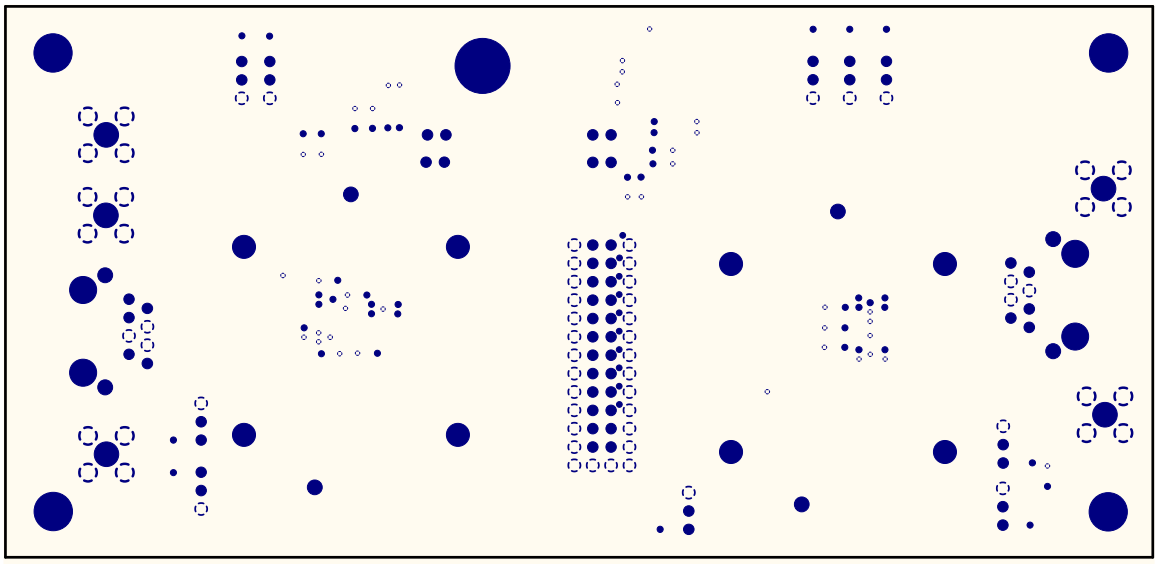
Bottom Silkscreen

**Appendix B (contd)**

**EVM Board Design – Top Layer– Ground Layer**



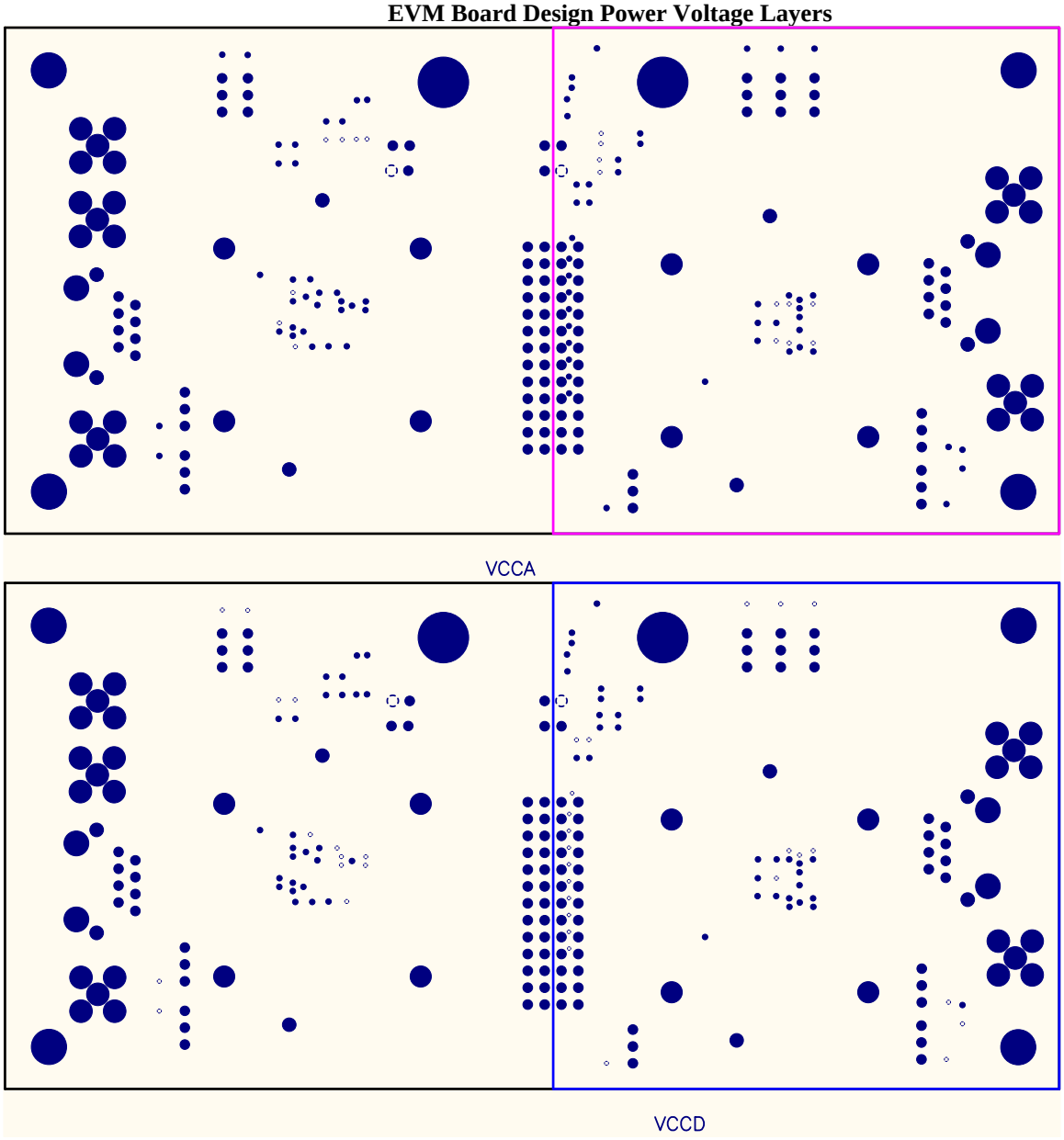
Top



GndB

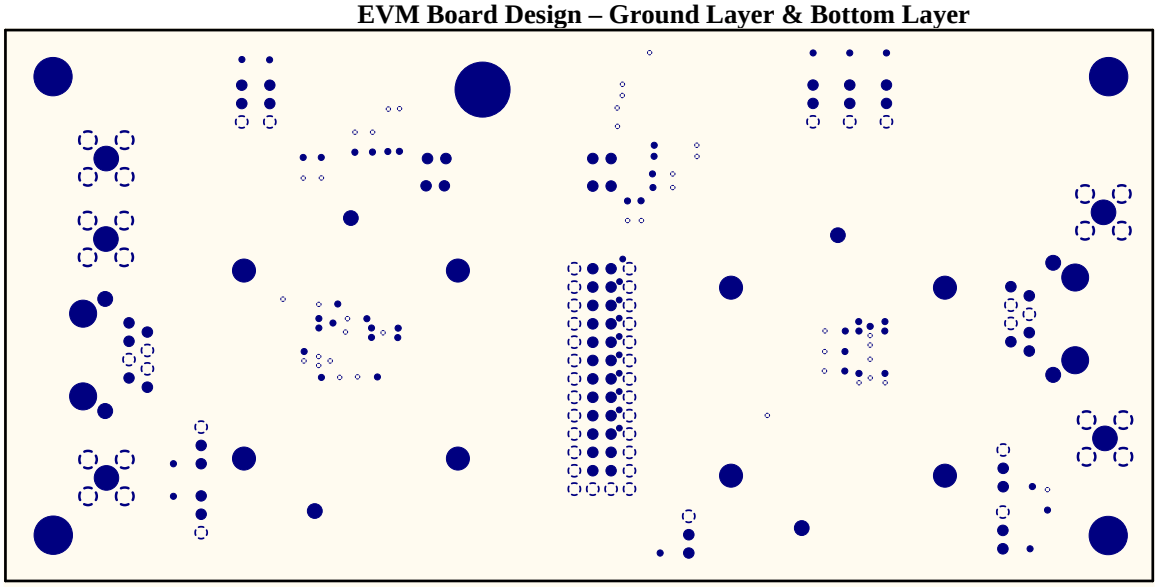
**Appendix B (contd)**

**EVM Board Design Power Voltage Layers**

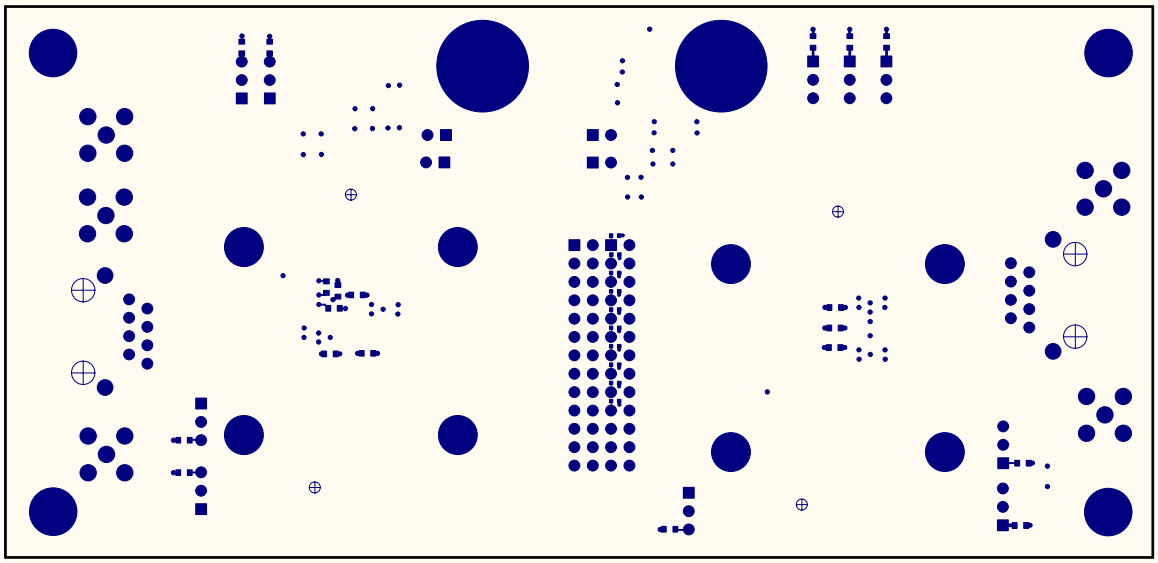


**Appendix B (contd)**

**EVM Board Design – Ground Layer & Bottom Layer**



Gnd



Bottom

**Appendix C-**

**BLINK EVM BOM**

| Count | Component Name | RefDes | Value | Description |
|---|---|---|---|---|
| 2 | BERG13 | BS3, BS4 | | DIN BUS & ROUT BUS 26 pin Headers |
| 2 | C1210+ | C18-C19 | 10 uf | |
| 1 | C0402 | C2 | | Not Installed |
| 1 | C1210+ | C3 | 33 uf | |
| 1 | C0805 | C4 | 0.01 uf | |
| 1 | C0805 | C5 | 0.1 uf | |
| 16 | C0603 | C6-C23 | 0.1 uf | 0603 Ceramic capacitor, |
| 1 | DigiKey 160-1174-2-ND | D1 | | Diode, Light Emitting |
| 5 | SMA TOP | J1, J2, J3, J4, J5 | | SMA HIGH SPEED MALE CONNECTOR |
| 2 | BJACK | J6- J7 | | Power Jacks |
| 2 | RJ45 | J9, J10 | | |
| 2 | JUMPER3 | JP1,JP2, JP5-JP9, JP15, JP16 | | 3-Pin 0.1”x 0.025” Male Header Material |
| 4 | JUMPER2 | JP11-JP14 | | 2- Pin 0.1”x 0.025” Male Header Material |
| 2 | DigiKey HI1806T600R-00 | L1-L2 | | Inductor, 1806 |
| 1 | R0603 | R10 | 14.66K | |
| 10 | R0603 | R11, R24-R32 | 0.0 | Resistor, SMD 0603 |
| 1 | R0603 | R12 | 7.333K | |
| 4 | R0603 | R1-R4, R18-R21 | 0 Ohm | Resistor, SMD 0603 (*Installation Specific, Signal Steering Requirements) |
| 1 | R0805 | R33 | 180 | |
| 10 | R0402 | R34-R43 | 4.7K | Resistor, SMD 0402 |
| 10 | R603 | R5-R7, R13-R17, R44, R45 | | |
| 2 | R0603 | R8, R22 | 100 | |
| 2 | R0603 | R9, R23 | | No Resistors Installed |
| 2 | | U2 | | SOC-B66-05-04-0 U1 |
| 1 | SN65LV1021 OR SN65LV1023 | U3 | | SERIALIZER, SN65LVD1021 100-400MB operation. SN65LVD1023 400-660Mb Operation |
| 1 | SN65LV1212 OR SN65LV1224 | U4 | | DESERIALIZER. SN65LVD1212 100-400MB operation. SN65LVD1224 400-660Mb Operation |

*IF SMA Connectors are used for Serial data {R1=0, R3=0, R18=0, R20=0. Do not Install R2, R4, R19 & R21 } ***PREFERRED CONFIGURATION***

Else IF RJ45 Connectors are used for Serial data { Do not Install: R1, R3, R18 or R20 . Install 0 Ohm in: R2, R4, R19, R21 }

## EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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## REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

**General Statement for EVMs including a radio**

*User Power/Frequency Use Obligations*: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

**For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant**

**Caution**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

**FCC Interference Statement for Class B EVM devices**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

**For EVMs annotated as IC – INDUSTRY CANADA Compliant**

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**Concerning EVMs including radio transmitters**

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concerning EVMs including detachable antennas**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

**Concernant les EVMs avec appareils radio**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

## 【Important Notice for Users of EVMs for RF Products in Japan】

**This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan**

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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## EVALUATION BOARD/KIT/MODULE (EVM)
## WARNINGS, RESTRICTIONS AND DISCLAIMERS

**For Feasibility Evaluation Only, in Laboratory/Development Environments.** Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

**Certain Instructions**. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

**Agreement to Defend, Indemnify and Hold Harmless.** You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

**Safety-Critical or Life-Critical Applications.** If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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