Application Note

Avoid Common Mistakes When Selecting And Designing With Power MOSFETs

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ABSTRACT

Power MOSFETs are used in a wide variety of applications from switch-mode power supplies to e-bikes and audio amplifiers. The high current carrying capability, ease of driving and fast switching characteristics makes power MOSFETs an essential tool in the design engineers toolbox. When selecting a power MOSFET for an application, a thorough review of the application requirements and the FET data sheet can help avoid some common mistakes.

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1 Introduction

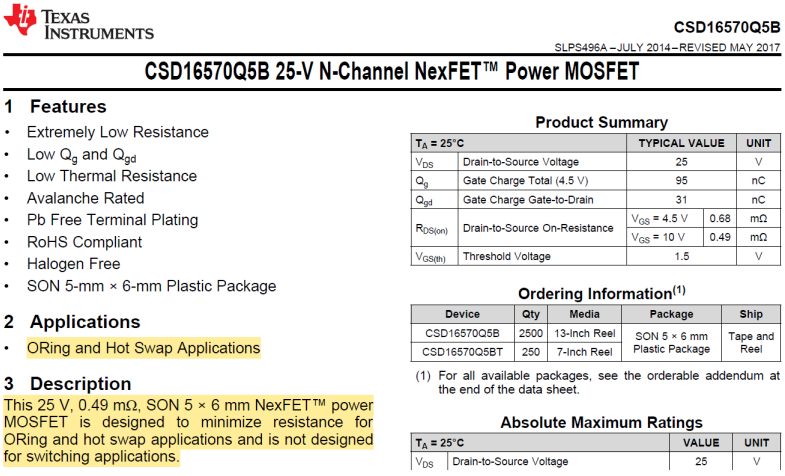
To assist the designer, TI has published a series of technical articles, application notes and tools for selecting and using MOSFETs: MOSFET Support and Training Tools application note. Once the FET has been chosen, there is more work to do to make sure the FET works as expected in the application.

2 Review the Data Sheet Limits

During FET selection, a review of the application and the data sheet is necessary to make sure the device is operating within the data sheet limits. This is especially true for the absolute maximum ratings which define the electrical and thermal limitations of the device. Exceeding the absolute maximum ratings can result in catastrophic failure of the FET. Most engineers derate from the limits in the data sheet to make sure there is enough margin in the design for unexpected events such as voltage spikes, transients, fault conditions, overloads, short circuits and etc. For example, a FET with abs max V_{DS} = 30V is typically derated to 24V maximum operating voltage.

3 Application-specific FETs

Some FETs are optimized for switch-mode applications while others are better suited for static switching. Some can work in either application type. The first thing to do is review the FET data sheet. On page 1, TI FET data sheets include information on applications the FET is optimized for. For example, Figure 3-1 shows the CSD16570Q5B data sheet and this FET is optimized for ORing and hot swap applications.



TEXAS INSTRUMENTS

CSD16570Q5B

SLPS496A – JULY 2014 – REVISED MAY 2017

CSD16570Q5B 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Extremely Low Resistance
- Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

2 Applications

- ORing and Hot Swap Applications

3 Description

This 25 V, 0.49 mΩ, SON 5 × 6 mm NexFET™ power MOSFET is designed to minimize resistance for ORing and hot swap applications and is not designed for switching applications.

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	95		nC
Q_{gd}	Gate Charge Gate-to-Drain	31		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	0.68	mΩ
		V_{GS} = 10 V	0.49	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD16570Q5B	2500	13-Inch Reel	SON 5 × 6 mm Plastic Package	Tape and Reel
CSD16570Q5BT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V

Figure 3-1. CSD16570Q5B Data Sheet

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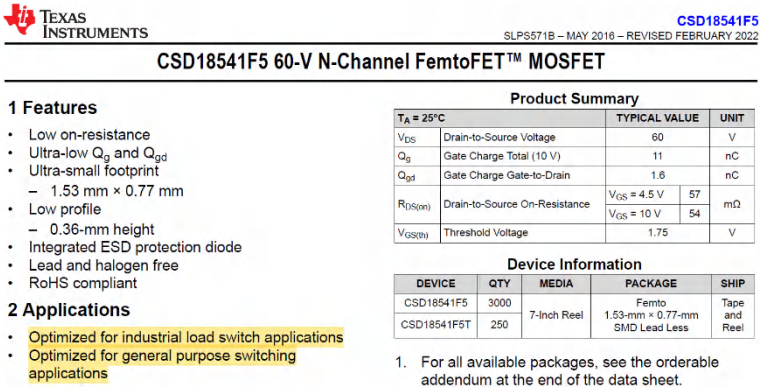
Likewise, Figure 3-2 shows an excerpt from the CSD18541F5 data sheet. This device is optimized for load switch and general purpose switching applications.



TEXAS INSTRUMENTS — CSD18541F5
SLPS571B – MAY 2016 – REVISED FEBRUARY 2022

CSD18541F5 60-V N-Channel FemtoFET™ MOSFET

1 Features

- Low on-resistance
- Ultra-low Q_g and Q_{gd}
- Ultra-small footprint
  - 1.53 mm × 0.77 mm
- Low profile
  - 0.36-mm height
- Integrated ESD protection diode
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for industrial load switch applications
- Optimized for general purpose switching applications

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	11		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.6		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	57	mΩ
		V_{GS} = 10 V	54	
$V_{GS(th)}$	Threshold Voltage	1.75		V

Device Information

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18541F5	3000	7-Inch Reel	Femto 1.53-mm × 0.77-mm SMD Lead Less	Tape and Reel
CSD18541F5T	250			

1. For all available packages, see the orderable addendum at the end of the data sheet.

Figure 3-2. CSD18541F5 Data Sheet

Digging further into the data sheet dynamic characteristics, the CSD16570Q5B is not a good candidate for switch-mode applications as the charge ratio, Q_{gd}/Q_{gs} > 1. This makes the MOSFET more susceptible to CdV/dt induced turn-on when used as the low side FET in a synchronous buck converter. Similarly, the CSD18541F5 has a charge ratio > 1, but the typical internal series gate resistance is R_G = 1200Ω. This limits the switching speed and this FET is not the best for switch-mode applications. If there are some questions whether a FET can be used in a particular application, then review the *Applications* section and *Dynamic Characteristics* section in the data sheet. If there are further questions, then contact your FET vendor for more information.

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4 Gate Drive Voltage Specifications

A common mistake is driving the FET gate at the incorrect voltage. Often V_{GS} is too low to achieve $R_{DS(on)}$ specified in the data sheet. More information on this topic is described later in the document.

Multiple specifications for V_{GS} are included in the FET data sheet. There is a specification for absolute maximum V_{GS}, a specification for gate-to-source threshold voltage, $V_{GS(th)}$, and a specification for $R_{DS(on)}$ at one or more values of V_{GS}. The next section reviews each of these items and how the specifications are used when selecting a FET.

4.1 Absolute maximum V_{GS}

The absolute maximum V_{GS} rating can be a single value or separate positive and negative values depending on the gate structure. As detailed in the What type of ESD protection does your MOSFET include? technical article, TI FETs can have single-ended, back-to-back or no gate ESD protection. FETs with a single-ended ESD structure only have a single value for absolute maximum V_{GS}. Applying a voltage of the opposite polarity forward biases the gate-to-source ESD diode allowing current to flow into the gate and clamping V_{GS} at a junction drop. An external gate resistor can be added to limit the gate current and prevent damaging the FET.

Devices with back-to-back or no ESD protection have separate positive and negative absolute maximum V_{GS} values that can be symmetric (that is, ±20V) or asymmetric (that is, -12V/+16V). Never operate the FET with V_{GS} in excess of the absolute maximum specifications or the FET can be damaged.

Table 4-1, Table 4-2, and Table 4-3 show examples of the absolute maximum ratings for the following TI N-channel MOSFETs:

Table 4-1. CSD17581Q5A Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-source voltage	30	V
V_{GS}	Gate-to-source voltage	±20	V
I_D	Continuous drain current (package limited)	60	A
	Continuous drain current (silicon limited), T_C = 25°C	123	
	Continuous drain current	24	
I_{DM}	Pulsed drain current	256	A
P_D	Power dissipation	3.1	W
	Power dissipation, T_C = 25°C	83	
T_J, T_{stg}	Operating junction temperature and storage temperature	–55 to 150	°C
E_{AS}	Avalanche energy, single pulse I_D = 39A, L = 0.1 mH, R_G = 25Ω	76	mJ

Table 4-2. CSD17381F4 Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-source voltage	30	V
V_{GS}	Gate-to-source voltage	12	V
I_D	Continuous drain current, T_A = 25°C	3.1	A
I_{DM}	Pulsed Drain Current, T_A = 25°C	12	A
I_G	Continuous gate clamp current	35	mA
	Pulsed gate clamp current	350	
P_D	Power dissipation	500	mW
ESD Rating	Human body model (HBM)	4	kV
	Charged device model (CDM)	2	kV
T_J, T_{stg}	Operating junction and storage temperature range	–55 to 150	°C
E_{AS}	Avalanche energy, single pulse I_D = 7.4A, L = 0.1mH, R_G = 25Ω	2.7	mJ

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Table 4-3. CSD16415Q5 Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-source voltage	25	V
V_{GS}	Gate-to-source voltage	–12 to 16	V
I_D	Continuous drain current (package limited)	100	A
	Continuous drain current (silicon limited), T_C = 25°C	261	
	Continuous drain current	38	
I_{DM}	Pulsed drain current, T_A = 25°C	200	A
P_D	Power dissipation	3.2	W
	Power dissipation, T_C = 25°C	156	
T_J, T_{stg}	Operating junction temperature and storage temperature	–55 to 150	°C
E_{AS}	Avalanche energy, single-pulse I_D = 100A, L = 0.1mH, R_G = 25Ω	500	mJ

4.2 Gate-to-source Threshold Voltage, $V_{GS(th)}$

The gate-to-source threshold voltage, $V_{GS(th)}$ is specified at I_D = 250µA in TI FET data sheets. This is where the FET just begins to conduct current and is lower than the minimum V_{GS} where $R_{DS(on)}$ is specified in the data sheet. For example, as shown in Table 4-4, typical $V_{GS(th)}$ = 1.75V for the CSD18541F5 60V N-channel FET but the minimum V_{GS} = 4.5V where $R_{DS(on)}$ is specified in the data sheet.

Table 4-4. CSD18541F5 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_{DS} = 250µA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 48V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V			10	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250µA	1.4	1.75	2.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5V, I_{DS} = 1A		57	75	mΩ
		V_{GS} = 10V, I_{DS} = 1A		54	65	
g_{fs}	Transconductance	V_{DS} = 6V, I_{DS} = 1A		7.7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		598	777	pF
C_{oss}	Output capacitance			47	61	pF
C_{rss}	Reverse transfer capacitance			8.1	10.5	pF
R_G	Series gate resistance			1200	1600	Ω
Q_g	Gate charge total (10V)	V_{DS} = 30V, I_{DS} = 1A		11	14	nC
Q_{gd}	Gate charge gate-to-drain			1.6		nC
Q_{gs}	Gate charge gate-to-source			1.5		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.8		nC
Q_{oss}	Output charge	V_{DS} = 30V, V_{GS} = 0V		3.2		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 30V, V_{GS} = 4.5V, I_{DS} = 1A, R_G = 0Ω		572		ns
t_r	Rise time			540		ns
$t_{d(off)}$	Turnoff delay time			1076		ns
t_f	Fall time			496		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 1A, V_{GS} = 0V		0.8	1	V

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A common mistake is assuming as long as $V_{GS} \geq V_{GS(th)}$, the FET is on and operates as intended in the application. This is not always the case. To ensure $R_{DS(on)}$ meets the data sheet limits, V_{GS} must always be greater than or equal to the minimum value where $R_{DS(on)}$ is specified in the data sheet. This is often overlooked and can cause unexpected problems in the application. A customer using the CSD18541F5 had to change the design because the application used V_{GS} = 3.3V instead of V_{GS} = 4.5V. As shown in Figure 4-1, operating the CSD18541F5 with V_{GS} < 4.5V, the slope of the curve is almost vertical and small changes in $V_{GS(th)}$ can result in exponential changes in $R_{DS(on)}$.

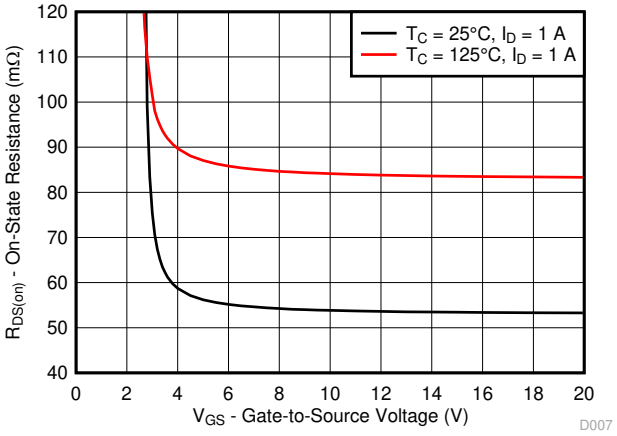

Figure 4-1. CSD18541F5 $R_{DS(on)}$ vs. V_{GS}

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5 High-side and Low-side Switches

Power MOSFETs are used as both high-side and low-side switches. What is the difference and how is the gate driven? A high-side switch places the FET between the input supply and the load. A low-side switch places the FET between the load and ground. Simplified examples are shown in Figure 5-1 and Figure 5-2.

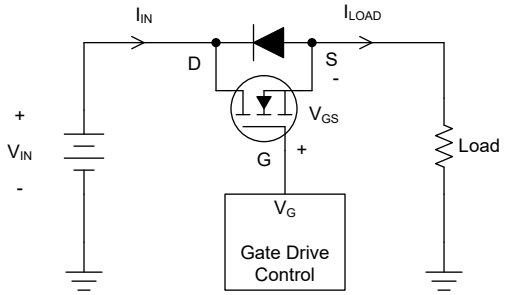

Figure 5-1. N-channel FET High Side Switch

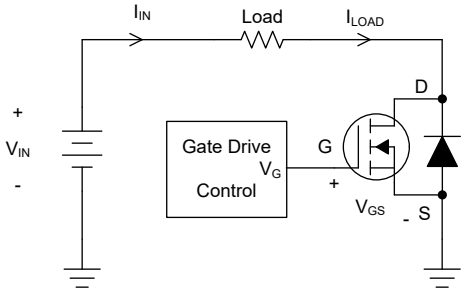

Figure 5-2. N-channel FET Low Side Switch

5.1 Driving a High-side N-channel FET

The gate of a high-side N-channel FET must to be driven to a voltage higher than the input by at least the minimum value of V_{GS} where $R_{DS(on)}$ is specified in the data sheet. This is because the drain and source are at approximately the same voltage when the FET is on and $V_{GS} = V_G – V_S = V_G – V_{IN}$. For example, when using the CSD18541F5 as a high switch with V_{IN} = 24V, $V_G \geq V_{IN} + V_{GS(min)}$ = 24V + 4.5V = 28.5V.

5.2 Driving a Low-side N-channel FET

Driving a low-side N-channel FET is much simpler since the source is grounded and the gate only needs to be driven to the minimum value of V_{GS} where $R_{DS(on)}$ is specified in the data sheet.

5.3 Driving a High-side P-channel FET

As shown in Figure 5-3, P-channel FETs are mainly used as high-side switches due to the simplicity of driving the gate. To turn the device on, the gate is pulled down to GND. To turn the device off, the gate is pulled up to V_{IN}. To avoid damaging the FET, always check the data sheet to make sure that the input voltage, $V_{IN} \leq$ abs max V_{GS}.

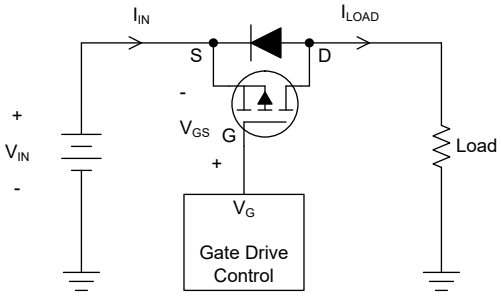

Figure 5-3. P-channel FET High Side Switch

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6 Use a Gate-to-source Resistor

A floating or open gate can be a recipe for FET failures. When the gate of the FET is left open, the gate can charge up to a voltage that unintentionally causes drain current, I_D, to flow. This can lead to unwanted behavior up to and including, catastrophic failure of the FET. As shown in Figure 6-1, adding a 10kΩ to 1MΩ resistor from gate-to-source is an easy way to make sure the FET is off if the gate is floating.

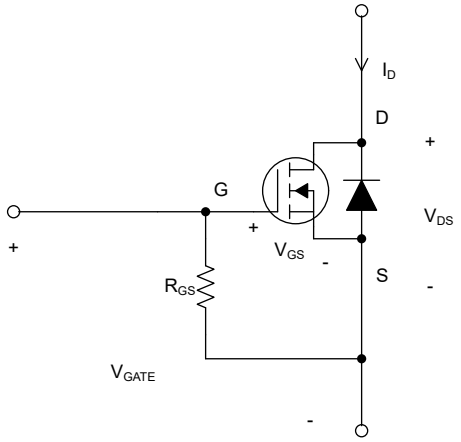

Figure 6-1. N-channel FET with Gate-to-source Resistor, R_{GS}

7 Lowest $R_{DS(on)}$≠ Lowest Power Loss

Does the MOSFET with the lowest $R_{DS(on)}$ result in the lowest power loss? This depends on the application and how the FET is being used. Conduction or I^2R loss is directly proportional to $R_{DS(on)}$ and, for those applications such as hot swap, load switch, and OR'ing, where the FET is not switching at 10s or 100s of kHz, the lowest on resistance device results in the lowest power loss.

In switch-mode applications such as DC-DC converters, switching loss can be a significant portion of the total MOSFET power loss. $R_{DS(on)}$ is a function of the FET die size and a larger die results in lower $R_{DS(on)}$ for a given MOSFET process technology and voltage rating. A larger die also has higher charge and capacitance, which results in increased switching loss. Selecting a FET for a switch-mode application must balance conduction loss and switching loss to achieve the lowest overall power loss in the FET.

TI has released a number of Excel-based FET selection tools for various applications that take this into account. For example, the synchronous buck FET selection tool allows the user to input the requirements and compare up to three different TI FET designs based on power loss, package and 1ku pricing.

8 Summary

Power MOSFETs are versatile devices that are used in a multitude of applications. This article presented some common mistakes to avoid when selecting and designing with FETs.

9 References

The following documents are further references to learn more about TI MOSFETs:

- Texas Instruments, *MOSFET Support and Training Tools*, application note
- Texas Instruments, *What type of ESD protection does your MOSFET include?*, technical article

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