Simple, high-performance, isolated power supply design with PSR (no-opto) flyback

Marshall Beck

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Agenda

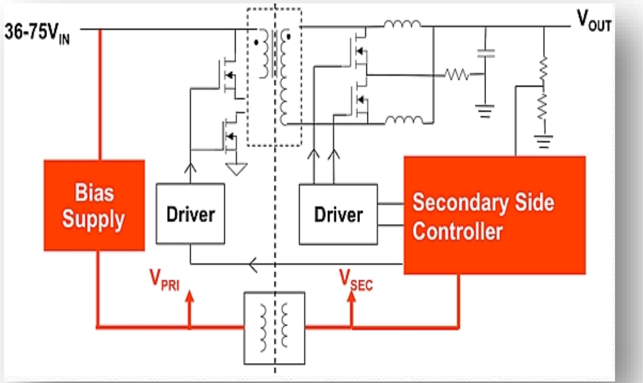
- Isolation in industrial applications
- PSR flyback:
  - PSR vs conventional flyback, control/operation, and TI offerings
- PSR flyback simple design flow
- TI supporting content on PSR flyback design

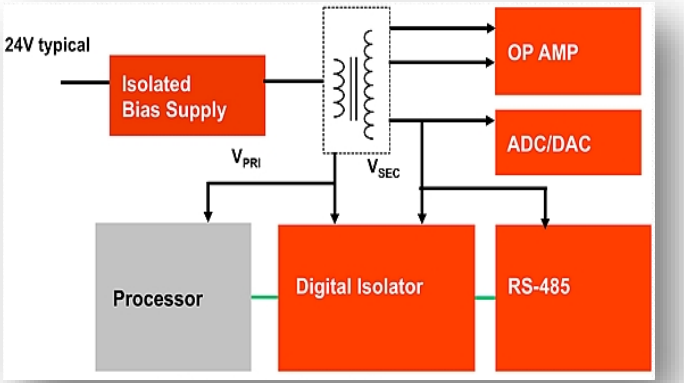
Industrial – Isolation everywhere

Wide V_{IN}
24 VDC (15-42V)
PoE (36-57V)

→ **Isolation** →

IP Phone
IP Surveillance
Sensors
PLC
E-Meter
Solar
Telecom

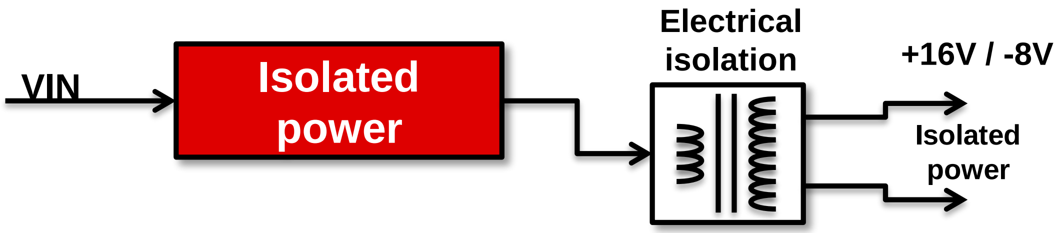




Where to use isolation?

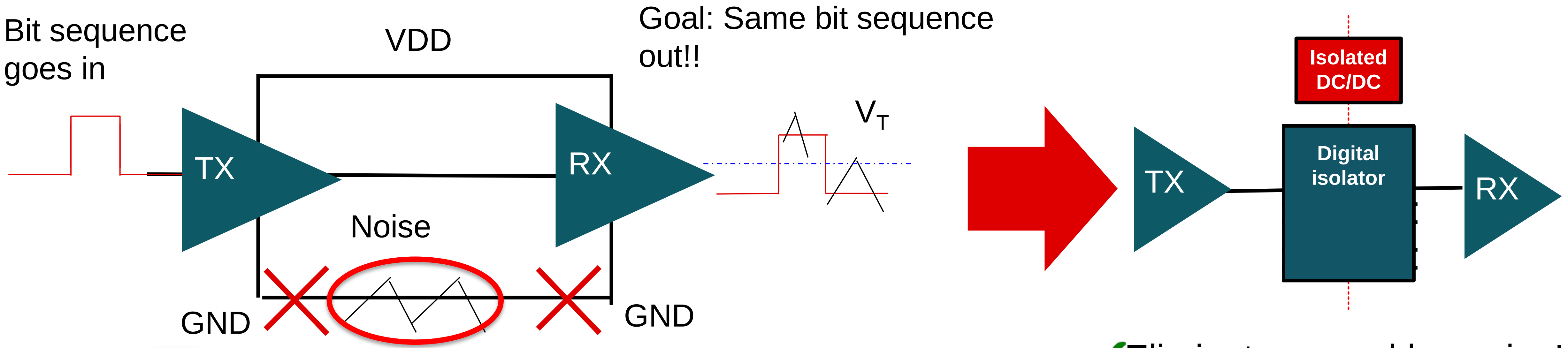
- **Safety**
  - Mandatory by safety standards to isolate the user from the hazardous voltage of a power supply. Protect user from ESD and surge events.
  - Typical applications: IP camera, solar inverter, factory automation – field site

- **Break ground loop, mitigate noise**
  - Installed to break the ground loop interference for noise-sensitive applications
  - Typical applications : PLCs, solar inverters, building automation (ie. RS232/485, etc.)
- **Inversion, level shifting & multiple rails**
  - Isolated output voltage can be conveniently configured as multiple isolated outputs, as a negative voltage rail or as a level-shifted voltage rail.
  - Typical applications : test and measurement, medical, e-bike, HVAC, motor drives



Isolated power – Simplify signal integrity!

- Typical communication protocols: **RS422/485, RS232, RS285, LVDS, Ethernet**
- Long cabling causes transient voltage differences and **possible errors!**
- **Solution: Isolate the TX and RX power!**



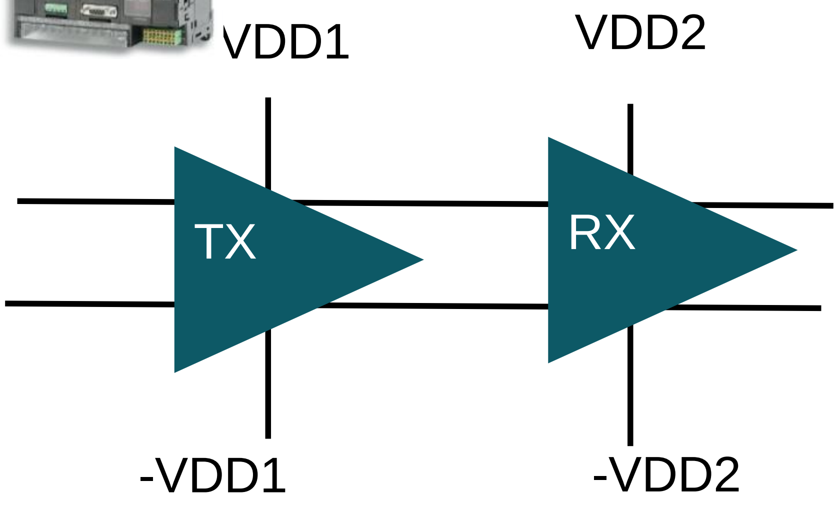
- ✗ Ground bouncing!
- ✗ Loose noise margin!
- ✗ Bit errors!

- ✓ Eliminate ground bouncing!
- ✓ Improved noise margin!
- ✓ Improved effective bit rate!

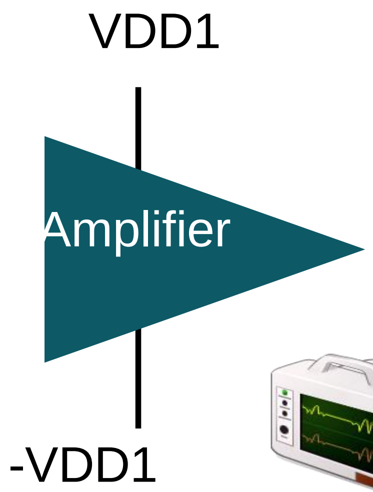
Isolated power – Simplify your power tree!

- Isolated output voltages can be conveniently configured as **multiple isolated outputs**, as a **negative voltage rail** or as a **level-shifted voltage rail**.
- **Example use cases**: Positive/negative rails for differential digital communications, op-amp, isolated bias supply for gate driver

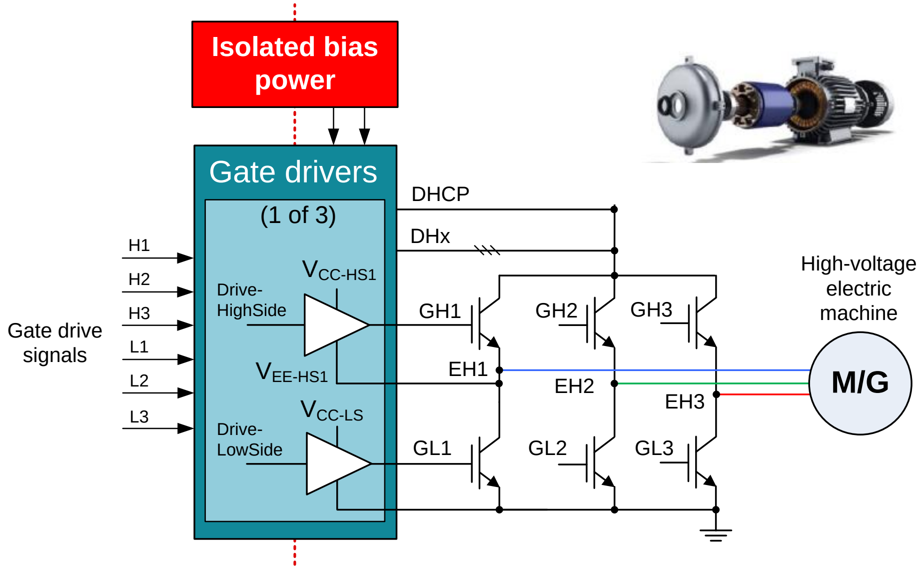
Differential RX/TX Power



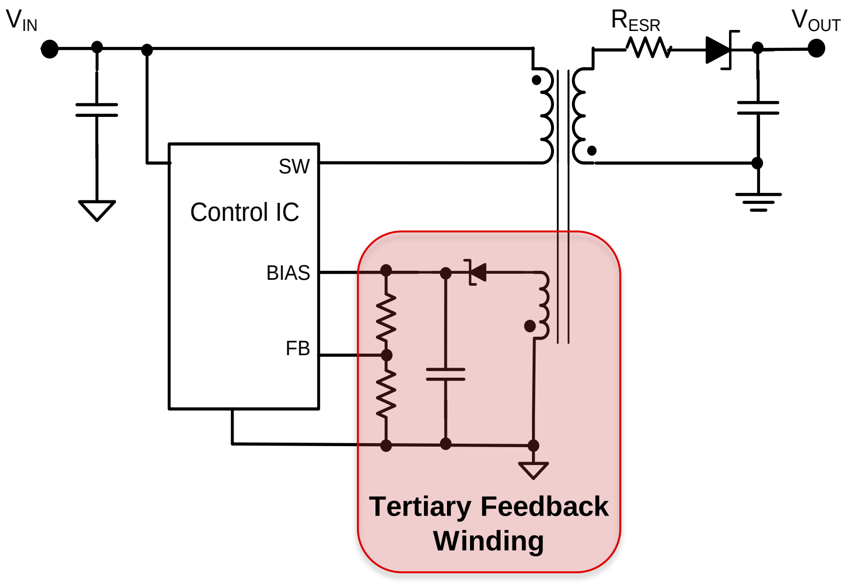
Signal conditioning (Op-amp, ADC/DAC)

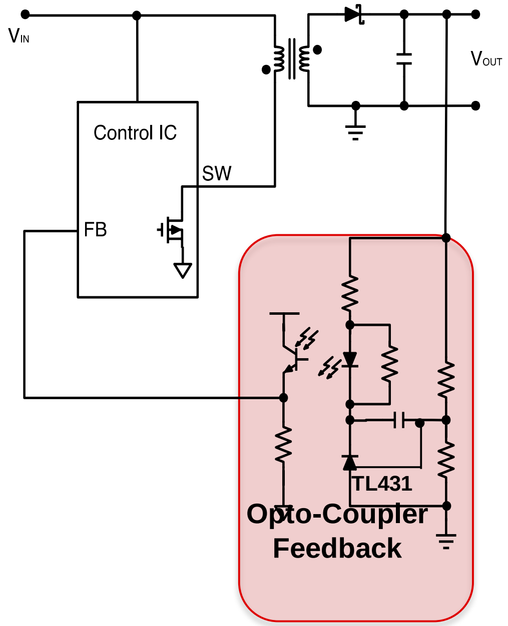


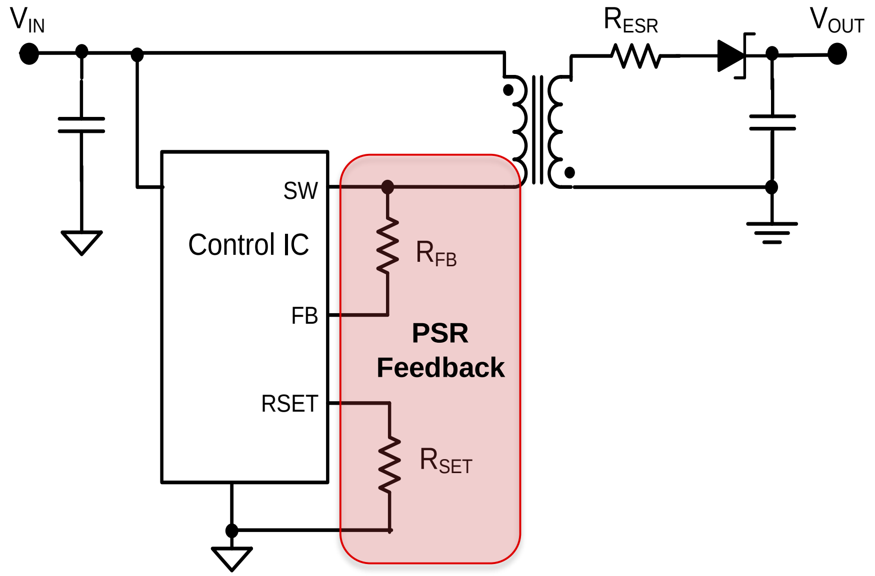
Isolated bias supply



Conventional PSR flyback vs. Aux-less PSR flyback







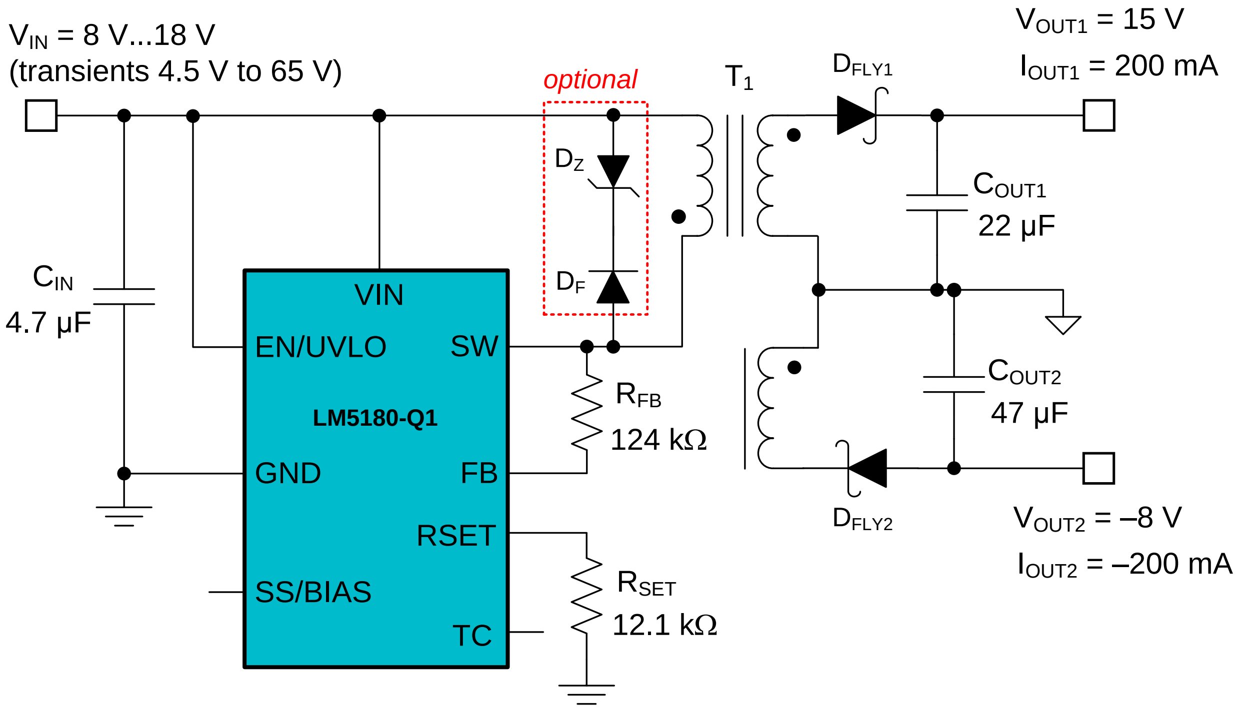
Conventional PSR flyback advantages:

- Increased design flexibility with external compensation and tertiary winding or opto-coupler feedback
- Operates in CCM (fixed frequency) or DCM mode

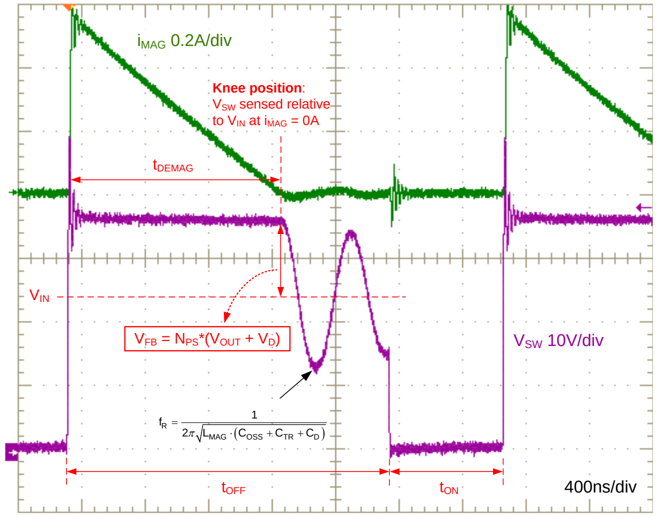
Aux-less PSR flyback advantages:

- Eliminates opto-coupler or tertiary winding with only one component crossing isolation barrier
- Extremely tight load regulation (±1%)
- Operates in DCM or Boundary Mode
- DCM and zero current switching enables high efficiency

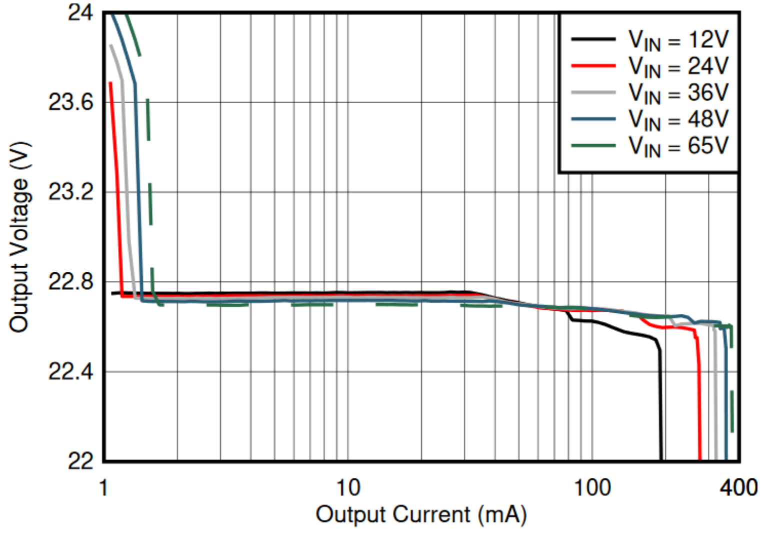
PSR flyback converter – no opto, no aux winding



PSR sensing – output voltage sampled using the primary-side SW voltage



Load regulation – sum of V_{OUT1} and V_{OUT2} with symmetrical loading



- No aux winding → easier magnetic design
- No optocoupler → higher temperature operation, longer lifetime
- Accurate output regulation → ideal for SiC gate drivers
- Leakage inductance tolerant → manage reinforced isolation creepage spacing

PSR flyback DC/DC family overview

PSR Flyback DC/DC Converter	Input Voltage Range	Peak Switch Current	Maximum Load Current V_{OUT} = 12 V, N_{PS} = 1, V_{IN} = 13.5V	Package Option
LM5181	4.5 V to 65 V	0.75 A	180 mA	WSON-8
LM5180	4.5 V to 65 V	1.5 A	360 mA	WSON-8
LM25180	4.5 V to 42 V	1.5 A	360 mA	WSON-8
LM25183	4.5 V to 42 V	2.5 A	600 mA	WSON-8
LM25184	4.5 V to 42 V	4.1 A	1 A	WSON-8

LM25183-Q1/LM25184-Q1

Highest power density 42V, 2.5A/4A primary side regulated (PSR) flyback converter with 65V integrated power MOSFET

AEC-Q100 Grade 1

Features

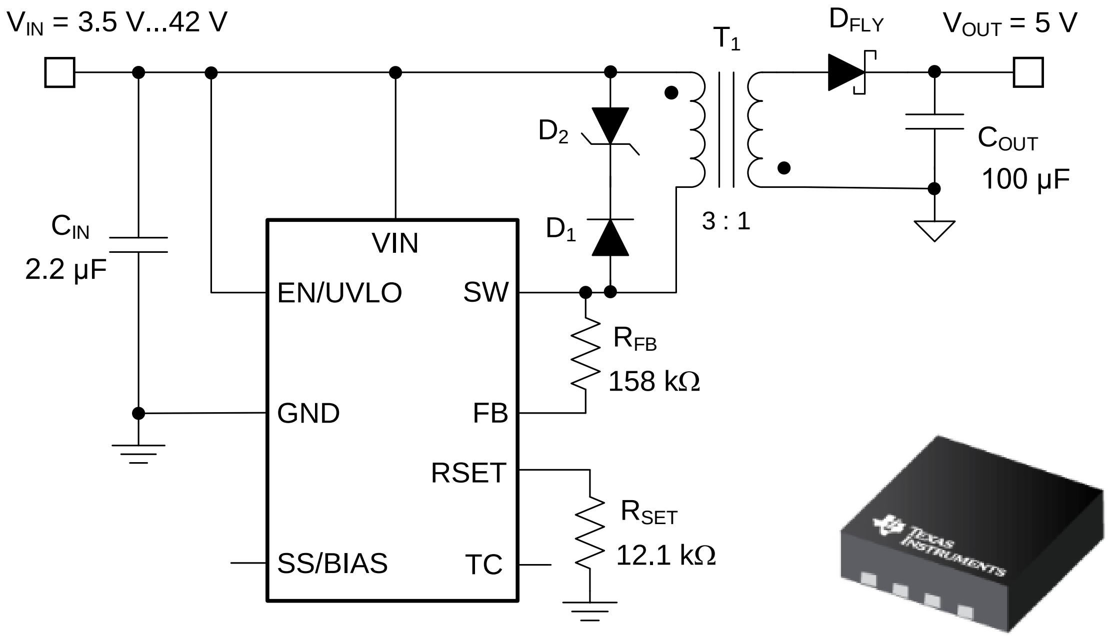
- Highest Power Density 42V PSR with tightest Output Regulation in its class
- **65V, 2.5A/4A internal power MOSFET**
- **4.5V–42V wide V_{IN} range** (abs max 45V)
  - 3.5V minimum V_{IN} after start-up
- **V_{OUT} accuracy ±1% achievable**
  - V_{IN} = 6V–42V, V_{OUT} = 5V, 2% load to full load
  - T_A = –40°C to 125°C
- **Boundary mode**, quasi-resonant operation
- Internal loop compensation, adjustable input UVLO
- External V_{CC} bias option for improved efficiency
- Adjustable or fixed internal 6ms soft-start
- Optional V_{OUT} temperature compensation
- **4 mm × 4 mm WSON-8** WF package, 0.8mm pitch
- **AEC-Q100 grade 1** ⇒ 125°C operating ambient range

Applications

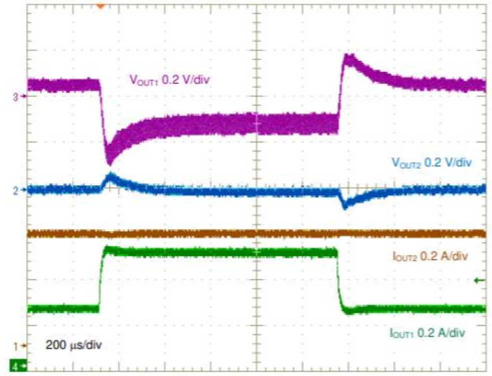
- **Factory automation, PLC**
- **Motor drive, telcom, solar, IP**

Benefits

- No opto-coupler or transformer auxiliary winding needed
- Accurate V_{OUT} regulation performance with sensing at zero current
- Low I_Q operation and external BIAS rail option enable high efficiency at light loads



LM25184 performance curves



V_{IN} = 24 V I_{OUT2} = 0.5 A

Figure 8-25. Positive Output Load Transient, 0.25 A to 0.5 A

Modest F_{SW} enables good transient performance and small magnetics

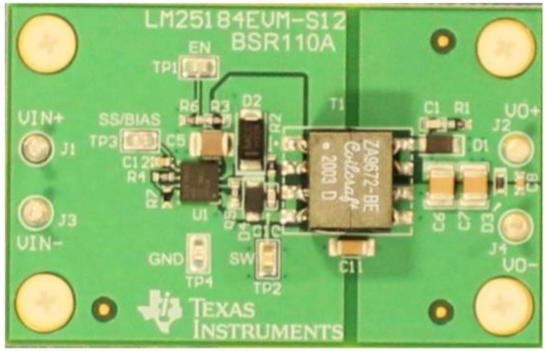
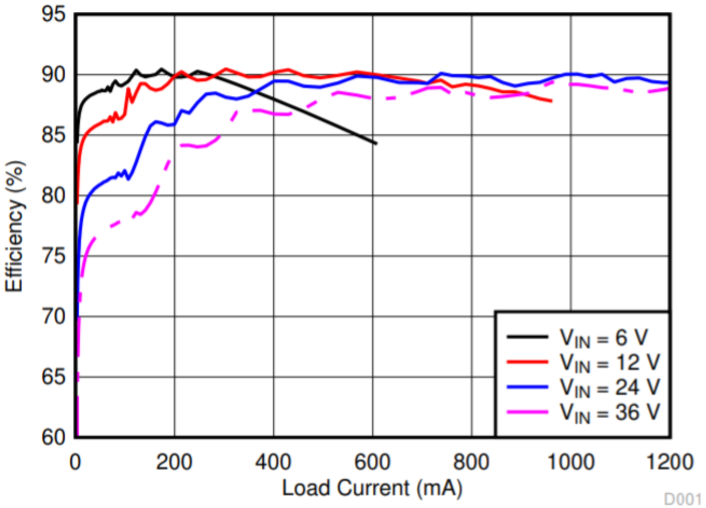
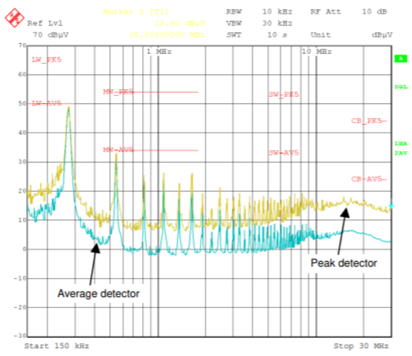


Figure 2. LM25184 EVM (Top Side), 56 mm × 36 mm

Low-heat generation

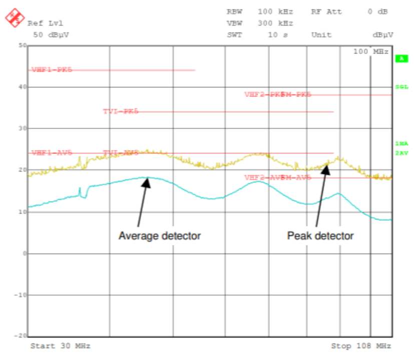


Typical Efficiency, V_{OUT} = 12 V



V_{IN} = 24 V 150 kHz to 30 MHz L_{IN} = 4.7 µH
I_{OUT} = 1 A C_{IN} = 10 µF

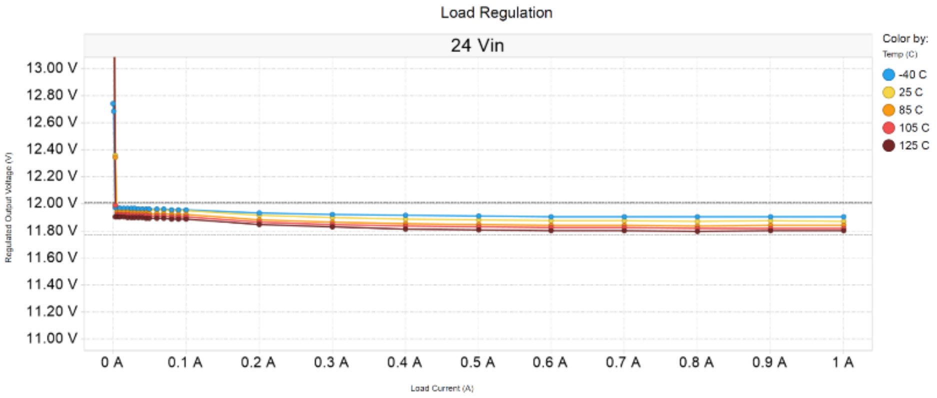
Figure 8-14. CISPR 25 Class 5 Conducted EMI Plot



V_{IN} = 24 V 30 MHz to 108 MHz L_{IN} = 4.7 µH
I_{OUT} = 1 A C_{IN} = 10 µF

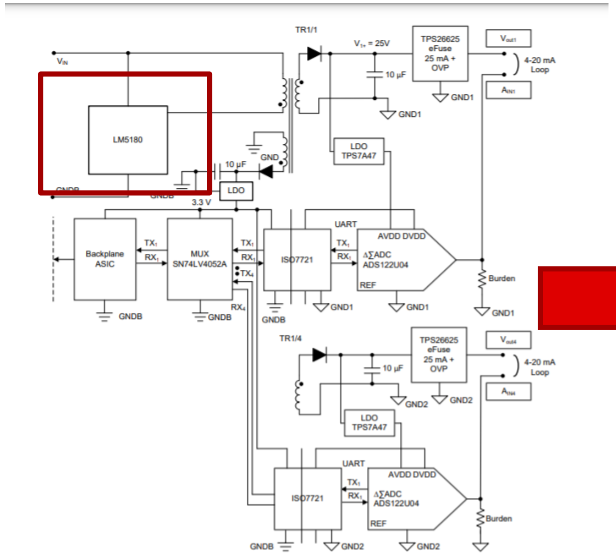
Figure 8-15. CISPR 25 Class 5 Conducted EMI Plot

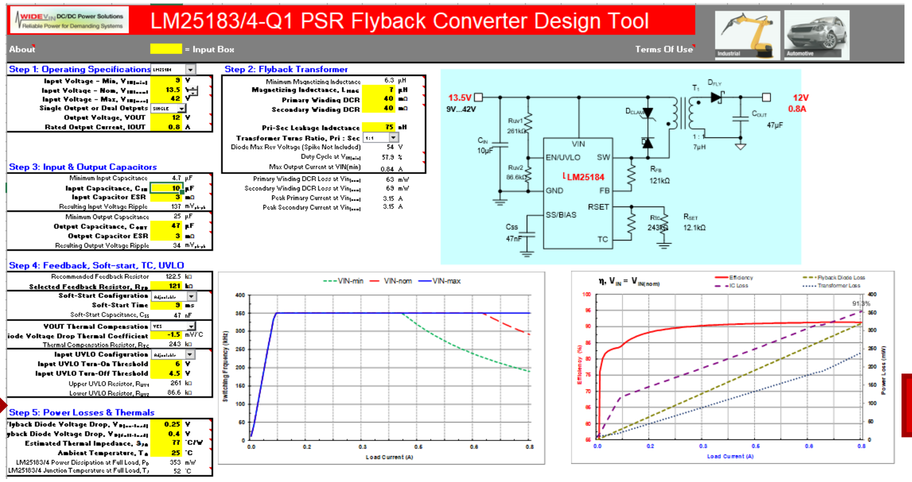
Passes stringent EMC standards with only differential filtering

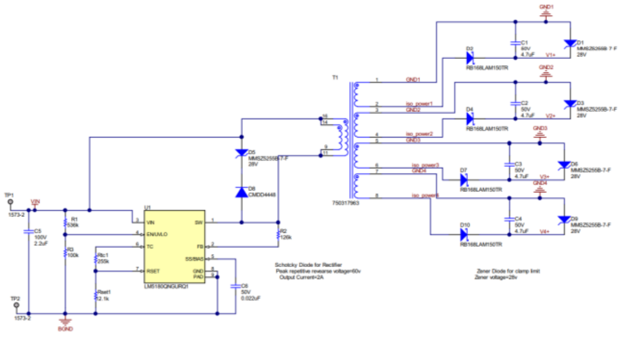


<1.7% variance from -40degC to 125degC

TI’s simple design flow

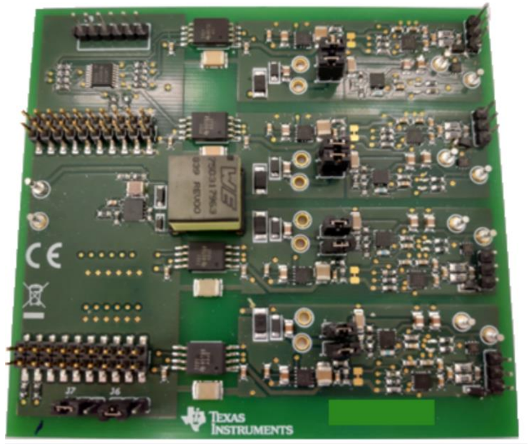






PSpice® for TI

webench® POWER DESIGNER



Design calculator tool

Input power conditions

Step 1: Operating Specifications — LM25183

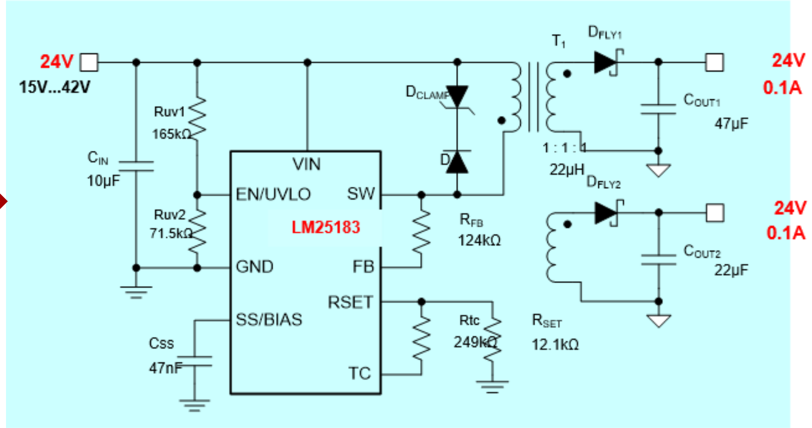
Input Voltage – Min, $V_{IN(min)}$	15	V
Input Voltage – Nom, $V_{IN(nom)}$	24	V
Input Voltage – Max, $V_{IN(max)}$	42	V
Single Output or Dual Outputs	DUAL	
Output Voltage, VOUT1	24	V
Rated Output Current, IOUT1	0.1	A
Output Voltage, VOUT2	24	V
Rated Output Current, IOUT2	0.1	A

Input xfm spec

Step 2: Flyback Transformer

Minimum Magnetizing Inductance	18.2	µH
Magnetizing Inductance, L_{MAG}	22	µH
Primary Winding DCR	40	mΩ
Secondary Winding #1 DCR	40	mΩ
Secondary Winding #2 DCR	100	mΩ
Pri-Sec Leakage Inductance	75	nH
Turns Ratio, PRI : SEC1	1 : 1	
Turns Ratio, SEC1 : SEC2	1	
Max Output Power at VIN(min)	10.44	W
Duty Cycle at $V_{IN(min)}$	61.9	%

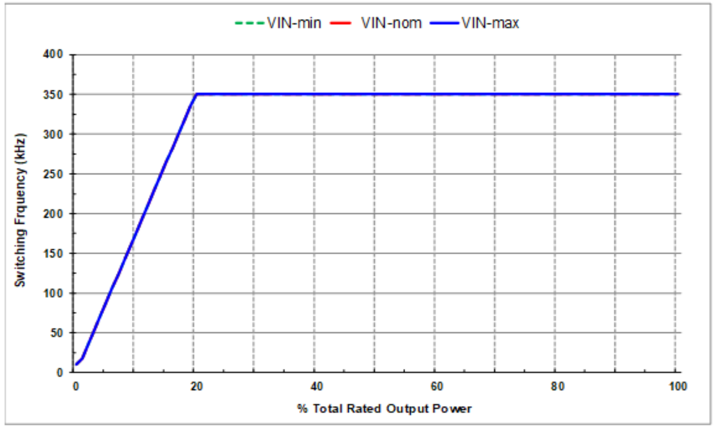
Get SCH and BOM

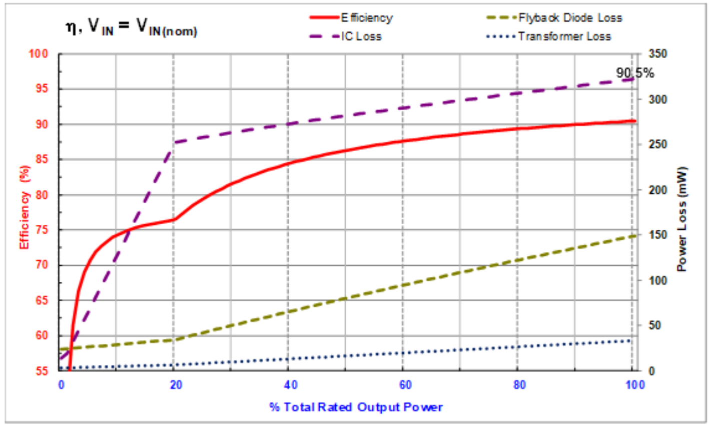


Ref Des	Value	Description	Size	Part Number	MFR	Footprint (mm)	Area (mm²)
C_{IN}	10µF	Capacitor, Ceramic, 10µF, 100V, X7R, 10%	1210	Std	Std	3.2 x 2.5	8.0
C_{OUT}	47µF	Capacitor, Ceramic, 47µF, 50V, X7R, 10%	1210	Std	Std	3.2 x 2.5	8.0
C_{OUT2}	22µF	Capacitor, Ceramic, 22µF, 50V, X7R, 10%	1210	Std	Std	3.2 x 2.5	8.0
Css	47nF	Capacitor, Ceramic, 47nF, 16V, X7R, 10%	0402	Std	Std	1.0 x 0.5	0.5
D_{FLY}	Diode	Rectifying Diode, Schottky	SMA	Std	Std	5.0 x 2.5	12.5
D_{FLY2}	Diode	Rectifying Diode, Schottky	SOD123	Std	Std	3.6 x 1.8	6.5
D_F	Diode	Clamp Circuit Diode, Fast Recovery	SOD123	Std	Std	3.6 x 1.8	6.5
D_{CLAMP}	24V	Clamp Circuit Diode, Zener, 24V	SOD123	Std	Std	3.6 x 1.8	6.5
D_{OUT}	26.4V	Output Clamp Diode, Zener, 27V	SOD523	Std	Std	1.6 x 0.8	1.3
R_{SET}	12.1k	Resistor, Chip, 12.1kΩ, 1/16W, 1%	0402	Std	Std	1.0 x 0.5	0.5
R_{FB}	124k	Resistor, Chip, 124kΩ, 1/16W, 1%	0402	Std	Std	1.0 x 0.5	0.5
R_{UV1}	165k	Resistor, Chip, 165kΩ, 1/16W, 1%	0402	Std	Std	1.0 x 0.5	0.5
R_{UV2}	71.5k	Resistor, Chip, 71.5kΩ, 1/16W, 1%	0402	Std	Std	1.0 x 0.5	0.5
R_{TC}	249k	Resistor, Chip, 249kΩ, 1/16W, 1%	0402	Std	Std	1.0 x 0.5	0.5
T_1	22µH	Transformer, 22µH, 1 : 1 : 1, 40mΩ Pri DCR, 3A Isat	10mm x 10mm	Various	Various	10 x 10	100
U_1	**LM25183**	**IC, LM25183, PSR Flyback Converter, 4.5V–42V Input**	**WSON-8**	**LM25183NGUR**	**TI**	4.0 x 4.0	16.0

Total Solution Size (buffered by 25%) 220.4 mm² =

Evaluate performance





Texas Instruments

Released reference designs

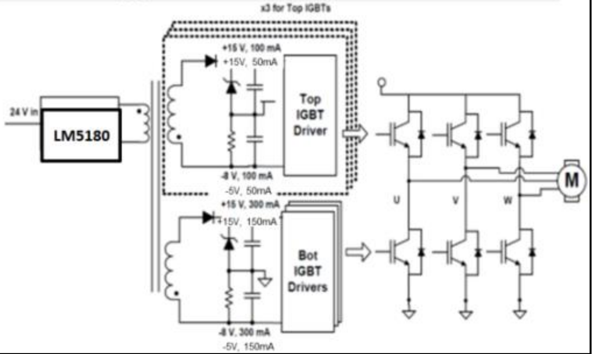
TIDA-010006
Isolated IGBT gate driver power supply using integrated switch PSR flyback controller

Features

- Isolated power supply for IGBT gate driving implemented in Fly back topology using controller with built-in switch
- Supports 6 IGBT gate drivers for 3-phase inverter
- Four isolated voltage rails: +15v / -9v (or) +15v/-5v
- Operates with unregulated 24V (±20%) input
- Output power: 1Watt per IGBT
- Functional isolation of 1.5kV DC between primary and secondary's as well as secondary's
- 5KV withstand voltage for 1 minute

Benefits

- Compact design due to built-in switch
- Primary side regulation converter eliminates need for feedback circuitry, simplifies design
- Peak efficiency of ~90% at balanced full load
- High switching frequency reduces transformer size
- Power supply shutdown feature supports STO feature



Target Applications

- AC Inverters and Servo drives
- Solar and Wind Inverters
- UPS Systems

Tools & Resources

- **TIDA-010006 and/or Tools Folder**
- **Design Guide**
- **Design Files:** Schematics, BOM, Gerbers, Software, etc.
- **Device Datasheets:**
  - LM5180

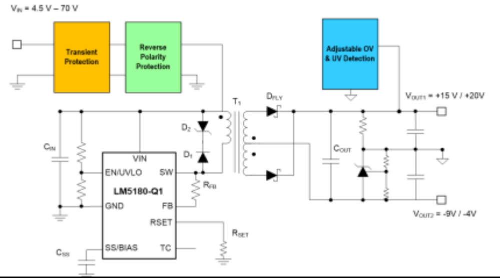
TIDA-020015
4.5V to 70V input bias supply with power stage reference design for Automotive IGBT/SiC gate drivers

Design Features

- Directly driven by 12V car battery which eliminates risk from intermediate power rail failure
- VOUT accuracy ±1% achievable
- VIN = 4.5V–70V, VOUT = +15V & -9V, ~180mA, 5% regulation to full load
- TA = –40°C to 125°C
- Boundary mode, quasi-resonant operation
- Internal loop compensation
- no need to extra clamping circuit, fits both 12V battery & 48V battery inputs
- Tested for ISO 7637-2:2004 conducted transient immunity compliance, including Load Dump

Design Benefits

- Easy-to-use, highly integrated, PSR flyback solution as Bias Power
- No opto-coupler or transformer auxiliary winding needed
- Low IQ operation at no-load current
- High efficiency at light loads
- Accurate V_{OUT} regulation performance with sensing at zero current
- Low I_Q operation and external BIAS rail option enable high efficiency at light loads



Tools & Resources

- Expected complexity of the TI Design
  - # of IC's: 2 (LM5180-Q1+LM74700-Q1)
  - # of passives: ~35
  - PCB dimensions: ~40mm*40mm
  - # of PCB layers: 2
  - Firmware needs: N/A

TI Information – Selective Disclosure

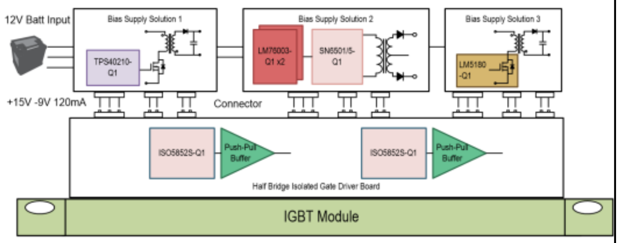
TIDA-020014
HEV/EV traction inverter power stage reference design with 3 types of IGBT/SiC bias supply solutions

Design Features

- 4.5V to 45V input, +15V and -9V outputs, configurable into +20V, -4V outputs
- Directly driven by 12V car battery with increased safety level
- Wide-Vin during very low dips in input voltage of 4.5V and up to 45V DC
- No Opto coupler
- Low IQ operation at no-load current
- High efficiency at light loads

Design Benefits

- A comprehensive design with multiple bias supply solutions for IGBT/SiC isolated gate drivers in HEV/EV
- Multiple solutions including PSR Flyback Converter, Flyback Controller, Buck + Push-pull
- Small size, compact, cost effective
- Plug in connection to IGBT driver board for easy HV evaluation
- Compatible Isolated Gate Driver board included for customer evaluation



Tools & Resources

- Expected complexity of the TI Design
  - # of IC's: 5 (LM5180-Q1, TPS40210-Q1, LM76003-Q1*2, SN6501-Q1/SN6505-Q1, LM74700-Q1*3)
  - # of passives: ~140 into 3 boards
  - PCB dimensions: ~40mm*40mm each board
  - # of PCB layers: 2
  - Firmware needs: N/A

TI Information – Selective Disclosure

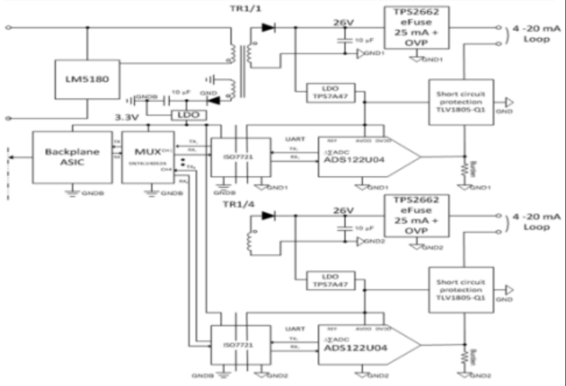
TIDACBL-0039 Intrinsic Safe Analog Input Module

Features

- 1 to 4 channel-channel isolated Intrinsic Safe AI
- Supply for the Field Transmitters with output power limitation (short limited to 35mA ().
- Input protected against miswiring (wiring to 24V)
- Transmitter supply: 26 +/-1V, Iout <35mA peak
- Input: short to L+ and GND protected, 24b accuracy

Benefits

- Short circuit protection on power output
- Mis-wiring protections on the Analog Input
- High-accuracy LM5180 allows to minimise heat dissipation from LDO (which can be low drop LDO)



Applications

- Robotics Analog Input Module for IS application
- PLC Analog Input Module

Additional details

- **Definer: Ingolf Franck -> Ben Su**
- **Field: Takeshi Sasaki**
- **Key devices: LM5180, TPS2662, ADS122U04**
- **Why is this design considered:** IS AI and how to protect inputs from shorts
- **Public market info:** IS application fast growing in Factory Automation
- **Technical status:** Design phase
- how to protect output power for

TI Information – Selective Disclosure

PSR flyback references

LM25184 Single-Output EVM User's Guide
LM5180 Single-Output EVM User's Guide
LM5180 Dual-Output EVM User's Guide
How an Auxless PSR Flyback Converter can Increase PLC Reliability and Density
Why Use PSR-Flyback Isolated Converters in Dual-Battery mHEV Systems
PSR Flyback DC/DC Converter Transformer Design for mHEV Applications
Flyback Transformer Design Considerations for Efficiency and EMI
Under the Hood of Flyback SMPS Designs

Conclusion

- **Isolated power sockets exist everywhere!**
  - **Medical and test & measurement, sensors in factory and building automation**: split rails for signal conditioning circuit (ie. op-amp, DAC/ADC)
  - **Factory automation, building automation, communications, and solar**: isolated power needed to ensure high signal integrity, with more and more sensors & faster speeds, signal integrity concerns only increase!
  - **Inverters in HVAC Systems, E-bike, Motor Drives**: Isolated gate driver requires isolated gate bias. SiC requires tighter regulation which is a great fit for No-opto PSR flyback.






Thank you!

PSR flyback converter – magnetic design considerations

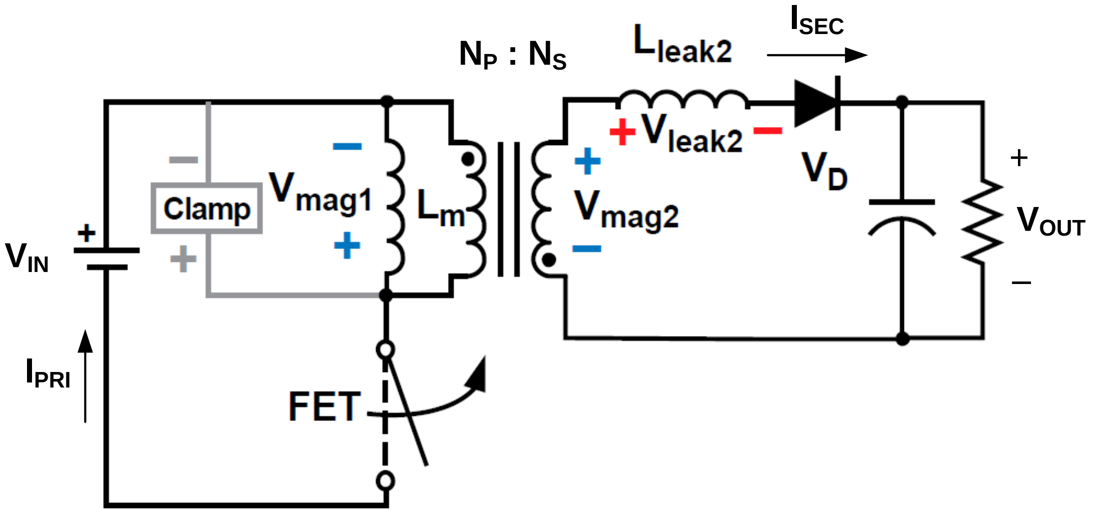
Engaging with the magnetic component vendor

Key Specification	Symbol		Purpose
Turns ratio	N_{PS}	→	Optimize flyback duty cycle range
Switching frequency	F_{SW}	→	Control core loss
Magnetizing inductance	L_{MAG}	→	Set PSR flyback mode boundaries
Saturation current (at 20°C)	I_{SAT}	→	Prevent magnetic saturation
Primary and secondary DCRs (at 20°C)	R_{PRI}, R_{SEC}	→	Reduce copper loss
Winding arrangement – interleaving, # of layers		→	Minimize R_{AC} and L_{LEAK}
Leakage inductance	L_{LEAK}	→	Reduce power loss & voltage spikes
Interwinding capacitance	$C_{P\text{-}S}$	→	Mitigate common-mode EMI
Hi-pot test limits (dielectric withstand)	$V_{ISO(PRI\text{-}SEC)}$	→	Provide a robust design
Insulation rating – functional / basic / reinforced	IR	→	Comply with safety requirements
Operating temperature range	$T_{AMB} + T_{RISE}$	→	Ensure reliability
Mechanicals – pinout, footprint, height	$L \times W \times H$	→	Minimize size and cost

Flyback transformer losses

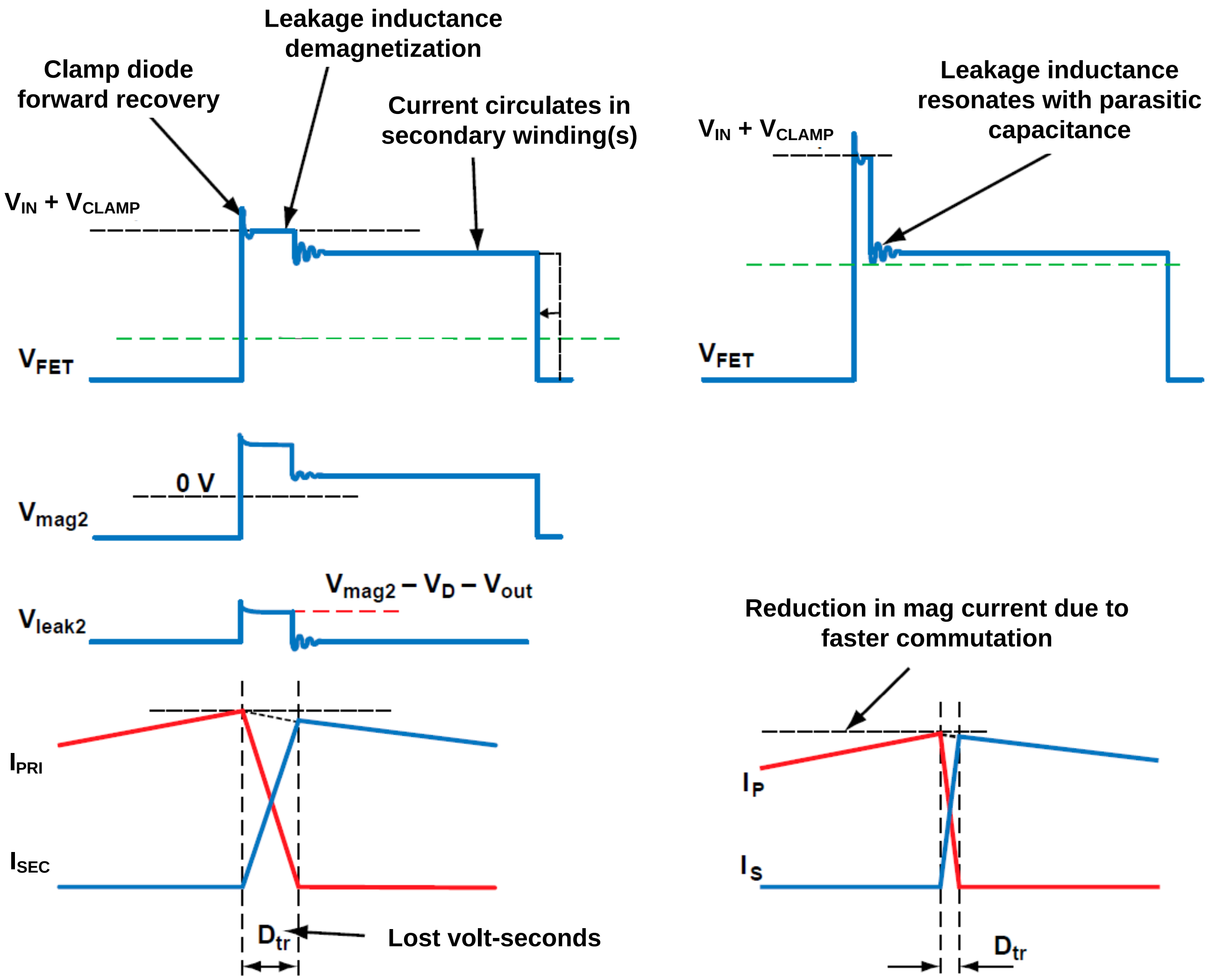
- **Copper** loss
  - DC resistance – depends on the wire cross-section and length (N, MLT)
  - AC resistance – depends on choice of wire diameter vs. F_{SW} and construction (layer stackup, proximity effects, gap effect)
- **Core** loss
  - Related to core material characteristics, B_{DC}, B_{AC}, F_{SW}
- **External** loss
  - Leakage inductance energy $$P_{LEAK} = \frac{L_{LEAK} \cdot I_{SW\text{-}PK}^{2}}{2} \cdot F_{SW}$$
    - Large percentage of this power dissipated in external clamp circuit or RC snubber
    - Magnetizing energy also dissipated – depends on clamp level and leakage inductance

Flyback transformer – impact of leakage inductance



Leakage inductance affects:

- Conversion efficiency
- Voltage spikes during commutation
  - clamp circuits and snubbers
- Current slew rate & loss of volt-seconds
- H-field radiated EMI
- Cross regulation in multi-output designs



Low clamp voltage

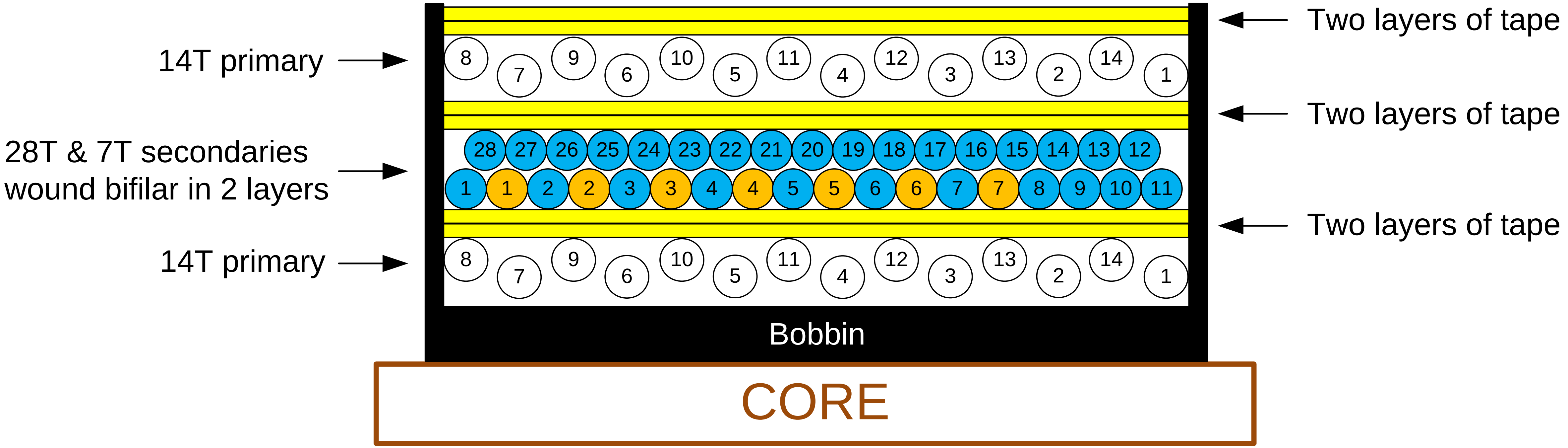
High clamp voltage

Flyback transformer design – impact on efficiency / x-reg

1. Guidelines to **optimize efficiency**
   - Choose the transformer **turns ratio** for best efficiency and duty cycle range
   - Minimize **leakage inductance** from primary to main (high-current) secondary
     - Interleave primary around secondary (or vice versa if $N_P < N_S$)
     - Reduces voltage spikes and power dissipation
     - Locate highest power secondary closest to primary (multi-output designs)
   - Minimize transformer high-frequency **conduction loss**
     - Use bifilar or multifilar wires when necessary to reduce AC resistance
     - Interleave primary and secondary windings
     - Select core shape for minimum number of layers (wide bobbin width)

2. Guidelines to **optimize cross regulation**
   - Minimize **leakage inductance** *between secondary windings* as it impacts cross regulation and secondary current wave shapes
     - Wind two highest power secondaries **bifilar** for best coupling
     - Consider **DC or AC stacking** for same polarity outputs that share common GND

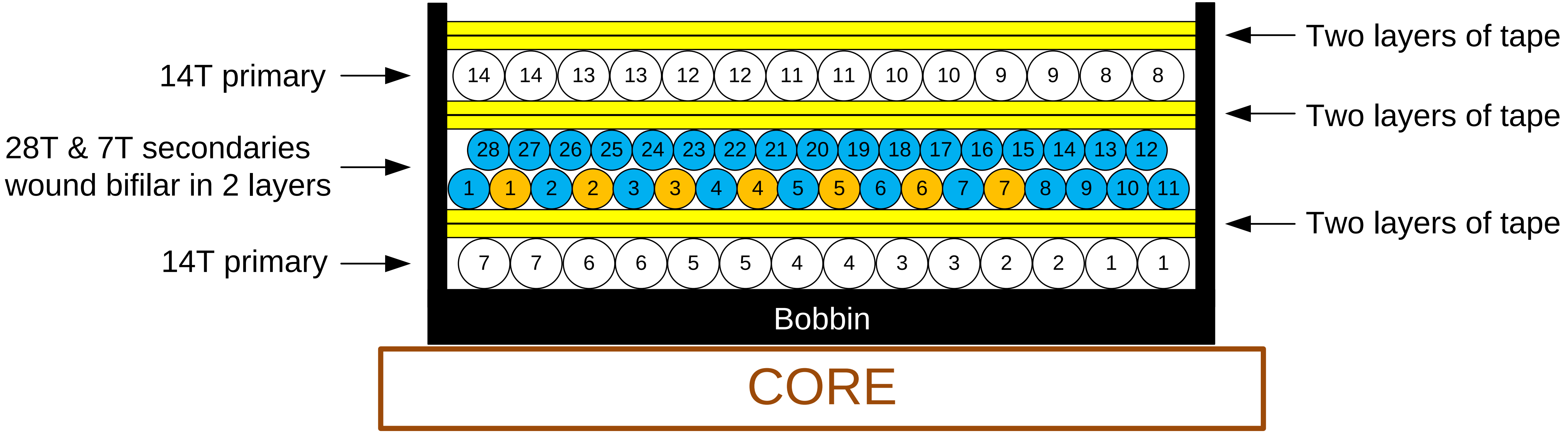
Dual-output transformer construction #1 14 : 28 : 7



Primary winding 50/50 parallel split

Parallel primary windings is a more convenient construction, but the **high dv/dt (noisy) SW node voltage** appears both on the inner and outer layers

Dual-output transformer construction #2 14 : 28 : 7



Primary winding 50/50 series split

Wind first **half** of primary on inside layer nearest the bobbin and the other **half** on the outside

→ Noisy node (SW) **shielded** on inside & quiet node (VIN) connects to outside layer

→ Place windings with similar dv/dt adjacent to each other to reduce interwinding capacitance

→ Better common-mode EMI performance