Using the bq4845 for a Low-Cost RTC/NVSRAM Subsystem

Introduction

The bq4845 combines a low-power real-time clock (RTC), a microcontroller supervisor, and a nonvolatile control circuit for static RAM on one IC. The part forms the basis of a low-cost, reliable RTC plus nonvolatile SRAM subsystem for many different embedded applications. By providing direct connections for a quartz crystal, an SRAM, and a backup source, the bq4845 eliminates as many as 15–20 discrete components.

The bq4845 contains 16 memory registers for clock, calendar, and control information as shown in Figure 1. The clock tracks seconds through years in binary coded decimal 12– or 24–hour format. The control information monitors and programs the onboard microcontroller supervisor and interrupts. The memory registers have the same interface as a standard byte-wide SRAM and can be mapped within the memory address space.

Figures 2 and 3 show how a typical battery backed-up RTC plus SRAM discrete solution compares with the bq4845 approach. The highly integrated bq4845 eliminates the discrete components needed in the power control, write protection, and reset circuits. It also features:

- Ultra-low backup current (< 500nA)
- Power-on reset
- Programmable watchdog timer with a separate output
- x8 real-time clock data
- Power-fail and periodic interrupt
- Low backup battery warning

0	Seconds	00
1	Seconds alarm	01
2	Minutes	02
3	Minutes alarm	03
4	Hours	04
5	Hours alarm	05
6	Day	06
7	Day alarm	07
8	Day-of-week	08
9	Month	09
10	Year	0A
11	Programmable rates	0B
12	Interrupt rates	0C
13	Flags	0D
14	Control	0E
15	Unused	0F

MM-13

Figure 1. Address Map

Contents

This application note discusses the key aspects of bq4845 operation.

Component Selection

SRAM

The bq4845 is designed to work with a low-power slow CMOS SRAM directly connected to V_{OUT} and $\overline{CE}_{OUT}$. Through these pins, the bq4845 provides power and a conditional chip enable to the memory. With valid system power, the output of the bq4845 supplies up to 100mA with $V_{OUT} = V_{CC}$ - 0.3V, and the chip enable control passes through with a propagation delay of less than 12ns. With no system power, the bq4845 switches over to the backup source and holds the chip enable inactive. In this mode, the bq4845 supplies up to 100µA with $V_{OUT} = V_{BACKUP}$ - 0.3V.

Monolithic CMOS SRAMs are available in byte-wide densities of 16kbits to 4Mbits. The section entitled "Backing Up Multiple SRAMs" describes how to use multiple SRAMs with the bq4845 for word-wide or odd memory configurations.

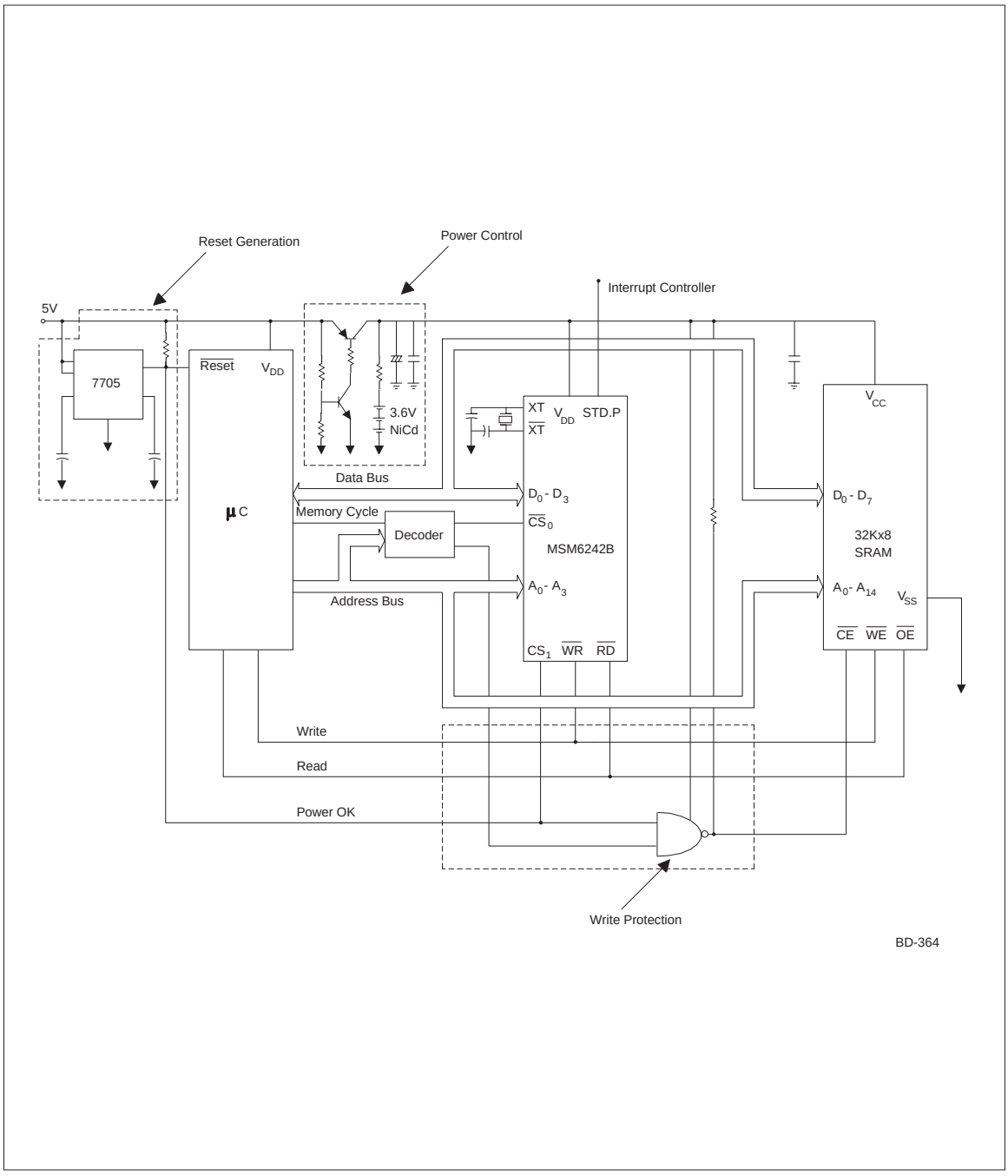


Figure 2. Discrete Solution

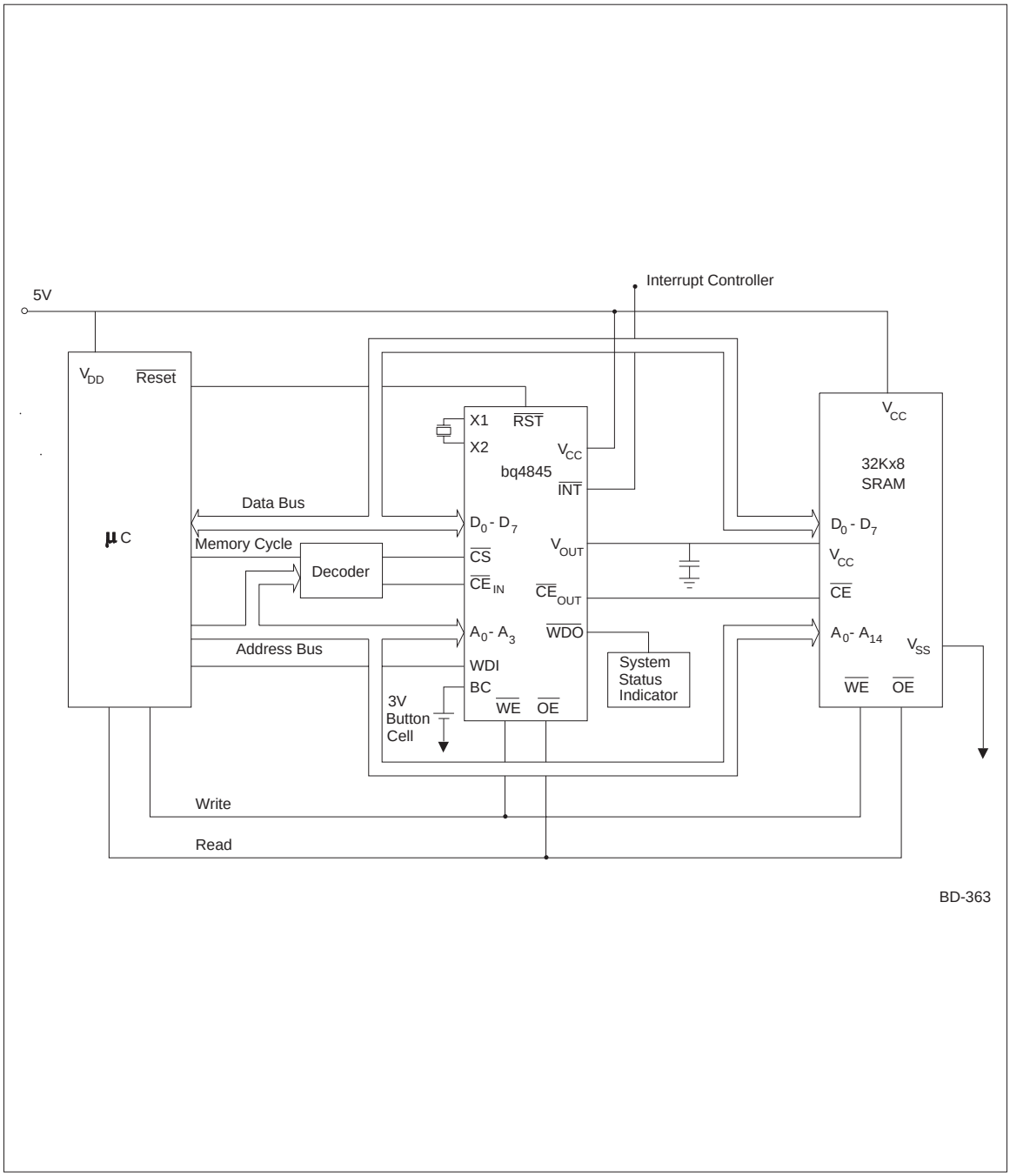


Figure 3. bq4845 Approach

To minimize power consumption in active and backup mode, follow these recommendations:

1. Use an L-L power rated SRAM. They typically consume less than 70mA in active mode and less than 1µA at 3V and 25°C in standby mode with a minimum data-retention voltage of 2V.
2. Use low-leakage ceramic bypass capacitors of 0.1µF across the SRAM and RTC.
3. Connect active high second chip enables (CE2) to V_{OUT} of the bq4845, **not** to V_{CC}.

Crystal

The bq4845 oscillator is designed to work with a 32.768kHz tuning fork type crystal connected directly to X1 and X2 with no external components required. The crystal should have the characteristics described in Table 1.

With the properly selected crystal, the bq4845 real-time clock should be accurate to ±1 minute per month at room temperature with no trim capacitors. If greater accuracy is desired, a small trim capacitor of no more than 10pF can be connected from X2 to GND. The section entitled "Calibrating the Clock" describes how to adjust the bq4845 clock.

Backup Source

The backup source on the BC input provides power to the real-time clock and the external SRAM when main system power is not applied. The backup source can be a primary (non-rechargeable) lithium cell, a secondary (rechargeable) NiCd pack, or a super capacitor. The choice of technology and capacity depends on the total data-retention load current and the anticipated amount of time the application is without power.

The total data-retention load of an RTC/NVSRAM subsystem consists of the current required to power the clock and maintain data in the SRAM, or $I_{DR} = I_{RTC} + I_{SRAM}$. I_{DR} varies with temperature and voltage. Therefore, the backup conditions of the application must be considered to determine the typical I_{DR}.

Figures 4 and 5 show how the data-retention currents of the bq4845 and an L-L rated SRAM vary over temperature. For most applications, the majority of the backup time is close to 3V and 25°C. Under these conditions, the typical data-retention current for a bq4845 application with a single L-L rated SRAM is I_{DR} = 0.5µA + 1µA or 1.5µA.

The bq4845 works with a primary or secondary cell. If the application spends the majority of its useful life powered-up, a super capacitor may be sufficient to meet the data-retention requirements of short intermittent power outages. For applications with long potential system-off periods, a primary lithium cell or secondary NiCd pack should be used.

The bq4845 requires the backup source to be within 2.3V to 4.0V. The potential of the source is checked on power-up. When it is approximately 2.1V, the battery low flag is set, indicating that clock and RAM data may be invalid.

If the backup source does not make a connection to the BC pin and the BC pin is floating, then on power-up, RST remains low.

Table 1. Crystal Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW

Lithium

The bq4845 is best suited for use with a primary lithium cell having a nominal voltage of 3V. The long shelf life, flat discharge curve, and high energy density allow a small lithium coin cell to backup a bq4845/SRAM subsystem for greater than 10 years. The minimum required capacity is given by:

Equation 1

$$C(Ah) = L * (1 - \frac{T_{ON}}{100}) * I_{DR} * 8760$$

where:

- L = useful lifetime of the equipment (years)
- T_{ON}= % of time system power is on
- I_{DR} = total data-retention current (A).

T_{ON} can be factored into the equation because capacity of the lithium cell is not consumed when system power is applied.

An inexpensive lithium coin cell meets the data-retention requirements of most single SRAM applications. These cells range in capacity from 30mAh to 300mAh. Cylindrical lithium cells offer greater than 1000mAh. The two chemistry types are: BR and CR. BR has better shelf life characteristics at elevated temperatures and should be used in industrial temperature operating environments to ensure that storage life wearout does not limit the backup time below the calculated value. The cells are available with solder tab connections for PCB mounting, or can be socketed for user replaceability.

NiCd

A small NiCd pack can be trickle-charged from the system voltage supply using a resistor. The value of the resistor depends on the recommended trickle charge rate of the battery manufacturer. The optimum series configuration is 3 cells, since this gives a nominal voltage of 3.6V. The capacity can be sized using equation 1 with T_{ON} = 0, and L equal to the longest anticipated time the system will be without power. A small 3.6V NiCd pack can provide years of clock operation and data retention using the bq4845 and an L-L rated SRAM. Like the lithium cells, the 3-cell NiCd packs are available with solder tabs.

Super Capacitor

A low-leakage super capacitor can be used to back up the bq4845 plus an external L-L SRAM. The zener diode across the capacitor keeps the voltage from exceeding the 4.0V limit on the BC input. The series charge resistor depends on the size and type of capacitor. The approximate backup time is given by the equation:

Equation 2

$$T(days) = \frac{(C * \Delta V)}{(86400 * I_{DR})}$$

where:

- C = capacitor value (F)
- ΔV = valid voltage back-up range (V)
- I_{DR} = total data-retention current (A)

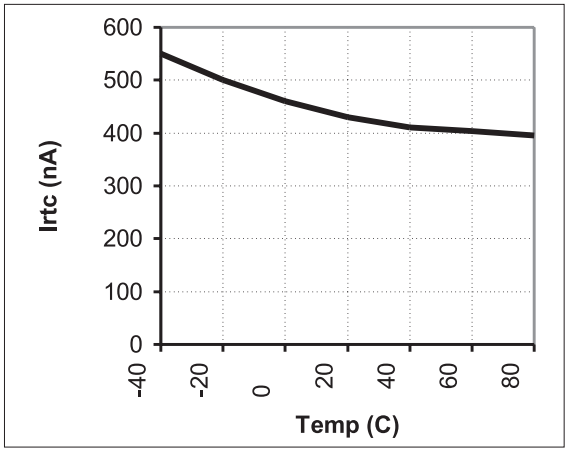


Figure 4. bq4845 Data-Retention Current at V_{BC} = 3V

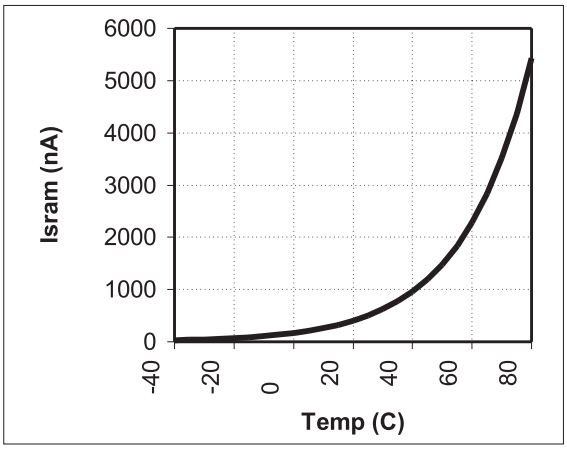


Figure 5. Typical L-LSRAM Data-Retention Current at V_{CC} = 3V

ΔV = 4.0 - 2.3 or 1.7V for a bq4845 application. Thus, a 1F or 2F super capacitor can provide weeks of backup time for the bq4845 RTC and a single L-L SRAM.

Figure 6 shows the three different backup configurations.

Board Layout

Crystal Connection

The quartz crystal should be connected directly to X1 and X2. A small trim capacitor can be placed on X2 for higher clock accuracy. To minimize the risk of noise coupling into the bq4845 RTC oscillator, follow these recommendations:

1. The crystal should be located as close as possible to the pin connections on the bq4845.
2. The pins should be surrounded by a ground guard ring.
3. No signals should run directly below the crystals or below the traces to the X1 and X2 pins.

Figure 7 shows an example configuration.

Backup Source Connection

The backup source placement is not as critical as it is for the crystal. Still, it should be placed as close to the bq4845 as possible, although the designer should also consider accessibility if the battery is to be easily replaced. The backup source should be connected directly to the BC input (+) and V_{SS} (-).

Lithium primary cells in electronic equipment require protection against reverse charging from V_{CC} when system power is on. The bq4845 battery input circuit includes two protection diodes in series between BC and V_{CC}. The protection diodes meet the UL requirements for the use of a lithium cell as a backup source in electronic circuits. **Therefore, no external reverse charging circuit is required or recommended**. The bq4845 is listed under UL file number E134016.

Calibrating the Clock

Accuracy Measurement

With a properly selected quartz crystal connected directly to X1 and X2, the bq4845 should be accurate to ±1 minute per month at room temperature with no trim capacitor. The accuracy of the clock changes with temperature as seen in Figure 8. If higher accuracy is required at room temperature, or the system operates at the temperature extremes, a small trim capacitor can be placed between X2 and ground. A simple calibration routine can be used to measure the frequency and trim the capacitor for optimum clock accuracy at the use temperature.

The calibration software routine uses the periodic interrupt to measure the frequency variance of the real-time clock. The interrupt rate is monitored on the $\overline{INT}$ pin. In this test setup, the $\overline{INT}$ pin is connected to a frequency meter, and should not interrupt the microcontroller. It may be beneficial to provide a jumper for the $\overline{INT}$ pin on the board design in order to disconnect it from the interrupt controller when the calibration routine is run. No test equipment should be connected directly to either crystal pin, as the added loading alters the characteristics of the oscillator and can make tuning impossible.

The calibration routine should be performed at the temperature at which the system spends the majority of its

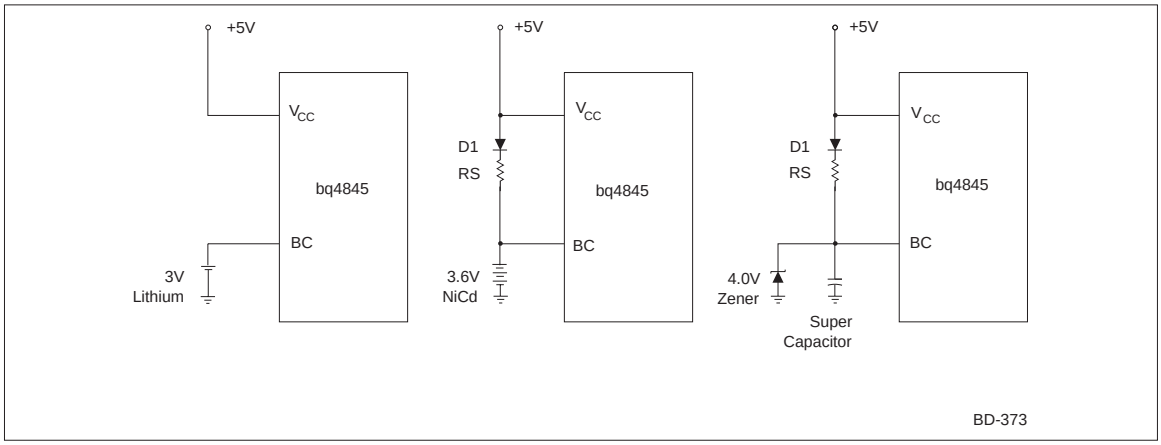


Figure 6. Backup Configurations

operating time. The calibration routine consists of the following sequence of operations (see Figure 9):

1. Control Register: Write $[XXXX01XX]_b$. Turns on the RTC.
2. Programmable Rates Register: Write $[XXXX0011]_b$. Sets the periodic interrupt rate to 8.192kHz.
3. Interrupts Enable Register: Write $[00000100]_b$. Enables only the periodic interrupt.
4. Flags Register: The program should now loop on reading this register. Reading the register resets the interrupt flag PF and returns $\overline{INT}$ high. The next interrupt will re-assert PF and $\overline{INT}$. Reading the register must occur at a rate which exceeds the periodic rate in order to catch all the transitions. The periodic rate can be adjusted by programming register B.
5. Monitor the frequency on the $\overline{INT}$ pin with a high-resolution meter. The $\overline{INT}$ pin is active low so the meter should trigger on a negative transition. Any

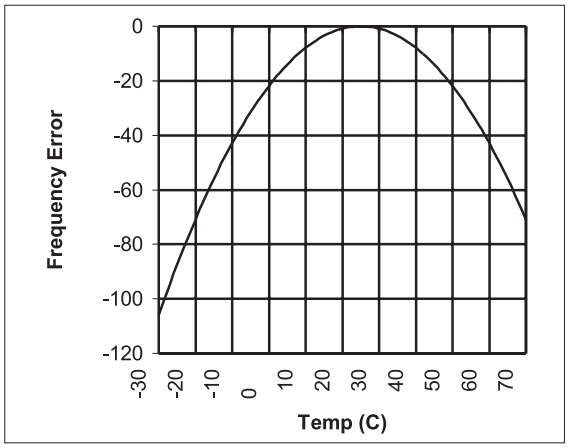


Figure 8. Frequency Error

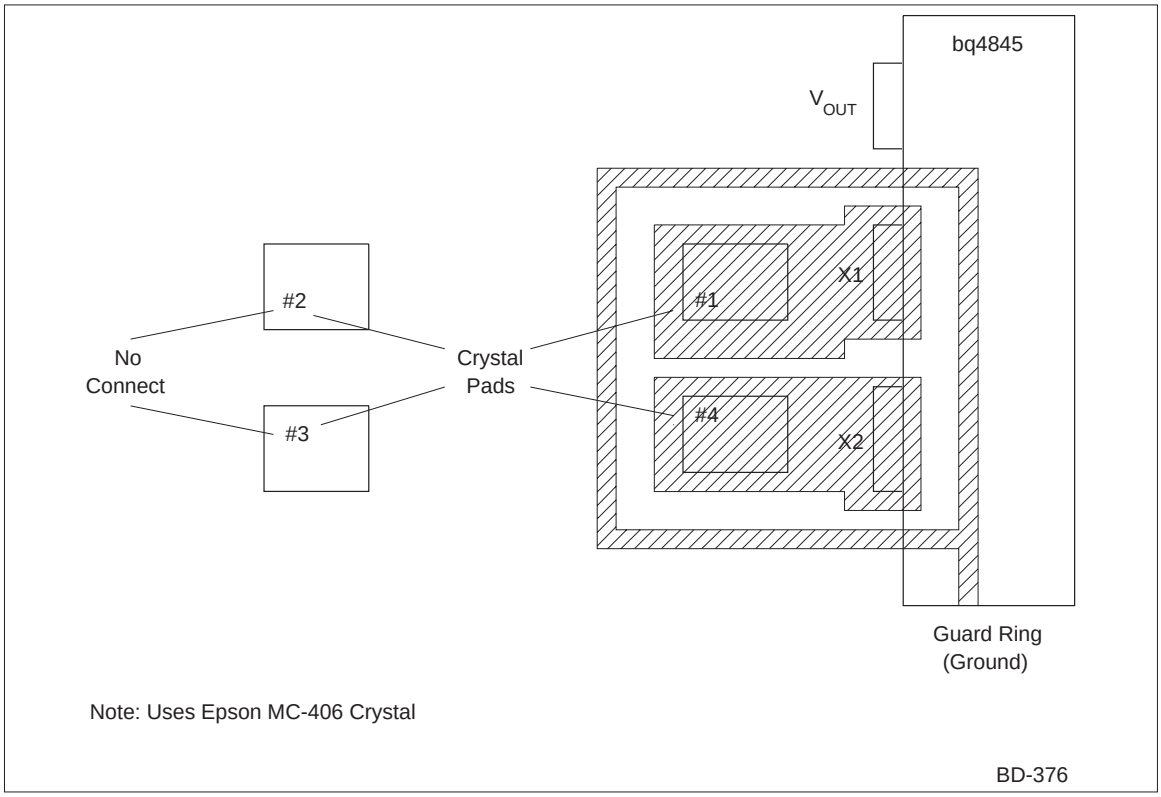


Figure 7. Crystal Connection

deviation from the set periodic rate indicates clock error.

6. Adjust the trim capacitor to provide a frequency as close to the set periodic rate as possible.

Adjustment Considerations

The bq4845 uses a very low-current oscillator and is sensitive to capacitance on the crystal inputs. To ensure the real-time clock does not stop in the low-voltage battery-back-up mode, the total capacitance on X2 should be no more than 15pF, including the trace capacitance. With short lead traces, the maximum recommended trim capacitor is 10pF. As a rule of thumb, each additional 1.54pF of capacitance on X2 results in a decrease of 0.8Hz or 64 seconds per month.

System Supervision

The bq4845 includes three system supervisory functions: Power-fail monitoring, µP monitoring, and µP reset generation. The three functions work together to provide orderly power-down and restart procedures.

Power-Fail Warning

The bq4845 can be programmed to generate a power-fail warning. The warning can be used to alert the microcontroller to save critical data in the SRAM prior to µP reset generation.

To program the power-fail warning, set the PWRIE bit of register C to 1. When the 5V system supply on V_{CC} drops below V_{PFD} as seen in Figure 10, the interrupt output $\overline{INT}$ goes low. Since other sources (clock alarm and periodic interrupt) can activate the the $\overline{INT}$ output, register D can be read to see if the power-fail warning flag is set to 1. If PWRF is 1, a power-fail condition has occurred and the microcontroller has 100µs to store data prior to assertion of the µP reset by the bq4845.

The power-fail thresholds (V_{PFD}) are set at 4.62V (typical) for the bq4845 and 4.37V (typical) for the bq4845Y. The $\overline{INT}$ pin is open drain, and requires a pull-up resistor.

Power-on Reset

The active-low power-on reset is asserted 100µs after power-fail detection as seen in Figure 10. The reset remains asserted for 200ms after valid power returns to provide for system stabilization. The output is open drain, and requires an external pull-up resistor.

Watchdog Timer

The watchdog timer is used to supervise processor operation. The watchdog monitors the WDI input. This input can be connected to a bus line or an I/O port. If WDI is not toggled within the programmed time-out period, the bq4845 asserts $\overline{WDO}$ and $\overline{RST}$. The timeout is programmed in register B according to Table 2. The bq4845 retains this time-out period through power cycles as long as battery power is valid. If the bq4845 loses backup power in data-retention mode, the default time-

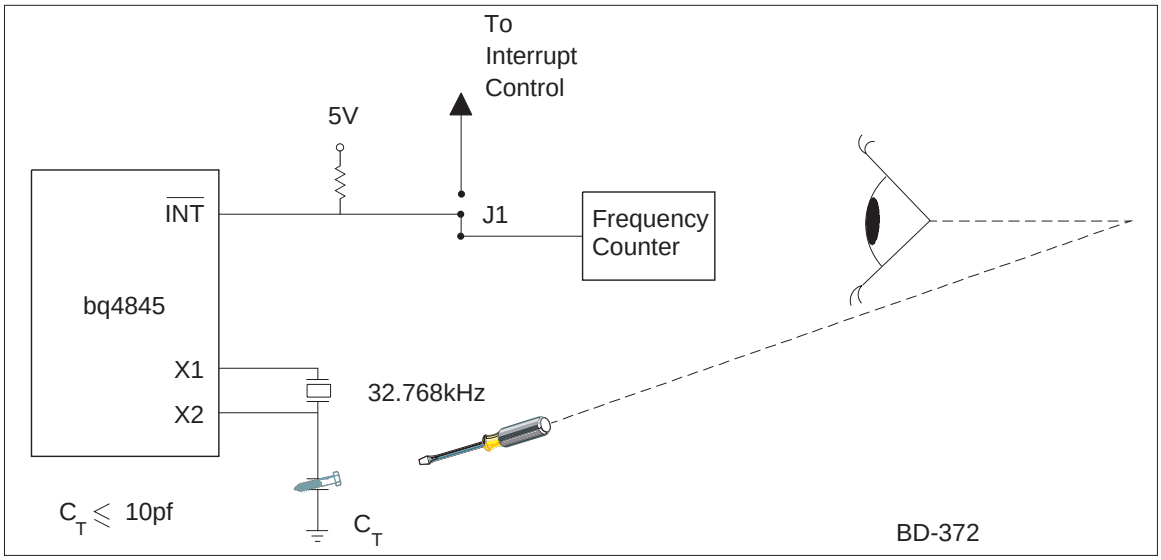
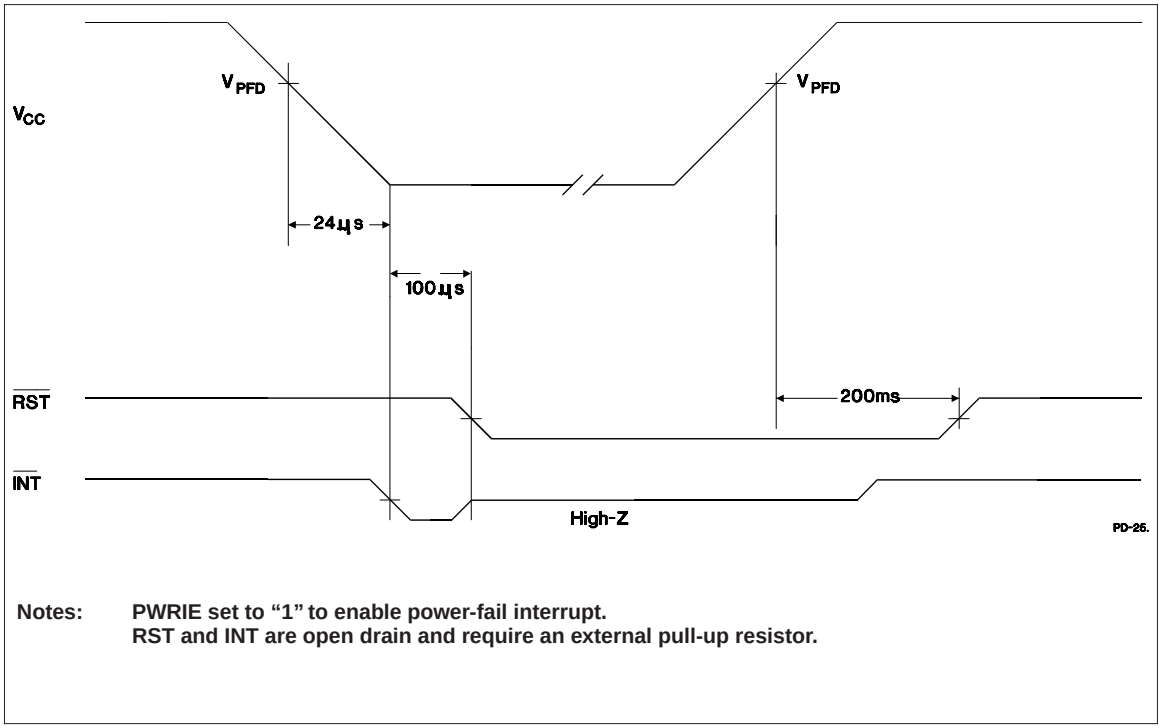


Figure 9. Frequency Adjustment

out period is 1.5s. The watchdog timer is disabled **only** if WDI is left floating.

If a watchdog time-out occurs, the run time of the subsequent initialization routine must be less then the programmed time-out period or the system may never recover.

$\overline{WDO}$ can be used to indicate to the system that the reset was caused by a watchdog fault and not a power failure. $\overline{WDO}$ is reset after a watchdog fault by a transition



Notes: **PWRIE set to "1" to enable power-fail interrupt.**
RST and INT are open drain and require an external pull-up resistor.

Figure 10. Power-Down/Power-Up Timing

Table 2. Watchdog Time-Out Rates

WD2	WD1	WD0	Watchdog Time-out Period
0	0	0	1.5s
0	0	1	23.4375ms
0	1	0	46.875ms
0	1	1	93.75ms
1	0	0	187.5ms
1	0	1	375ms
1	1	0	750ms
1	1	1	3s

on WDI. $\overline{WDO}$ can be connected to an audible alarm or a controller input I/O pin. $\overline{WDO}$ is held high when V_{CC} is below the power-fail threshold, battery-backup mode is enabled, or WDI is left floating.

Backing Up Multiple SRAMs

While monolithic SRAMs come in a wide variety of densities, some memory configurations may require the use of two external memory chips.

Word-Wide Configurations

For a word-wide or x16 configuration, two L-L rated SRAMs can be put in parallel as shown in Figure 11. The combined active current of the memory at the operating cycle must be less than 100mA. The total data- retention current is

$$I_{DR} = I_{RTC} + 2 * I_{SRAM}.$$

Odd Configurations

To build an odd memory configuration like a 2Mbit RTC/NVSRAM subsystem, additional logic may be needed. One 7400 CMOS NAND gate provides the chip select decoding for the 256Kx8 NVSRAM configuration shown in Figure 12.

Additional Integration—bq4847

The bq4847 combines the bq4845 with a crystal and lithium coin cell in a 600-mil dual-in-line package to offer an additional level of integration. The only component required for the RTC/NVSRAM subsystem is the static RAM connected directly to the bq4847. The internal battery has over 130mAh of capacity to provide greater than 10 years of data retention in most applications. To prevent inadvertent battery discharge during handling, the bq4847 battery is isolated from the V_{OUT} and $\overline{CE}_{OUT}$ pins until the initial application of V_{CC}. After V_{CC} is applied, the battery connects to V_{OUT} whenever V_{CC} drops below V_{SO} (typically 3V).

The internal crystal meets the specifications described in Table 1. The bq4847 is calibrated at the factory to provide clock accuracy better than one minute per month at 25°C.

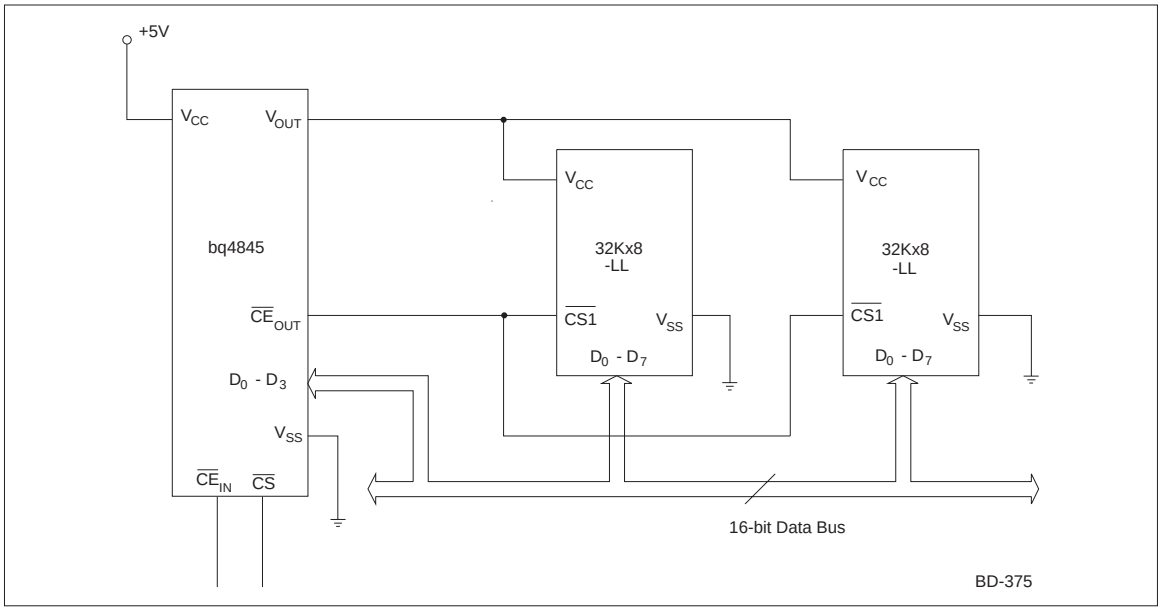


Figure 11. 32Kx16 Memory Configuration

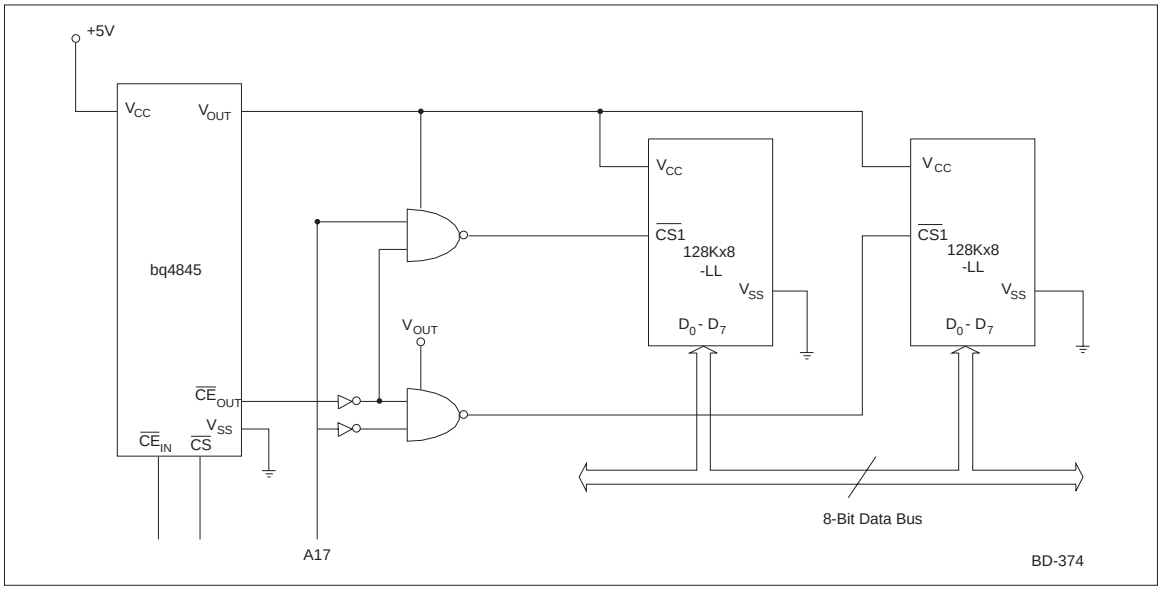


Figure 12. 256Kx8 Memory Configuration

Notes

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