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bq20z75/95 Printed-Circuit Board Layout Guide

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ABSTRACT

New single-package IC fuel gauges can significantly simplify PCB layout. Attention to layout, however, is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that can be troublesome. This document presents guidelines that can ensure a stable and well performing project.

Introduction

New single-package integrated circuits (IC) are available that combine the separate fuel gauge and AFE chips into one small package. This configuration can significantly simplify printed-circuit board (PCB) layout, but attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues. Careful placement and routing with regard to the principles described in the following discussion can ensure success.

IC Orientation

The orientation of the fuel gauge IC is often driven by the shape of the board. Some pack designs have severe dimensional constraints, such as only allowing for a 10-mm width. This leaves no choice but to mount the bq20z75/95 IC in such a manner that no space is available for decoupling/filter capacitors to be placed next to the IC pins. In that case, adequate decoupling can be provided by mounting the capacitors on the other side of the board, as shown in Figure 1.
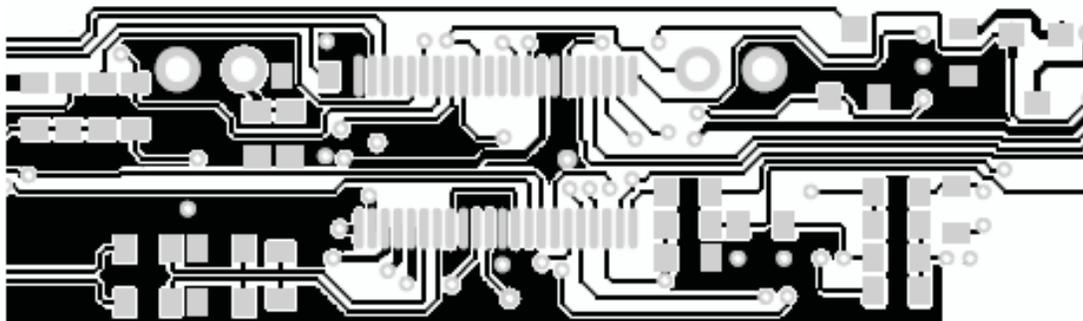

Figure 1. Typical Narrow Board Design Where Most Decoupling/Filter Capacitors Are Located on Other Side.

bq20z75/95 Power Supply Decoupling Capacitor

Fortunately, only one capacitor needs to be extremely close to the IC. The power supply decoupling from REG to VSS is very important for optimal operation of the bq20z75/95 advanced gas gauge. For the bq20z95, this is the 1-µF ceramic capacitor from pin 32 to pins 31 and 34. Ensure that a heavy copper trace is between pins 31 and 34. For the bq20z75, the capacitor is from REG pin 26 to VSS pins 25 and 28. This is C15 in the reference schematic in Figure 10.

To keep the loop area small, place both terminals of this capacitor within 3 mm of the IC, and centered around pin 32 (bq20z95) or pin 26 (bq20z75). Use the shortest possible traces. A large loop area renders the capacitor useless and forms a little loop antenna for noise pickup.

Ground System

The bq20z75/95 requires a low-current ground system separate from the high-current PACK(–) path. Refer to the ground symbols in the bq20z75/95 reference designs, and provide the separate low-current ground system accordingly. It is important that the low-current ground system only connects to PACK(–) at the sense resistor Kelvin pick-off point as shown in Figure 2. The use of an optional inner layer ground plane is recommended, but not required, for the low-current ground system.
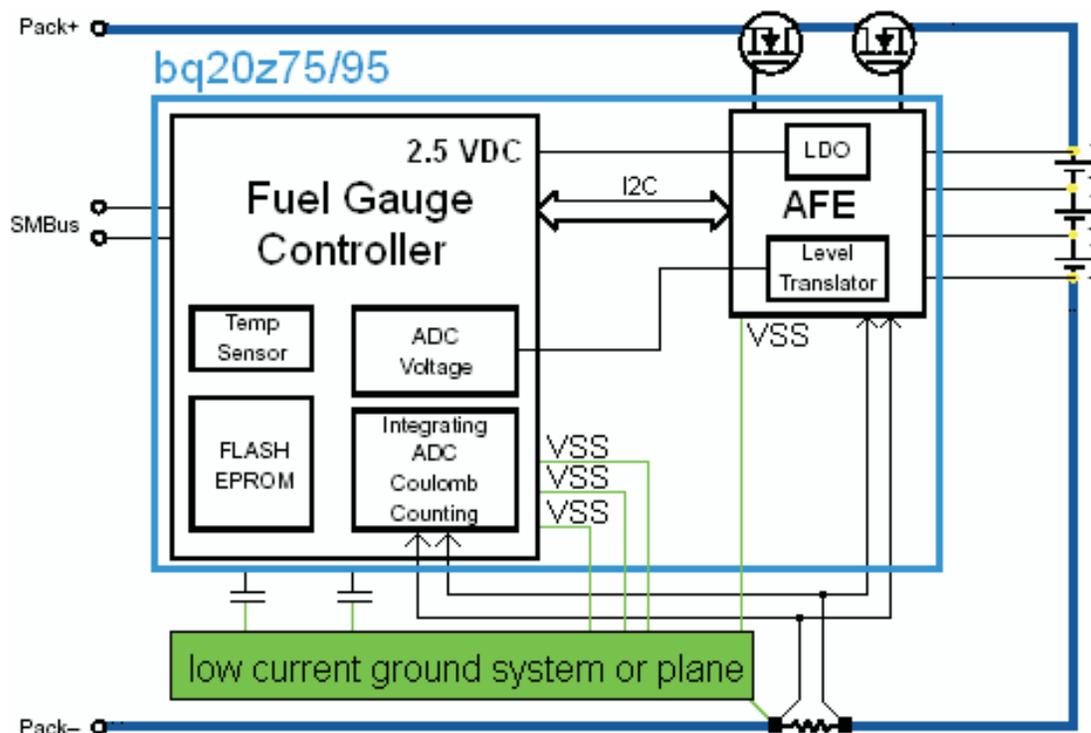
Figure 2. Diagram Showing bq20z75/95 Using Low-Current Ground System for Its Vss Pins and Associated Components

Kevin Connections

Kelvin voltage sensing is extremely important in order to accurately measure current and top and bottom cell voltages. Figure 3 and Figure 4 demonstrate *correct* and *incorrect* techniques, respectively.
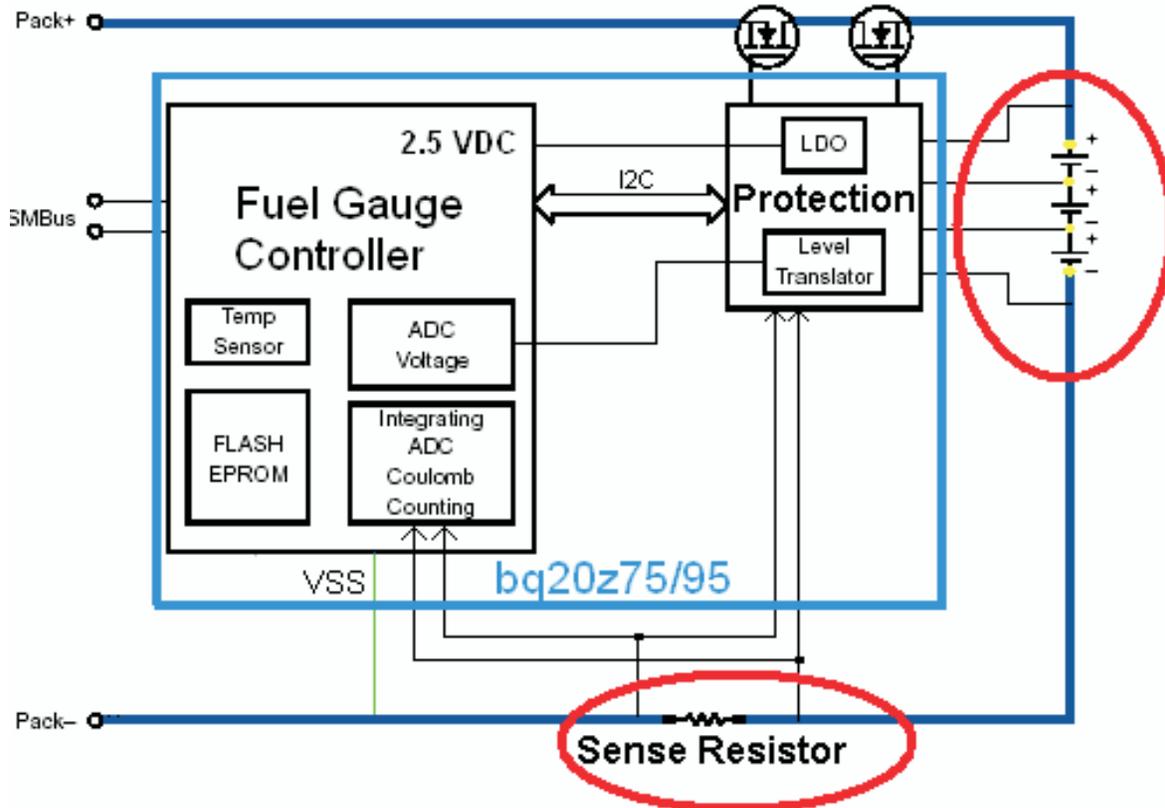
Figure 3. Incorrect Kelvin Voltage Sensing Technique

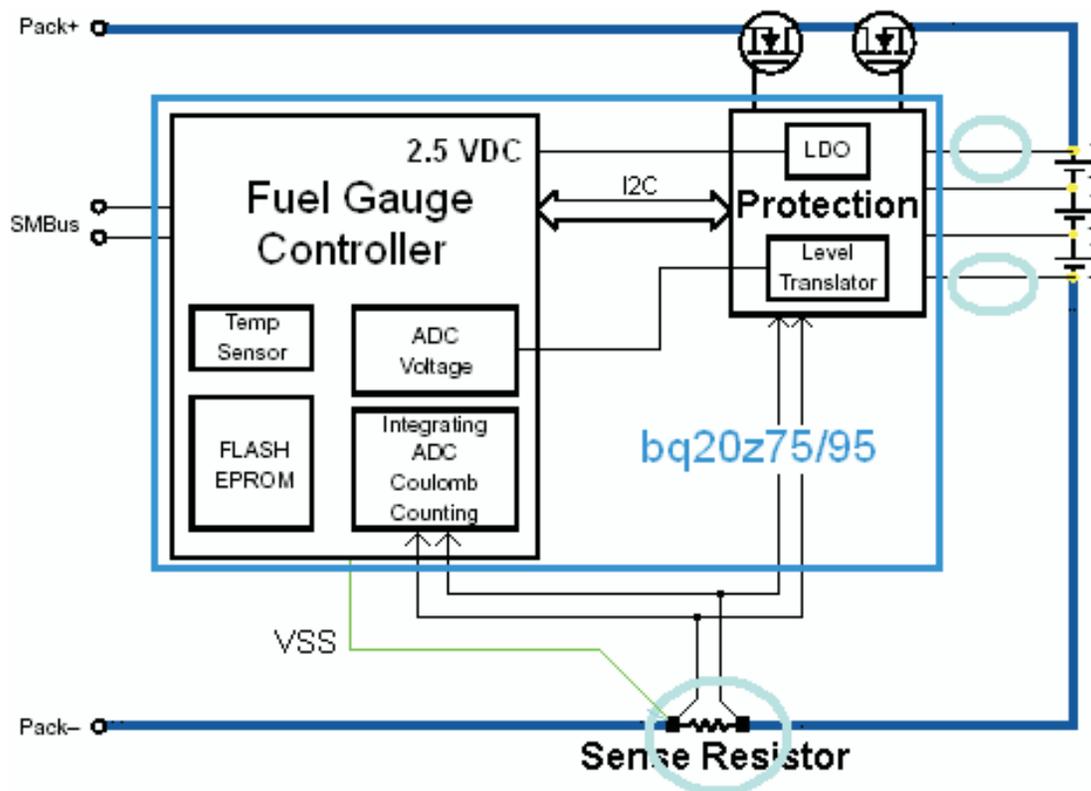In Figure 3, sensing through high-current copper traces produces measurement errors.

Figure 4. Correct Kelvin Voltage Sensing Technique

As Figure 4 shows, in some cases, the top and bottom cell voltage sensing may be extended out to the cells.

RBI and LED Capacitors

The 3.3-V LEDOUT (pin 8) output requires a 4.7-µF ceramic capacitor when LEDs are used, but still requires 2.2 µF capacitance for loop stability when LEDs are not used, as with the bq20z75. This capacitor also should be placed as close to the IC as is practical, but several millimeters of copper trace is not a problem.

Placement of the RBI capacitor is not as critical. It can be placed further away from the IC.

MRST Connection

RESET and MRST are connected to allow the internal AFE to control the gas gauge reset state. The connection between these pins must be as short as possible in order to avoid any incoming noise. The recommended direct interconnection presents no problem. If unwanted resets are found, one or more of the following solutions may be effective:

- Add a 0.1-µF capacitor between MRST and ground.
- Provide a 1-kΩ pullup resistor to 2.5 V at RESET.
- Surround the entire circuit with a ground pattern.

Normally, these steps are not required. If a test pin is added at MRST, provide it with a 10-kΩ series resistor.

Communication Line Protection Components

The 5.6-V zener diodes, used to protect the communication pins of the bq20z75/95 from ESD, should be located as close to the pack connector as possible. Return the grounded end of these zener diodes to the Pack(−) node, rather than to the low-current digital ground system. In this manner, ESD is diverted away from the sensitive electronics as much as possible.

Protector FET Bypass and Pack Terminal Bypass Capacitors

The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuits. In Figure 5, an example layout demonstrates this technique.
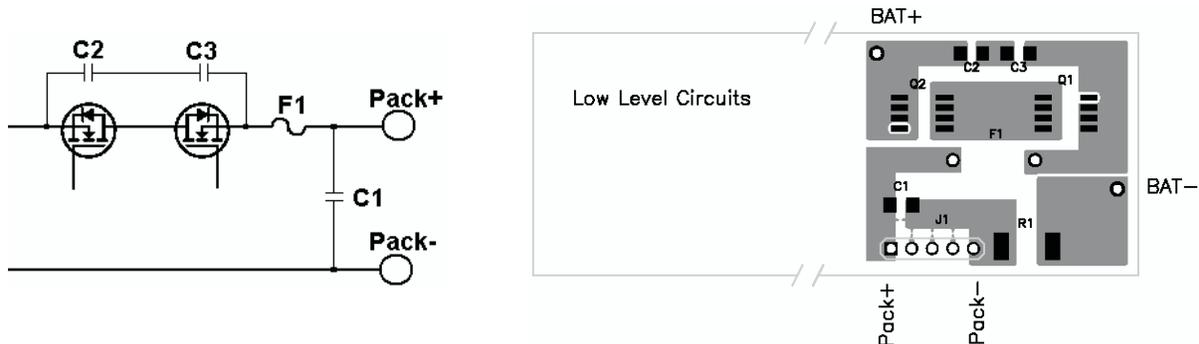
Figure 5. Using Wide Copper Traces Lowers the Inductance of Bypass Capacitors C1, C2, C3

Board Offset Considerations

Although the most important component for board offset reduction is the decoupling capacitor for REG (2.5 V REG), additional benefit is possible by using this recommended pattern for the Coulomb Counter differential low-pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100-Ω resistors as shown in Figure 6. If the current sense leads are long, ensure that the 100-Ω resistors are within 10–15 mm from the IC.
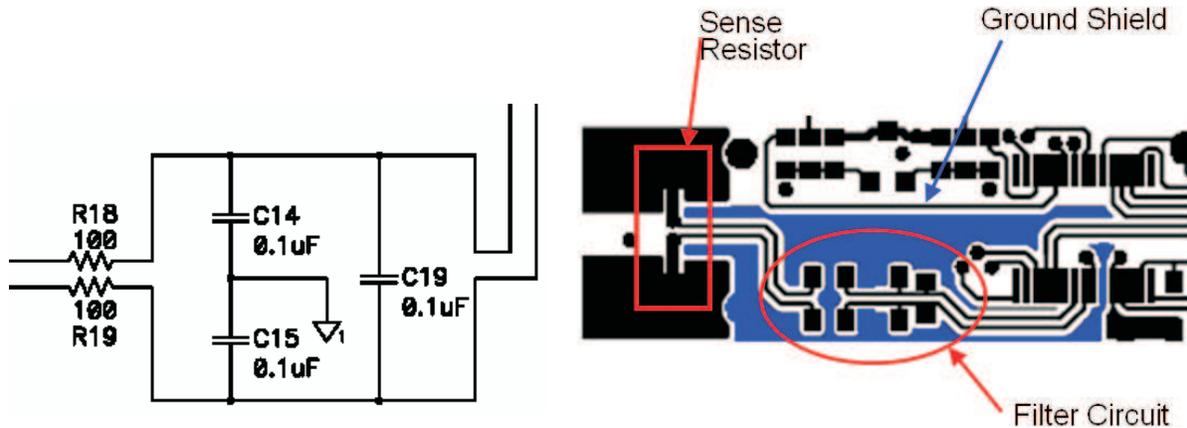
Figure 6. Differential Filter Components With Symmetrical Layout

ESD Spark Gap

Protect SMBus Clock, Data, and other communication lines from ESD with a spark gap at the connector. The pattern shown in Figure 7 is recommended, with 0,2-mm spacing between the points.
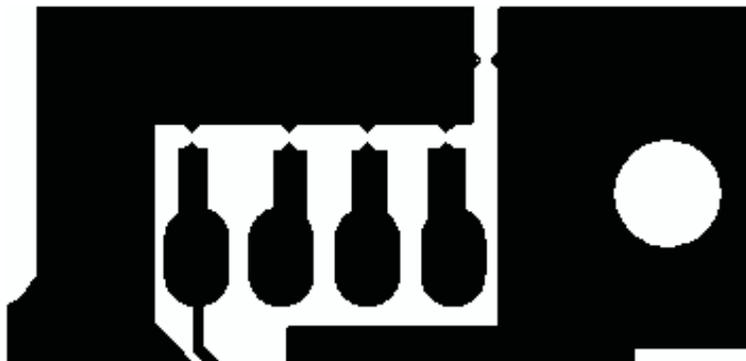
Figure 7. Recommended Spark Gap Pattern Helps Protect Communication Lines From ESD

Radio Frequency Interference

Normally, strong RF signals have no effect on gas gauge performance. However, any silicon structure can rectify RF signals, producing unwanted voltages and currents at critical nodes. In fact, any copper trace or battery connection has a frequency where it becomes an effective half-wave or quarter-wave receiving antenna. For example, the 1900-MHz cell phone band has a quarter wavelength of only 3,9 cm. A 3-watt cell phone, held next to a battery management circuit board, can induce significant errors under the right conditions. Full sweep RF testing for every new design is strongly recommended. Layout modification and/or the use of small bypass capacitors can usually mitigate the problem.

The most vulnerable node on the bq20z75/95 reference design is the SAFE output, which feeds into a signal diode, followed by a FET gate and shunt capacitor. This type of network demodulates an RF signal and can produce enough DC on the gate of the fuse ignition FET to actually ignite the chemical fuse. The solution is to keep the trace from the SAFE output to the diode as short as possible to reduce its effectiveness as an antenna. Alternately, both sides of the trace can be guarded with grounded copper.

Unwanted Magnetic Coupling

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultralow-current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement such as that shown in Figure 8, where the high-current section is on the opposite side of the board from the electronic devices. This is not possible in many situations due to mechanical constraints; nevertheless, every attempt should be made to route high-current traces away from signal traces, which enter the bq20z75/95 directly.

IC voltage references and registers can be disturbed and, in rare cases, damaged due to magnetic and capacitive coupling from the high-current path. Note that during surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as illustrated in Figure 9.
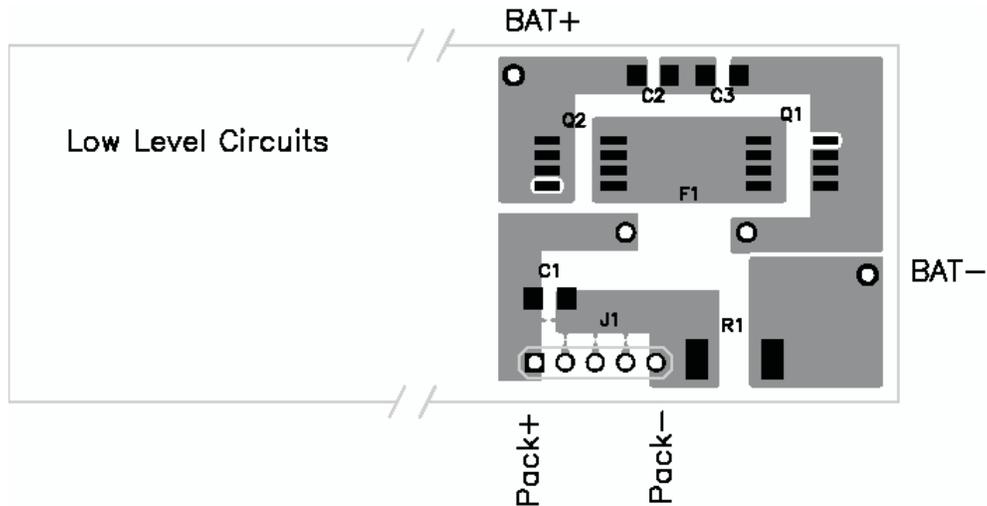
Figure 8. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity
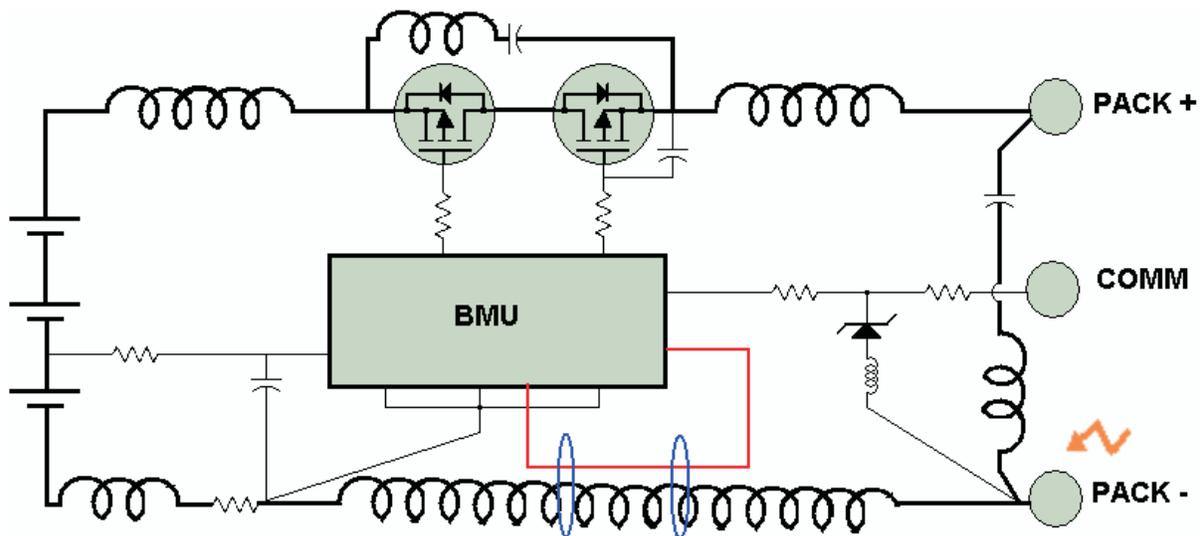
Figure 9. Avoiding Close Spacing Between High-Current and Low-Level Signal Lines

Thermal Considerations

Avoid thermal problems by placing the sense resistor, protection FETS, and high-current traces well away from the ICs.

Reference Schematic

Figure 10 is a reference schematic for a 4-series-cell bq20z95 battery management fuel gauge application. The bq20z75 schematic is similar, but has no LEDs.

Figure 10. bq20z95 4-Series-Cell Reference Schematic

IMPORTANT NOTICE