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bq77908A/bq77910A Series FET Considerations

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ABSTRACT

The bq77908A and bq77910A EVMs are a parallel FET circuit implementation of the devices but have component patterns which allow modification to a series FET configuration. While a modification as simple as moving Q7 to Q4 demonstrates the function of the topology, damage can result from over-current or short-circuit testing either with the EVM or circuits based on the simple schematic. This document describes the potential for damage through description and example waveforms. The reader can then use this information in determining a circuit for their specific application.

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1   Simple Circuit Modification

The Evaluation Modules (EVMs) for the bq77908A and bq77910A share the circuit topology and reference designators. Signal names may vary due to the part capabilities and pin definitions. Refer to the bq77908AEVM User's Guide (SLUU854) or the bq77910AEVM User's Guide (SLUU855) for circuit details. The description in this document is applicable to both EVMs and both the A and non-A suffix parts. The circuit will be referred to simply as "EVM".

The EVM is built, tested and delivered in a parallel FET configuration, but has various un-populated component patterns, some of which allow a simple-series FET configuration. For more information on FET configurations supported by the part, refer to the "Pack/System Connection Arrangements" section of the data sheets. The simplest change to the board is to remove the Q7 FET and install an appropriate FET at the Q4 position. The CHG- output is then used for the PACK- terminal. C27, C31, C34, C35 and D10 might also be removed. Figure 1 shows the area of the top side component modifications; refer to the EVM User's Guide for board details.
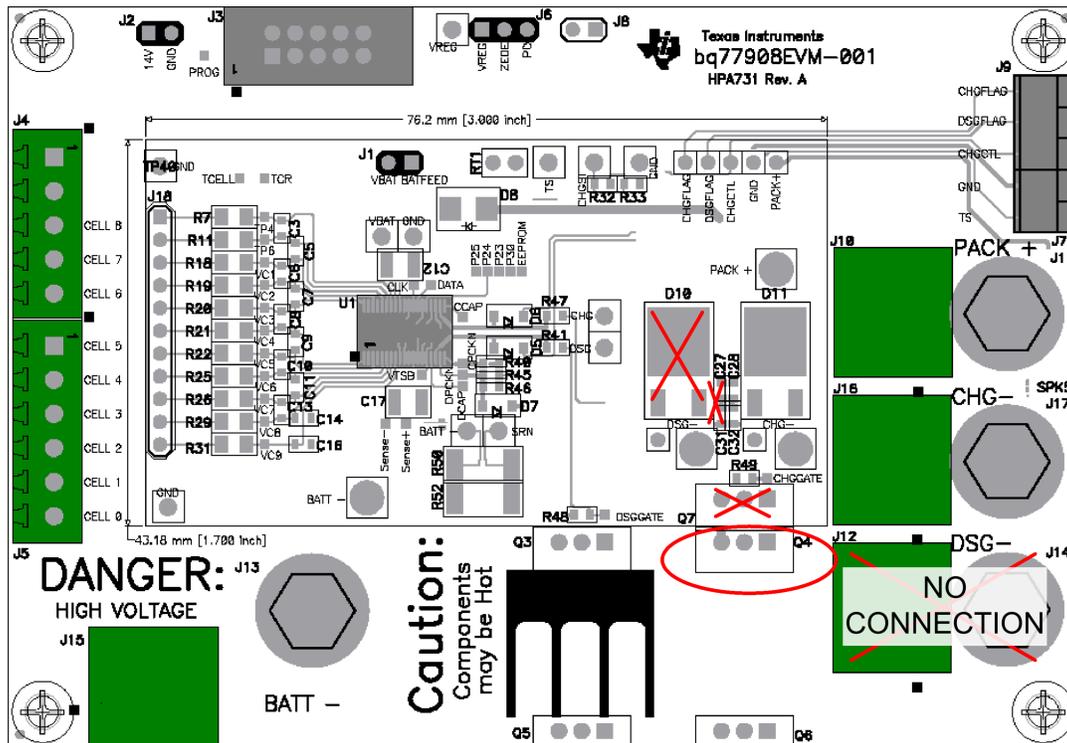

Figure 1. EVM Top Side Series-FET Modification Areas

Figure 2 shows the resulting simple-series FET circuit. The diagram also shows a functional representation of the driver circuit. The absolute maximum limits of the related pins are represented as internal zener diodes D90-D93 with the positive voltage limit shown. Negative voltage limits would forward bias the diodes and are not shown on the diagram, refer to the datasheet for limits. Damage to one of these internal diodes may show up as a short or open and may damage other internal circuitry.
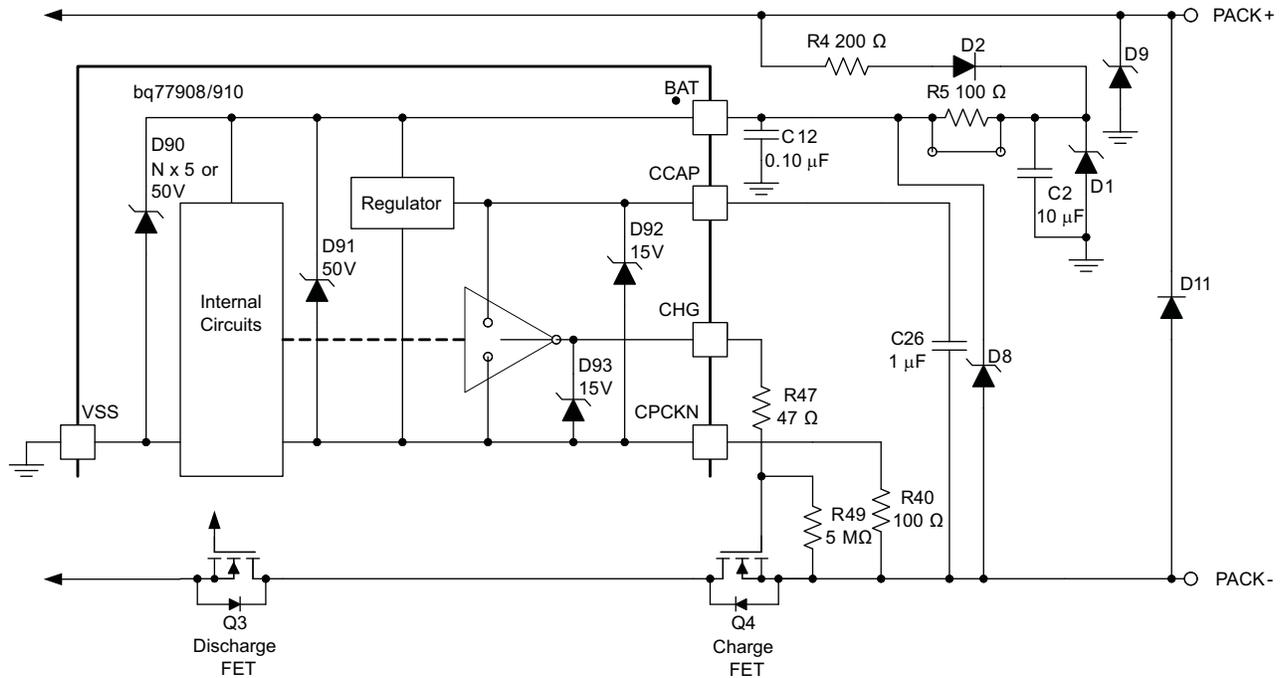
Figure 2. CHG Output Related Simple Series FET Circuit

This circuit modification allows demonstration of the functionality of the part, but may not provide adequate protection for the device pins. In the parallel configuration, the charge driver swings negative with respect to V_{SS} while with the series FET configuration, the driver swings both positive and negative with respect to V_{SS}. The transient on an over-current or short circuit discharge may be the most dynamic event in the circuit. Figure 3 represents the voltages during a current protection event. During the load the pack voltage is pulled down. The BAT pin voltage drops as the circuit operating current comes from C2. When the device protects and turns off the discharge FET, the system inductances cause the voltages on the PACK+ and PACK– to rise. Load inductance makes PACK– rise above PACK+ and D11 may conduct. BAT rises as C2 charges through various current paths. Figure 4 shows various current paths during the protection event. The CCAP pin voltage also rises due to C26 and it slowly discharges through the regulator to the BAT pin.
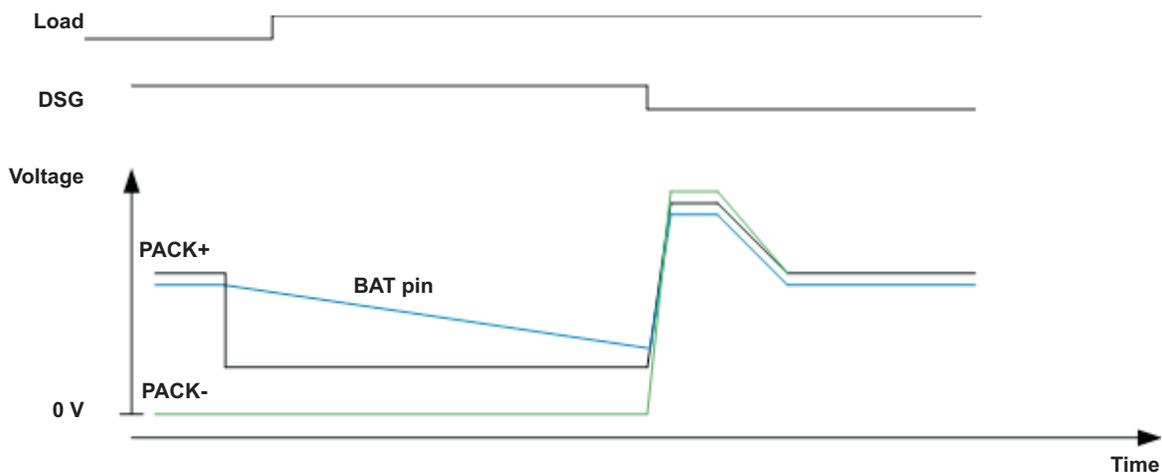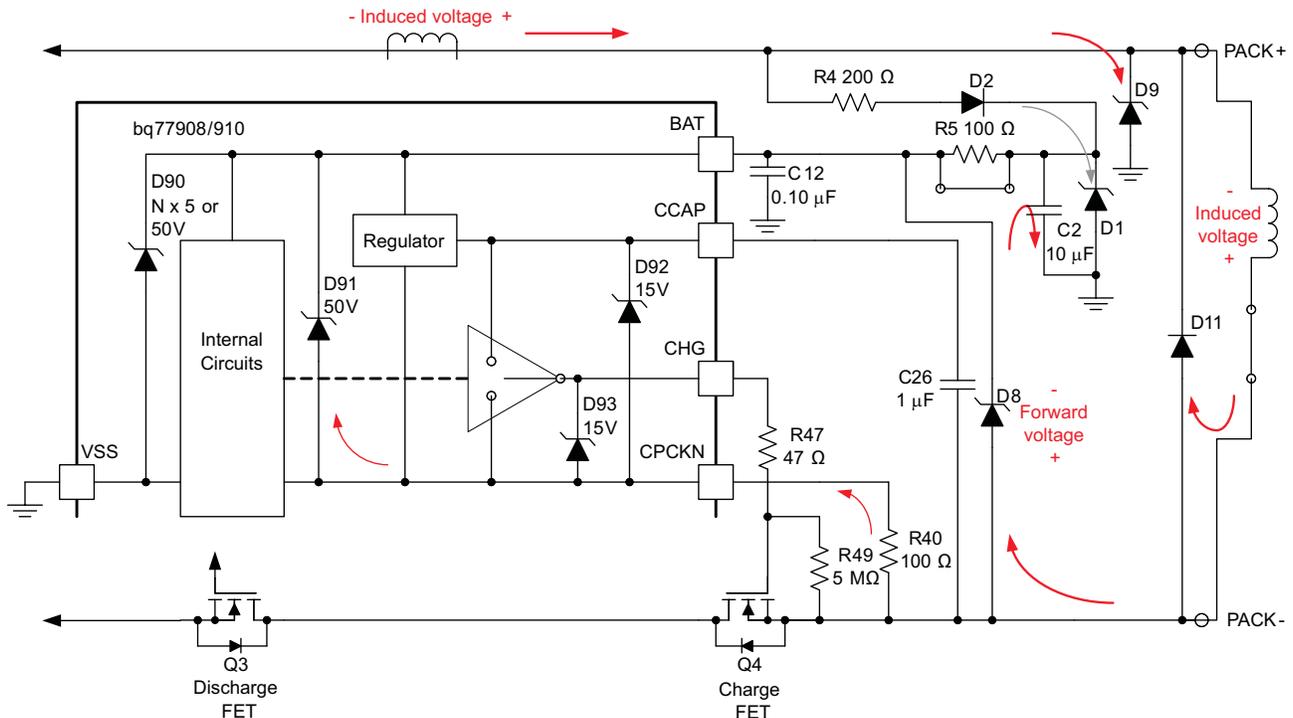

Figure 3. Expected Voltages with Current Protection

Figure 4. Currents During Current Protection

2 Fast Rise on BAT Pin

One problem which may be caused by the simple configuration is a fast rise in the BAT pin voltage. In the parallel configuration C2 will charge through R4 and D2. In the simple-series FET circuit, D8 charges C2 very quickly. This can result in a high dV/dt on the BAT pin and cause the part to malfunction. Figure 5 shows that after BAT rises at the short circuit protection, the VREG falls indicating the device has shut down. The figure also shows the importance of setting the scope scale and/or sample rate to see the detail of the transient. A capture with higher resolution, Figure 6 shows the transient on the PACK signals.
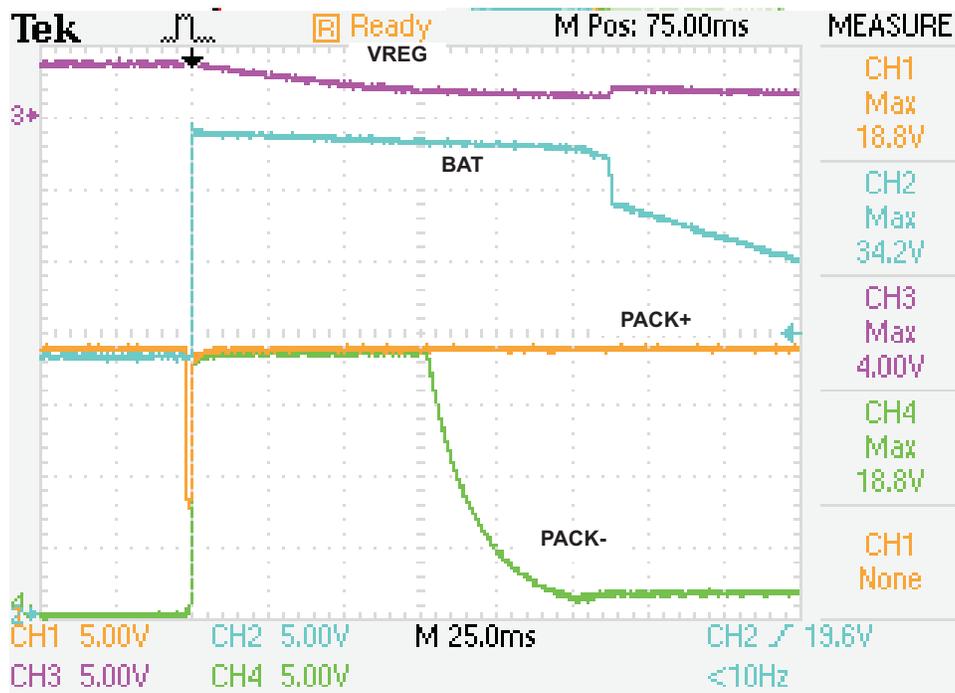
Figure 5. Device Shut Down on Current Protection
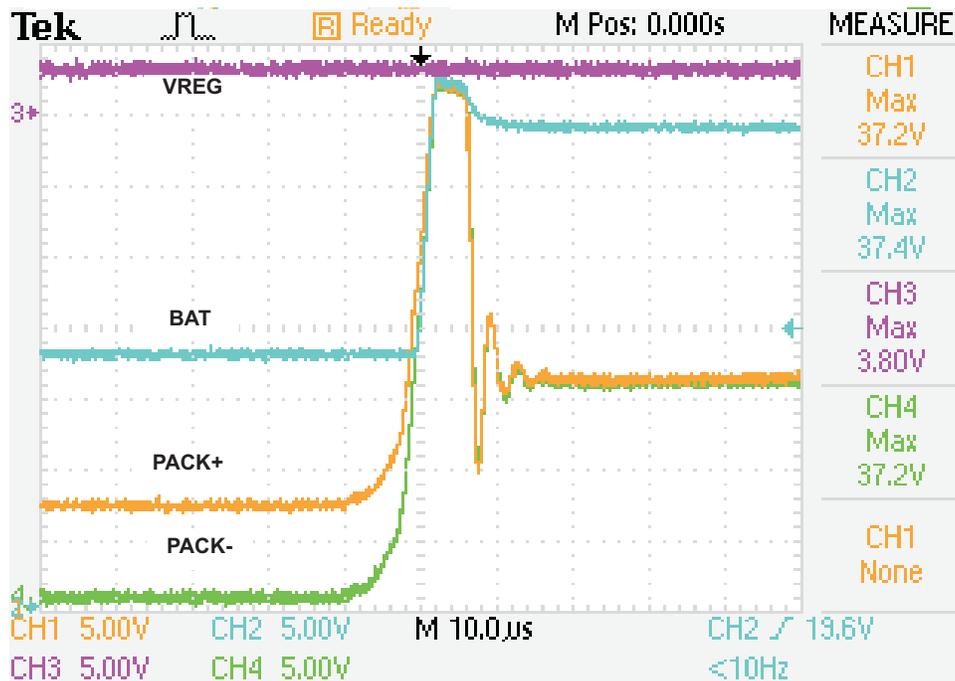
Figure 6. Transient at Current Protection

3 CHG Output Driver Reverse Voltage

As a result of the fast charge of C2, the current through D8 may be large and the forward voltage could be significant. If D9 clamped at a lower voltage, there would be less current into D1, however the BAT pin voltage can drop and a substantial current can flow to charge the C2 capacitor. Remember that diodes do have a slope compared to the typical ideal assumption as shown in Figure 7, and that their voltage will increase with current. The datasheet for the D8 used on the EVM shows a forward voltage of 3.5 V max at 30 A. This voltage can forward bias the diode, D91, in the part. R40 will limit the current into DPCKN, but the absolute maximum value is for voltage, not current. While Figure 6 does not clearly show a damaging voltage, parts have been reported damaged.
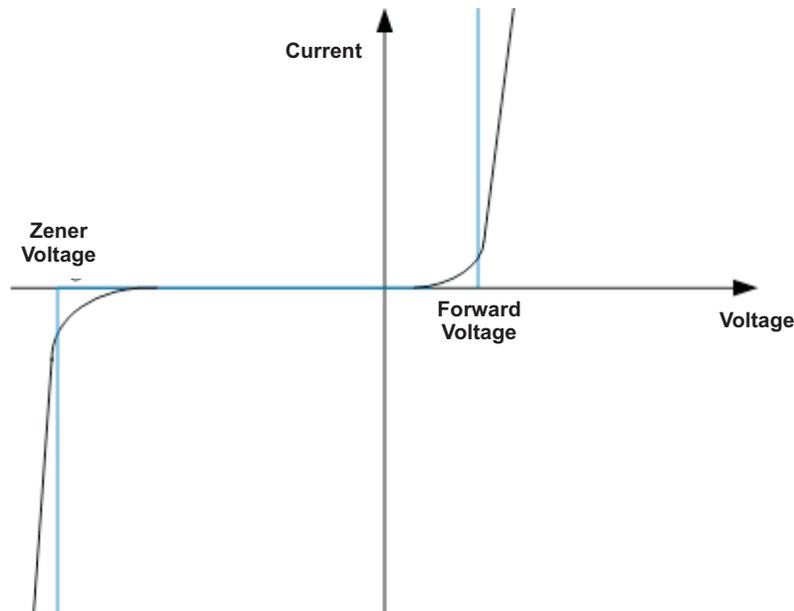
Figure 7. Diode Characteristic

4 R5 Shunt Not Propagated

The EVM provides R5 with a shunt to measure the current under different operating conditions. In some cases, R5 is copied onto an application board without the shunt. On the EVM the shunt may be left off from an earlier test. When the over-current protection trips with R5 in the circuit as shown in Figure 8, the BAT pin is not clamped by D1, but can rise substantially above it due to the voltage drop across R5, depending on the clamp voltage of D9. If the transient voltage is sufficient, D90 in the part could be damaged.
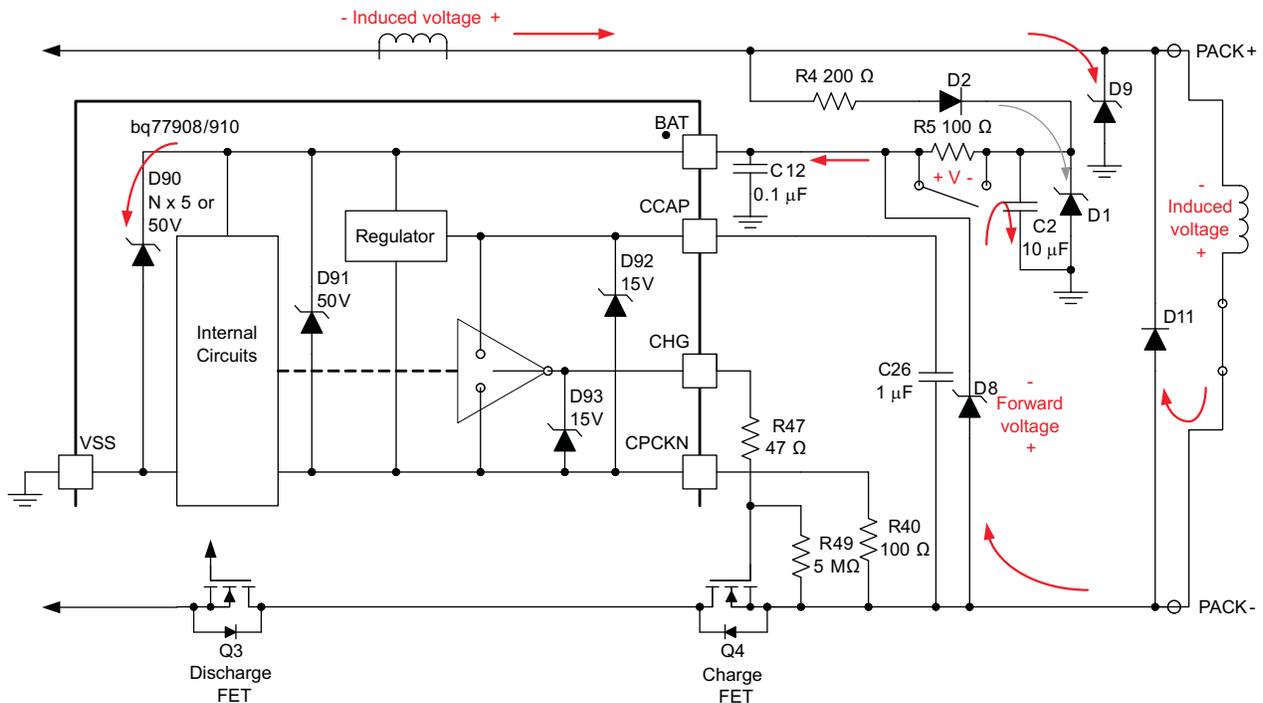
Figure 8. R5 in Circuit Allows BAT Voltage Rise

5   Risks Moving the Zener

One possibility to reduce the charge current would be to move the zener from D8 to the D21 position at the CPCKN pin as shown in Figure 9. However, this method allows charging to resume even when the protector has CHG turned off if the charger voltage rises sufficiently. The voltage drop across R40 will also be present at R49 and the charge FET can come on.
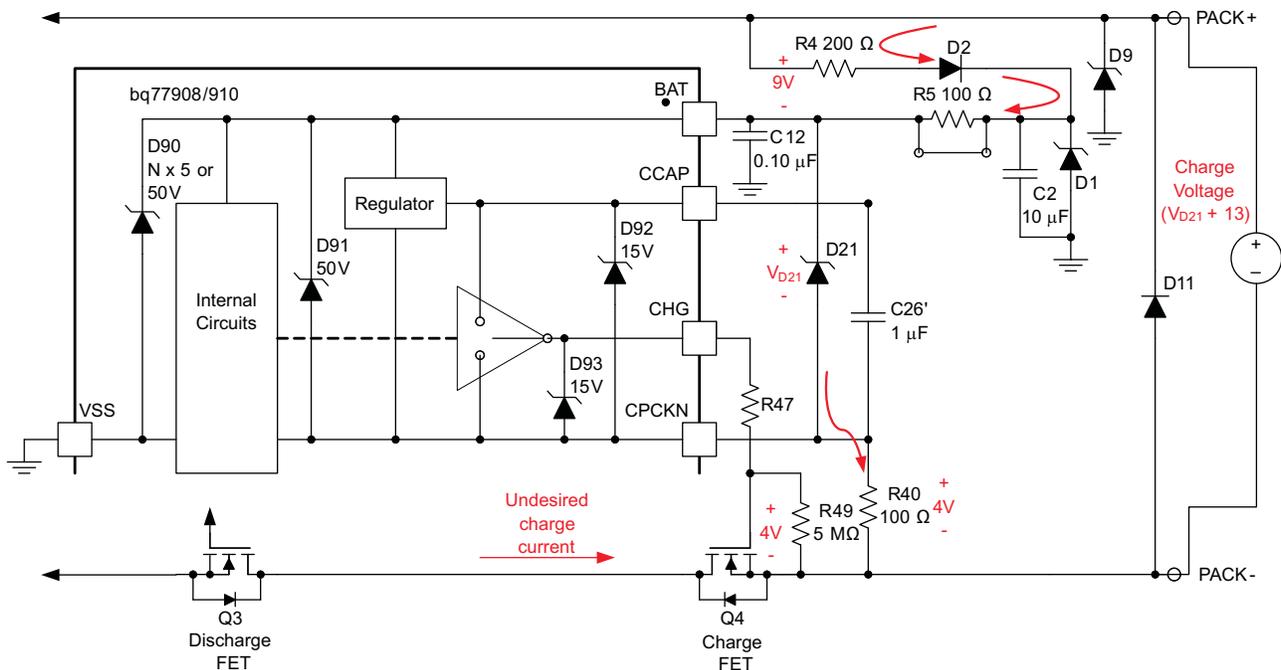
Figure 9. Undesired Charge From Moving Zener

6   Blocking Diodes

Adding diodes D20 and D21 as shown in Figure 10 prevents D8 from charging C2. During the transient, current flows through R40 and D21 to charge C2 in a parallel path with R4 and D2. D21 can be a Schottky-type diode. The voltage rise of BAT is slower and the part stays awake as shown in Figure 11 and Figure 12. Figure 12 also shows that the BAT voltage rises as CCAP discharges through the regulator, but this does not violate the abs max limits. However, the connection of C26 to PACK– causes the CCAP pin to be pushed up during the transient and although this happened without D21, the increased current through R40 will raise the voltage between CCAP and CPCKN putting D92 at risk of damage. Figure 13 shows the tendency of this voltage to rise although the peak voltage captured is not large and the part was not damaged in this test.
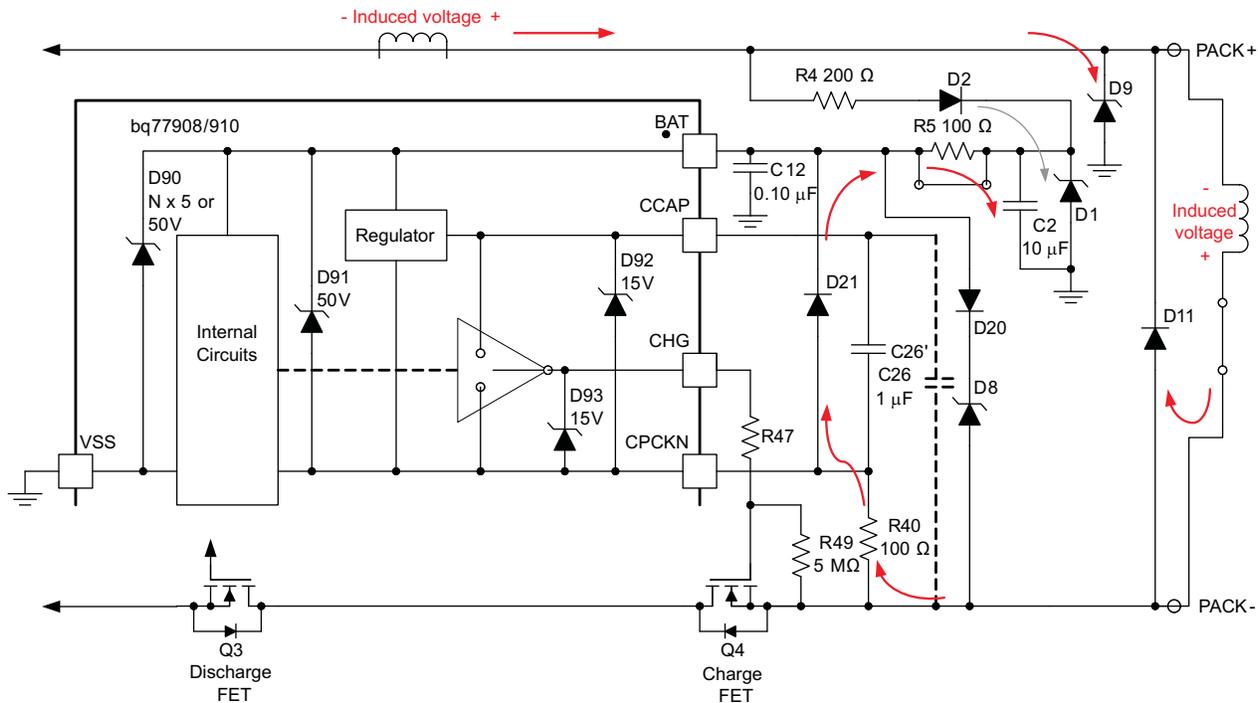
Figure 10. Blocking Diodes to Control BAT Rise
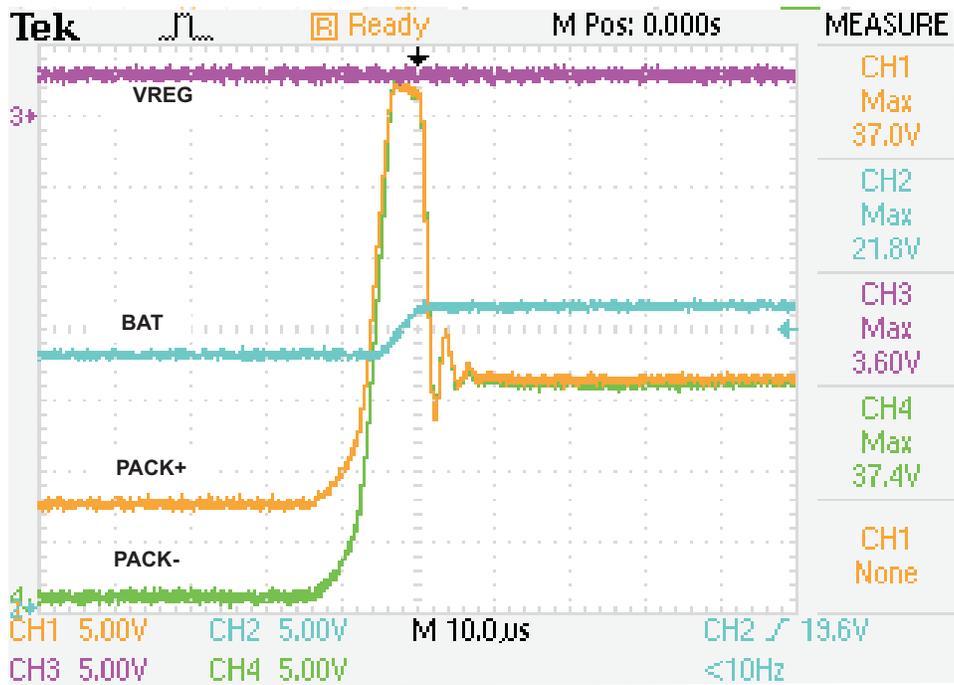
Figure 11. BAT Pin Rise Slowed by Blocking Diodes
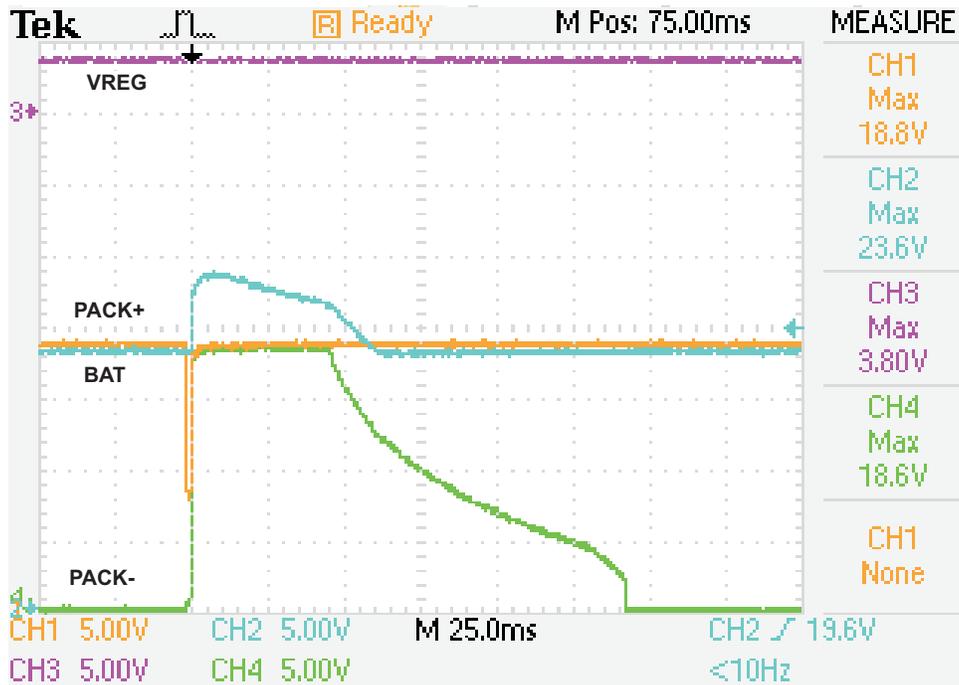
Figure 12. Device Remains on With Current Protection With Blocking Diodes
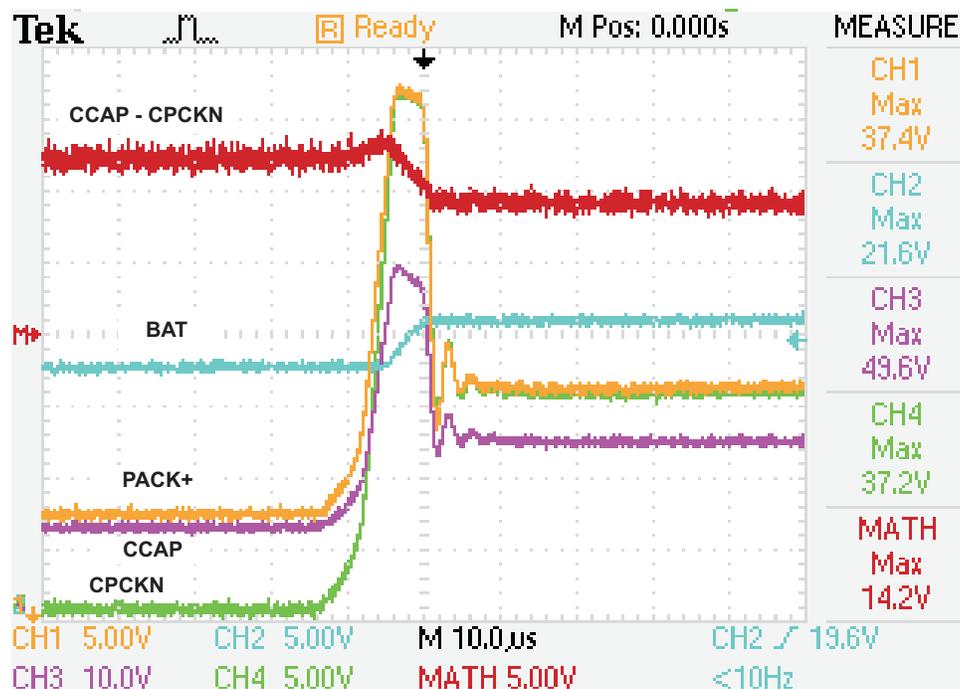
Figure 13. C26 Placement Gives CCAP-CPCKN Peak

7   CCAP Capacitor Location and Drive Impact

Moving C26 to the C26' location allows the capacitor to maintain a constant voltage between the CCAP and CPCKN pins. However, moving C26 to C26' adds another consideration with the CHG output switching and its effect on the pin voltages. When the CHG output turns on, it is effectively connected to the CCAP pin. When it turns off, CHG is effectively connected to CPCKN. The EVM's R47 small default value of 47 Ω allowed fast switching of the charge FET, but fast switching is not necessarily needed or desired for the charge FET. With the original C26 placement, at turn on instantaneous current flows from C26 into CCAP, through the driver, out the CHG pin, through R47 and the FET capacitance and returns to C26 at the PACK– net. With the capacitor moved to C26', the turn-on current now flows through R40 too and can push the CPCKN low with respect to BAT as shown in Figure 14.
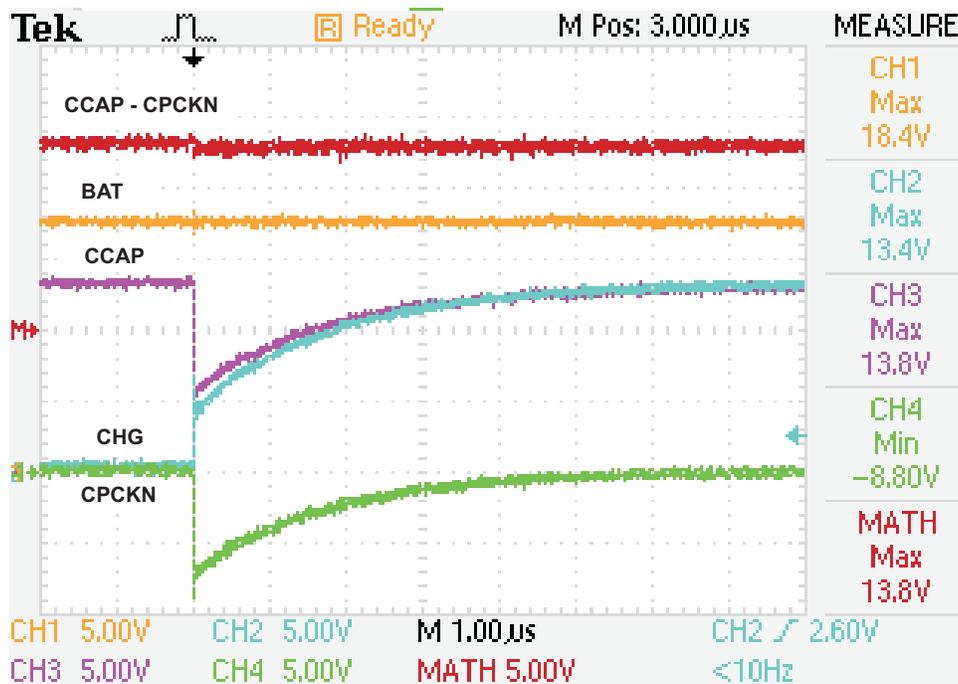
Figure 14. CPCKN Driven Down by FET Turn on With Fast Switching and C26'

The drop in CPCKN voltage is not a concern for D92 since C26' will maintain the voltage, but if the device is turning on the charge FET with a high charger voltage, having CPCKN go low could be a risk to D91. Simply moving D8 to the D21 position is not desired since the voltage across R40 would tend to turn on the charge FET again with a higher charger voltage. Increasing the switching time of the charge FET by making R47 1 kΩ, significantly reduces the effect of the CPCKN voltage drop at turn on as shown in Figure 15. Depending on the application circuit, changing the R47 value may be sufficient or additional limit diodes may be desired.
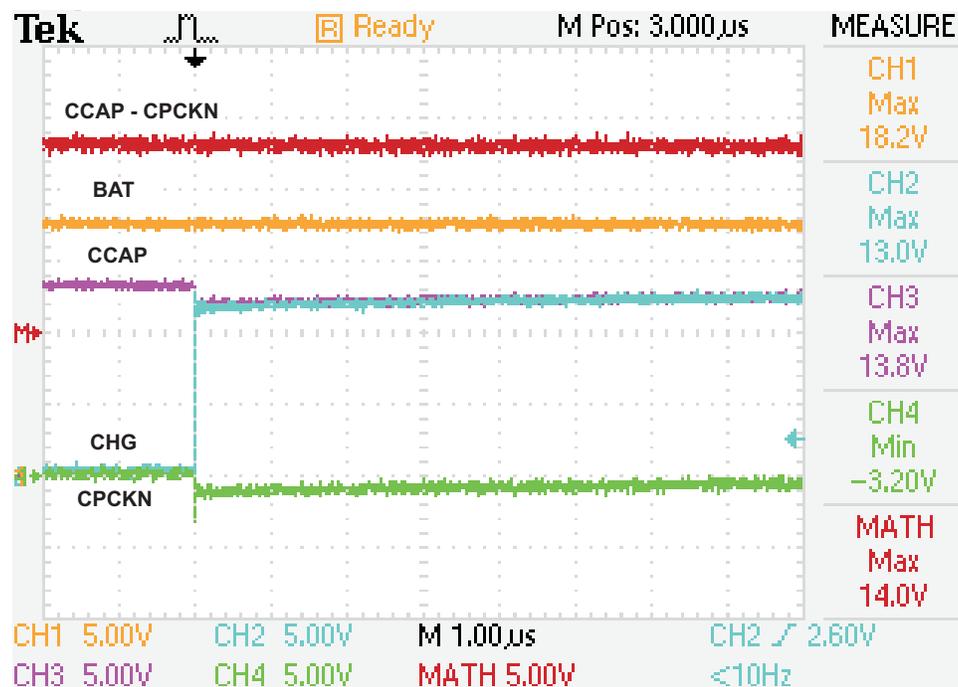
Figure 15. CPCKN Excursion Reduced by 1 kΩ – R47

Turn off of driver is not typically a concern. In both cases current flows through both R40 and R47. With the original C26 placement, the CCAP – CPCKN voltage is reduced momentarily. With the C26' placement CCAP–CPCKN is maintained by the capacitor and the voltage shifts up with the voltage across R40.

The result with the Figure 16 modified circuit with D20, D21, C26' position, and R47 = 1 kΩ is shown in Figure 17, Figure 18 and Figure 19. During short circuit, BAT rises slowly so the device does not turn off and CCAP-CPCKN does not peak.
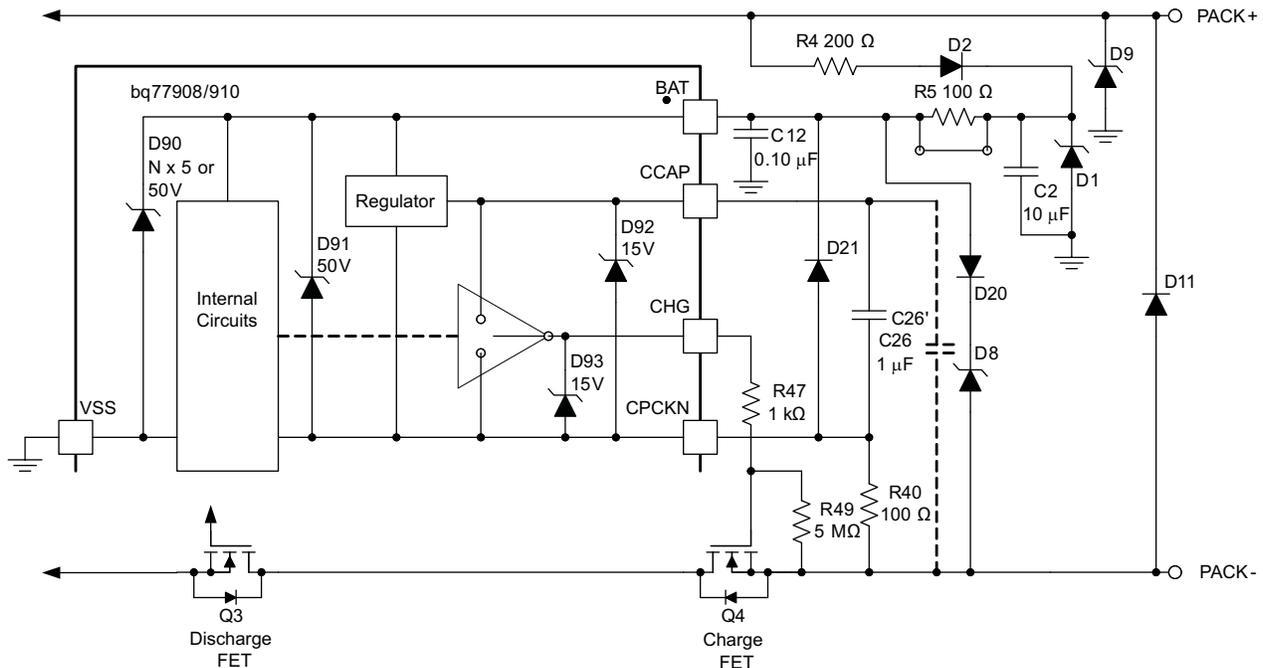
Figure 16. Test implementation
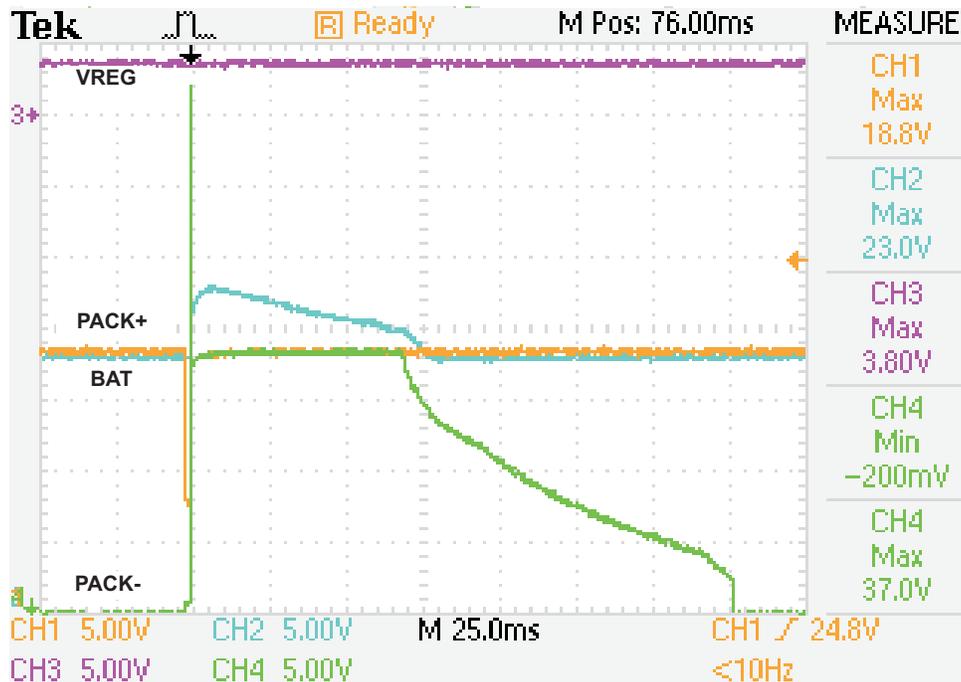
Figure 17. BAT Pin Rises Slowly in Transient
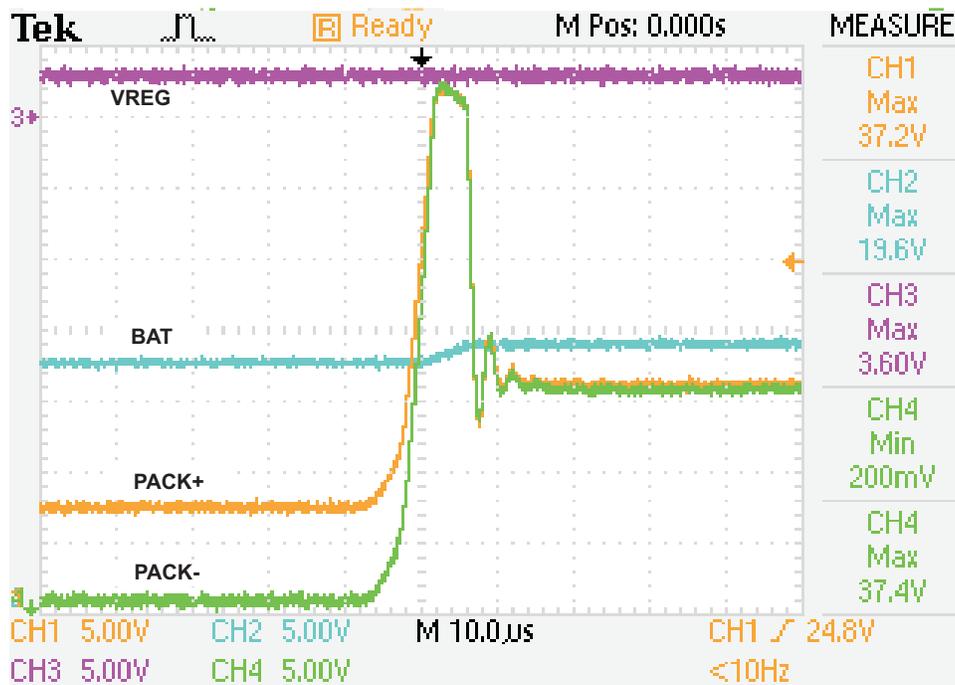
Figure 18. Device Stays On
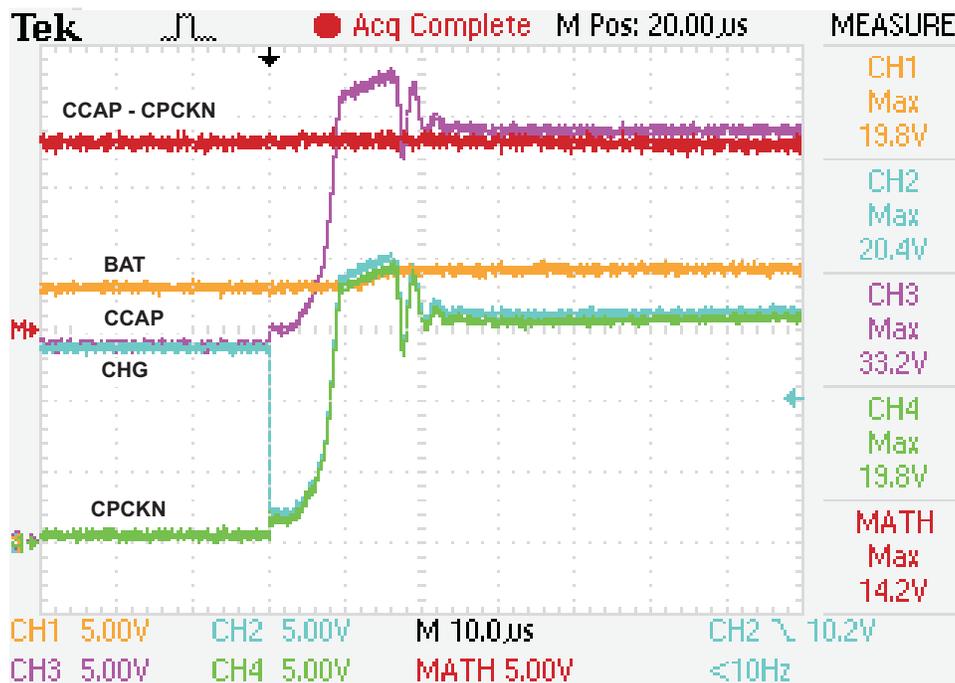
Figure 19. CCAP During Current Protection Turn Off

In conclusion, the simple-series FET circuit may need modification for a specific design to avoid damaging parts or mis-operation due to system current protection transients. The blocking diode technique and discussion here may help the reader determine a circuit configuration for their application to avoid detrimental effects of the system transients. For particularly severe transient environments, or reverse charger requirements, it may be beneficial to explore circuits which use the CHG output as a logic signal to control an external FET driver which can accept voltages beyond the range of the IC.

IMPORTANT NOTICE