Getting Started with the BQ76925

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ABSTRACT

The BQ76925 is combined with a microcontroller to build a complete battery management system. Key aspects of the system include the microcontroller, filtering and protection, communications, measurement, and power management. Important considerations are discussed that aid in the design of the hardware and firmware of the battery management system.

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1 System Overview

Figure 1 presents the major features of a typical battery management system (BMS) built around the BQ76925 analog front-end (AFE). The BQ76925 provides three analog outputs that allow a microcontroller to easily monitor cell voltage, current, and temperature. Cell voltages are level-shifted, scaled, and multiplexed to the VCOUT pin. Cell current is monitored through a sense resistor placed in series with the cell stack. The voltage across the sense resistor is amplified and driven to the VIOUT pin. The VTB pin supplies a switched bias to stimulate a thermistor network for temperature measurement.

A microcontroller (MCU) with an analog-to-digital converter (ADC) is required to complete the measurement system. The MCU accesses registers in the AFE through an I²C interface to control the AFE functions and state. The AFE supplies a low-drift reference for accurate A/D conversions. Calibration constants (also called correction factors) stored in the AFE ROM are read by the MCU and applied to the ADC results to achieve high measurement accuracy.

The BQ76925 supplies a 3.3-V regulated output for powering the MCU. The AFE also includes integrated cell balancing FETs that are under MCU control. Finally, the on-board comparator from the AFE signals an overcurrent condition to the MCU for fast fault response.

In a typical application, the BMS monitors the battery cell parameters to ensure they are within safe operating limits. If a fault is detected, action is taken such as opening a switch or blowing a fuse to interrupt the current path. The BMS can also track and report the battery state of charge (SOC).
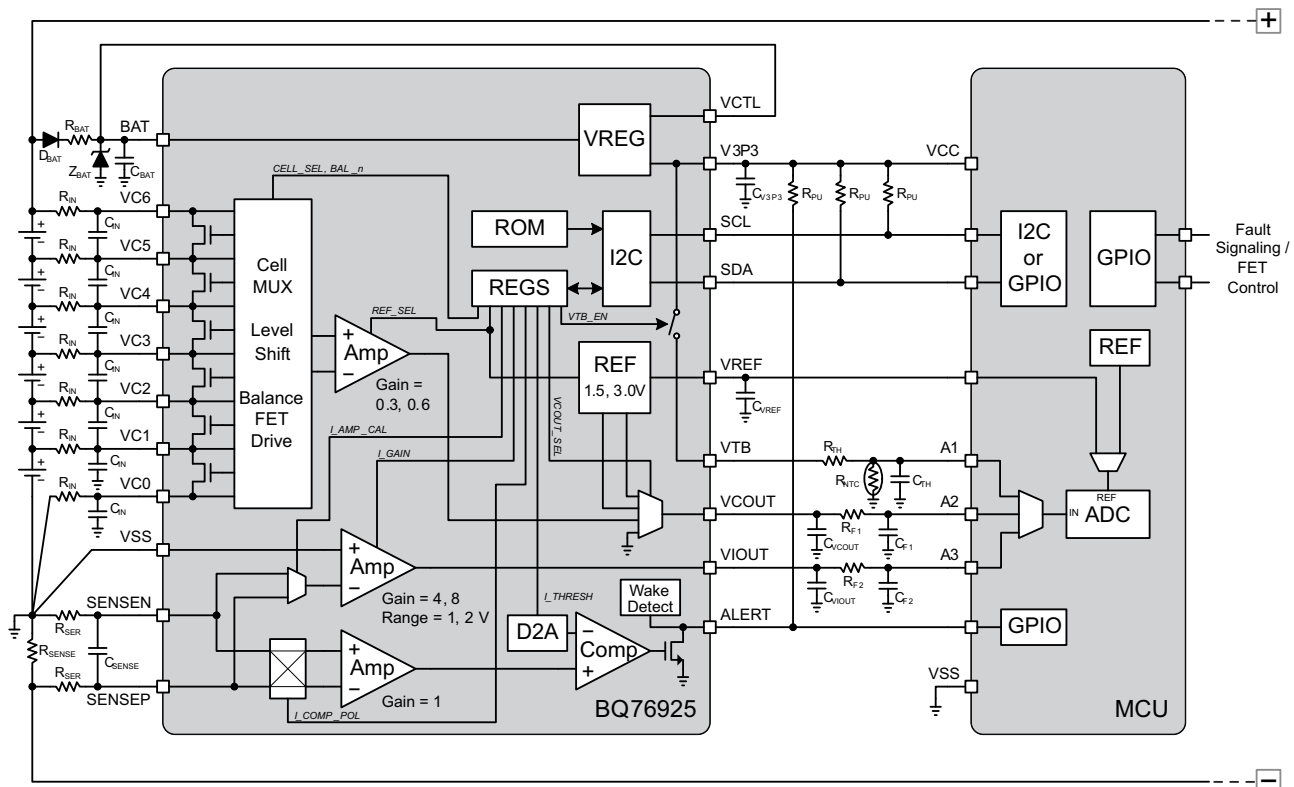

Figure 1. Example Battery Management System Using the BQ76925

1.1 MCU Requirements

Minimum MCU requirements depend on the required functionality of the BMS as well as the particular features and capabilities of the selected core architecture and MCU family. In this context, some general recommendations are given.

Devices that meet and exceed the following recommendations can be found in TI's MSP430 MCU products. One example is the MSP430G2132 from the MSP430 value line.

1.1.1 Analog-to-Digital Conversion

For most applications, a 10-bit ADC is adequate. A minimum of three input channels are needed to measure cell voltage, current, and temperature. For improved accuracy, a fourth input channel can be used to calibrate the ADC during manufacturing of the BMS.

An external reference input that allows the BQ76925 to supply the ADC reference voltage may also help to improve measurement accuracy. The data sheet specification of the voltage reference from the BQ76925 must be compared against the internal reference voltage specification of the MCU to determine if using the AFE reference is advantageous.

1.1.2 Communications

The MCU must provide standard-mode I²C master transmit and receive functionality. This may be satisfied using either a dedicated hardware peripheral or a software (bit-banged) implementation, and must be capable of supporting single-byte read and write. Multi-master, repeated start, and clock stretching support are not required if the BQ76925 is the only device on the bus.

1.1.3 Flash Memory

Minimum requirements for code space depend on the level and complexity of functionality implemented in the firmware. Efficiency of the code size depends on additional factors including processor core architecture, compiler, coding language, and coding style.

As a point of reference, example code implementing basic communication, measurement, and fault detection functions (including correction factor calculations) has been developed in C to run on an MSP430 16-bit RISC MCU using less than 2 kB of flash memory.

1.1.4 Other Features

General-purpose IOs can be used to control current interrupting switches (for example power FETs) or otherwise communicate fault information outside of the MCU (for example, to an attached appliance or charger). Additionally, they can be used to control LEDs to indicate battery SOC.

A timer peripheral is useful for scheduling events and timing faults. A watchdog timer is important for fail-safe operation.

2 External Filtering and Protection

Figure 1 shows a number of external filtering components. These components are important for various reasons such as transient protection, current limiting, and stability as discussed in the following sections. Recommended component values can be found in the *BQ76925 Host-controlled Analog Front End Data Sheet*.

2.1 Input Filters

TI recommends input filters for the supply (BAT), cell voltage (VC0 – VC6), and current sensing inputs (SENSEN, SENSEP). A key function of these filters is to protect the BQ76925 from large transients caused by switching of the battery load. For example, in applications where the battery is used to drive a motor, motor switching can induce peak voltages more than twice the DC voltage of the battery. In these cases, the absolute maximum ratings of the AFE must not be exceeded.

Load switching can also cause the battery voltage to drop well below its DC level, close to zero in some applications. A second function of the filter on the BAT pin is to avoid an unintentional reset of the AFE by keeping the BAT voltage from falling below the shutdown level when the battery voltage suddenly drops. Figure 1 shows that a blocking diode can be added in series with the input filter on BAT to further ensure that the BAT pin does not drop with the battery voltage.

Take care when using a blocking diode so that repeated peak transients do not eventually pump up the filter capacitor beyond the voltage ratings of the AFE. If this situation occurs, a clamp can be added in parallel with the filter capacitor.

A second function of the input filter resistance on VC0 – VC6 is to set and limit the balancing current. The internal balancing FET resistance is typically less than 10 Ω, so additional external resistance is required to keep the balancing current below the maximum allowed in the data sheet.

Figure 1 shows a differential input filter network for the cell inputs although many of the data sheet diagrams show single ended filters on each input. Single ended provides an easier calculation of the filter time constant, but the differential filter helps keep the inputs within abs max limits for differential voltages. The connection of VC1 filter capacitor to ground rather than VC0 keeps VC0 from being pushed below ground during sudden heavy loads on the battery.

2.2 Output Filters

For stability, output capacitors are required on V3P3, VREF, VCOUT, and VIOUT. See the *BQ76925 Host-controlled Analog Front End Data Sheet* for recommended values. These capacitors also function as bypass capacitors in response to MCU internal switching and A/D conversion operations.

Additional filtering on VCOUT and VIOUT (see R_{F1}, C_{F1} and R_{F2}, C_{F2} in Figure 1) may be desired to smooth out noisy signals prior to A/D conversion. Figure 2 shows this concept. The final output response is a combination of the input filtering, AFE response and output filtering. Note that filtering introduces a time delay that must be considered when computing overall system response time.
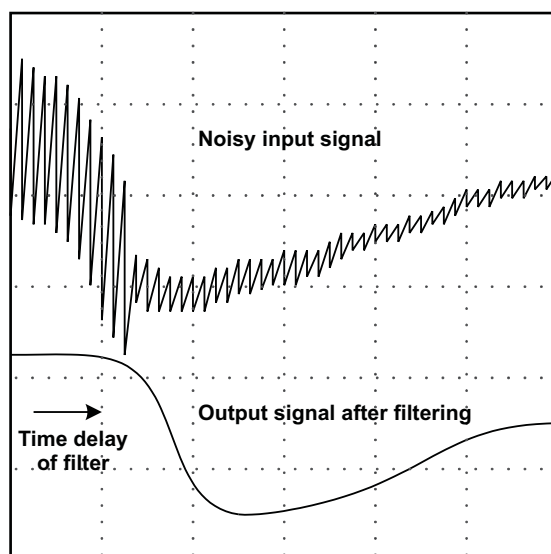

Figure 2. Filtering a Noisy Input Signal

3 Communications System

The BQ76925 is controlled through a standard-mode I²C interface. All control is accomplished by reading and writing the AFE registers. The AFE register space spans 32 addresses. The device slave address and register address are combined, so that each register occupies one slave address on the I²C bus. Therefore, the BQ76925 register space appears as 32 logical devices on the bus.

Figure 3 and Figure 4 show a write and read transaction. The byte labeled Address refers to the combined address, which is further described in the following section.
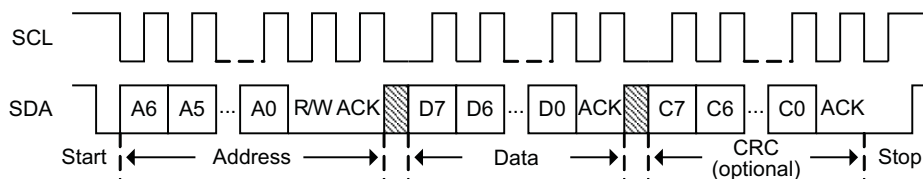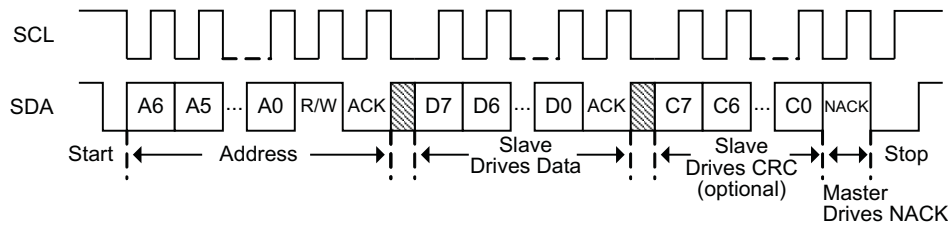

Figure 3. I²C Write Transaction

Figure 4. I²C Read Transaction

3.1 Addressing

The combined slave and register address is calculated from the BQ76925 group address and the register absolute address. The 4-bit group address is set to a fixed value of 0x4. The 5-bit register addresses are numbered from 0x00 – 0x1F. The 7-bit combined address is calculated by shifting the group address left by three and adding the register address. Table 1 shows the combined address for all named BQ76925 registers.

Table 1. Combined Addresses for all Named BQ76925 Registers

REGISTER ADDRESS	REGISTER AME	COMBINED ADDRESS
0x00	STATUS	0x20
0x01	CELL_CTL	0x21
0x02	BAL_CTL	0x22
0x03	CONFIG_1	0x23
0x04	CONFIG_2	0x24
0x05	POWER_CTL	0x25
0x07	CHIP_ID	0x27
0x10	VREF_CAL	0x30
0x11	VC1_CAL	0x31
0x12	VC2_CAL	0x32
0x13	VC3_CAL	0x33
0x14	VC4_CAL	0x34
0x15	VC5_CAL	0x35
0x16	VC6_CAL	0x36
0x17	VC_CAL_EXT_1	0x37
0x18	VC_CAL_EXT_2	0x38
0x1B	VREF_CAL_EXT	0x3B

3.2 CRC Generation

Figure 3 and Figure 4 show that an optional CRC byte can accompany each transaction. The host can request a CRC on a read transaction at any time simply by reading one additional byte following the data byte. To enable CRC checking on write, the CRC_ENA bit in the CONFIG_2 register must be set. When this bit is set, the BQ76925 must receive a valid CRC on each write transaction or else the transaction is discarded.

There are a number of techniques for computing a CRC. Pseudocode for calculating the CRC-8 used in the BQ76925 (polynomial = $x^8 + x^2 + x + 1$) is given in the following:

```
char poly = 0x07                  # 8-bit polynomial
char crc = 0x00                   # Initialize 8-bit CRC
for each byte in message:         # Loop over all bytes in the message
    crc = crc xor byte
    for index = 1 to 8:           # Loop over all bits in the CRC
        if crc > 127:             # If msb is set, shift left and XOR with poly
            crc = crc << 1
```

```
        crc = crc xor poly
else:                           # Else just shift left
        crc = crc << 1
```

4   Measurement System

The measurement system is at the heart of the BMS. Overall performance depends on the performance of the BQ76925, the reference voltage, and the ADC of the MCU.

4.1   Correction Factor Concept

One method to achieve high accuracy in analog integrated circuits is to provide on-chip trim circuits to correct for variations in the manufacturing process. During factory testing of the device, the trim is adjusted until the specified performance is achieved. The trim circuits are typically controlled by on-chip fuses or non-volatile memory.

The BQ76925 takes a similar, yet different, approach to achieve high accuracy. Device performance is measured in the factory and trim information is stored in non-volatile memory. However, rather than correct the device performance using on-chip circuitry, the trim information is made available to the MCU so that the correction can be applied to the A/D measurement results in firmware. The trim information is referred to as correction factors.

4.1.1   Representation in Non-Volatile Memory

A separate gain and offset correction factor is determined for each cell voltage channel as well as the reference voltage. The correction factors are stored as 5-bit and 6-bit integer values in the 2 complement format. The units for gain correction are 0.1%, and the units for offset correction are in mV.

The correction factors do not occupy contiguous register space, so two registers must be read in order to assemble each correction factor. For example, the four least significant bits of the offset correction factor for channel 1 are stored in the VC1_CAL register at positions D4 to D7, while the most significant bit is stored in the VC_CAL_EXT_1 register at position D7. Table 2 and Table 3 show the assembled correction factors for each channel in terms of register field names. See the *BQ76925 Host-controlled Analog Front End Data Sheet* for the register map.

Table 2. Assembled Integer Gain Correction Factors

CHANNEL	NAME	GAIN CORRECTION
Reference Voltage (VREF)	VREF_GC	(VREF_GC_4 << 4) + VREF_GAIN_CORR
Cell 1 Voltage (VC1)	VC1_GC	(VC1_GC_4 << 4) + VC1_GAIN_CORR
Cell 2 Voltage (VC2)	VC2_GC	(VC2_GC_4 << 4) + VC2_GAIN_CORR
Cell 3 Voltage (VC3)	VC3_GC	(VC3_GC_4 << 4) + VC3_GAIN_CORR
Cell 4 Voltage (VC4)	VC4_GC	(VC4_GC_4 << 4) + VC4_GAIN_CORR
Cell 5 Voltage (VC5)	VC5_GC	(VC5_GC_4 << 4) + VC5_GAIN_CORR
Cell 6 Voltage (VC6)	VC6_GC	(VC6_GC_4 << 4) + VC6_GAIN_CORR

Table 3. Assembled Integer Offset Correction Factors

CHANNEL	NAME	OFFSET CORRECTION
Reference Voltage (VREF)	VREF_OC	(VREF_OC_5 << 5) + (VREF_OC_4 << 4) + VREF_OFFSET_CORR
Cell 1 Voltage (VC1)	VC1_OC	(VC1_OC_4 << 4) + VC1_OFFSET_CORR
Cell 2 Voltage (VC2)	VC2_OC	(VC2_OC_4 << 4) + VC2_OFFSET_CORR
Cell 3 Voltage (VC3)	VC3_OC	(VC3_OC_4 << 4) + VC3_OFFSET_CORR
Cell 4 Voltage (VC4)	VC4_OC	(VC4_OC_4 << 4) + VC4_OFFSET_CORR
Cell 5 Voltage (VC5)	VC5_OC	(VC5_OC_4 << 4) + VC5_OFFSET_CORR
Cell 6 Voltage (VC6)	VC6_OC	(VC6_OC_4 << 4) + VC6_OFFSET_CORR

4.1.2   Calibration Application

The stored calibration is for 6 cells. When cell count is reduced from 6 cells but cell 6 is used for the top cell as discussed in the section about cell amplifier headroom under the BAT voltage drop in the *BQ76925 Host-controlled Analog Front End Data Sheet*, it operates over a different input range for the 1.4 to 4.4 V per cell range. The stored calibration may not be suitable for that cell. Use additional or different correction if needed.

4.2   *Reference Voltage*

The A/D conversion results are directly proportional to the reference voltage. Therefore, performance of the reference voltage is very important for measurement accuracy.

$$V_{ADC} = \frac{V_{REF} \times (ADC\ Count)}{(Full\ Scale\ Count)}$$

(1)

Depending on the capabilities of the MCU, the ADC reference voltage can be the MCU supply voltage, internally generated within the MCU or provided externally on an MCU input pin. Generally speaking, an internally generated reference voltage provides better performance than simply using the supply voltage, and the highest performance can be achieved using an external reference.

Initial accuracy at room temperature and temperature drift are key parameters that determine the performance of a voltage reference. The BQ76925 reference has excellent temperature performance of ±40 ppm/°C, which means that the voltage varies by a maximum of 0.004% for each change of 1° from room temperature. For example, at a temperature of 50°C the reference voltage varies by at most (50 – 25) × 0.004 = 0.1%.

The BQ76925 nominal reference voltage (VREFNOM) is selected to be 1.5 or 3.0 V by writing to the REF_SEL bit in the CONFIG_2 register. Using the supplied gain correction factor (GCVREF) and offset correction factor (OCVREF), the initial value of the reference voltage can be calculated to within 0.1%.

$$V_{REF,INIT} = \left(1 + GC_{VREF}\right) \times V_{REF,NOM} + OC_{VREF}$$

(2)

For example, let VREF_GC = –4, VREF_OC = 7, and VREF,NOM = 3.0 V. Equation 3 through Equation 5 show to calculate the initial value of the reference voltage.

$$GC_{VREF} = VRE\_GC \times 0.001 = -0.004$$ (3)

$$OC_{VREF} = VREF\_OC \times 0.001 = 0.007$$ (4)

$$V_{REF,INIT} = (1 + (-0.004)) \times 3.0 + 0.007 = 2.2995\ V$$ (5)

4.3   *Voltage Measurement*

The MCU selects a cell input for measurement on VCOUT by writing to the CELL_SEL bits in the CELL_CTL register. The selected cell input is level shifted to VSS reference and scaled by a nominal gain $G_{VCOUT,NOM}$ = 0.3 (REF_SEL = 0) or 0.6 (REF_SEL = 1).

Equation 6 shows that the measured value of VCOUT is calculated from the V_{ADC} result using $V_{REF,INIT}$ as the reference voltage.

$$VCOUT = V_{ADC}\left(V_{REF} = V_{REF,INIT}\right) = \frac{ADC\ Count}{Full\ Scale\ Count} \times \left[\left(1 + GC_{VREF}\right) \times V_{REF,NOM} + OC_{VREF}\right]$$

(6)

To achieve the specified output accuracy, offset and gain correction factors must be applied to the ADC result to give the corrected value of VCOUT.

$$VCOUT_{CORR} = \left(VCOUT + OC_{VCOUT}\right) \times \left(1 + GC_{VCOUT}\right)$$

(7)

It is important to understand the difference between VCOUT and VCOUT$_{CORR}$. VCOUT is the measured value at the VCOUT pin. This corresponds to the actual voltage on the VCOUT pin to the accuracy limits of the ADC and reference voltage. VCOUT$_{CORR}$ represents what the VCOUT voltage *should* have been equal to if the cell amplifier had no gain and offset errors. Then, to calculate the cell input voltage, VCOUT$_{CORR}$ is simply divided by $G_{VCOUT,NOM}$.

Equation 8 shows Equation 6 substituted in Equation 7.

$$VCOUT_{CORR} = \left(\frac{ADC\ Count}{Full\ Scale\ Count} \times \left[\left(1 + GC_{VREF}\right) \times V_{REF,NOM} + OC_{VREF} \right] + OC_{VCOUT} \right) \times \left(1 + GC_{VCOUT}\right) \tag{8}$$

Continuing the previous voltage reference example, assume a 10-bit A/D conversion has resulted in a count of 818 for a measurement of the cell 1 voltage. Let VC1_GC = 2 and VC1_OC = –3.

Equation 9 shows how to calculate the corrected value of VCOUT.

$$GC_{VCOUT} = VC1\_GC \times 0.001 = 0.002$$

$$OC_{VCOUT} = VC1\_OC \times 0.001 = -0.003$$

$$VCOUT_{CORR} = \left(2.995 \times \frac{818}{1023} + (-0.003) \right) \times (1 + 0.002) = 2.397\ V \tag{9}$$

Equation 10 shows how to calculate the corresponding cell input voltage.

$$VC1 = \frac{VCOUT_{CORR}}{G_{VCOUT,NOM}} = \frac{2.397}{0.6} = 3.995\ V \tag{10}$$

4.3.1   Firmware Implementation

Implementing Equation 8 in a MCU can present some difficulties because it contains division and floating point values which tend to consume large amounts of code space. However, by multiplying Equation 8 through by Full Scale Count **x** 106, the equation can be transformed to avoid division and contain only integers.

$$VCOUT_{CORR} \times Full\ Scale\ Count \times 10^6 =$$

$$\left[ADCCount \times \left(V_{REF,NOM} \times \left(1000 + VREF\_GC\right) + VREF\_OC \right) + Full\ Scale\ Count \times VCn\_OC \right]$$

$$\times (1000 + VCn\_GC) \tag{11}$$

Equation 11 requires 32-bit integers for intermediate results, but the final result can be truncated to 16 bits (for example, by right shifting 16 times) with negligible loss of accuracy. When comparing the final result to preset fault limits, the limit values must be scaled in the same way as $VCOUT_{CORR}$ (that is, multiplied by Full Scale Count **x** 106 and truncated to 16-bits if the final result was also truncated).

4.4   *Current Measurement*

The differential voltage across the sense resistor is measured in two steps. In the first step, the voltage at SENSEN is measured with respect to VSS. In a well-designed system where VSS and SENSEN are star connected to the same point, this first step can be regarded as a calibration step that need only be repeated infrequently. In the second step, SENSEP is measured with respect to VSS. The MCU then calculates the differential voltage by subtracting the SENSEP measurement from the SENSEN measurement.

When the SENSEN and SENSEP voltages are 0 (corresponding to 0 current), the VIOUT amplifier has an offset of approximately 1 V (REF_SEL = 0) or 2 V (REF_SEL = 1). This allows both positive and negative currents to be measured as a positive voltage. The exact value of VIOUT under the 0 current condition is not important because it cancels out in the calculation of V_{SENSE}. Note that the amplifier is inverting, so that when SENSEP is greater than 0, the VIOUT voltage goes down. The drive current of the amplifier is low and the amplifier design makes the output rise faster than the fall.

The MCU selects the SENSEN or SENSEP measurement by writing the I_AMP_CAL bit in the CONFIG_1 register. The current amplifier gain G_{VIOUT} is set to 4 or 8 by writing the I_GAIN bit also found in the CONFIG_1 register. Equation 12 shows how to calculate the voltage across the sense resistor.

$$V_{SENSE} = \frac{[VIOUT(SENSEN)\text{-}VIOUT(SENSEP)]}{G_{VIOUT}}$$

$$= \frac{ADC\ Count_{SENSEN} - ADC\ Count_{SENSEP}}{Full\ Scale\ Count \times G_{VIOUT}} \times V_{REF,INIT}$$

$$= \frac{ADC\ Count_{SENSEN} - ADC\ Count_{SENSEP}}{Full\ Scale\ Count \times G_{VIOUT}}$$

$$\times \left[(1 + GC_{VREF}) \times V_{REF,NOM} + OC_{VREF} \right] \qquad (12)$$

Similar to the transformation made for the cell voltage calculation, the current calculation can be transformed for easy implementation in an MCU.

$$V_{SENSE} \times Full\ Scale\ Count \times G_{VIOUT} \times 1000$$

$$= (ADC\ Count_{SENSEN} - ADC\ Count_{SENSEP})$$

$$\times \left[(1000 + VREF\_GC) \times V_{REF,NOM} + VREF\_OC \right] \qquad (13)$$

4.5 *Temperature Measurement*

The MCU writes to the VTB_EN bit in the POWER_CTL register to switch the thermistor bias on and off. When the thermistor is biased, a voltage measurement can be taken from which temperature can be derived according to the characteristics of the thermistor. Equation 14 shows that the calculation of the thermistor voltage follows the form of the voltage and current measurements.

$$V_{THERM} = \frac{ADC\ Count}{Full\ Scale\ Count} \times \left[(1 + GC_{VREF}) \times V_{REF,NOM} + OC_{VREF} \right] \qquad (14)$$

Equation 15 shows that similar transformations can be made for easy implementation in a MCU.

$$V_{THERM} \times Full\ Scale\ Count \times 1000$$

$$= ADC\ Count \times \left[(1000 + VREF\_GC) \times V_{REF,NOM} + VREF\_OC \right] \qquad (15)$$

4.5.1 Ratiometric Temperature Measurement

The thermistor bias VTB is a switched version of the 3.3-V regulated voltage at V3P3. Therefore, variations on V3P3 affect the temperature calculation. This dependence can be removed by placing a fixed resistor divider in parallel with the thermistor network. Using an additional input to the ADC, the voltage of the resistor divider can be measured so that VTB can be calculated and its tolerance taken out of the temperature calculation.

Figure 5 shows such an arrangement. The resistors R_A and R_B ideally has a tight tolerance and low temperature coefficient. Their values need to be chosen so that the maximum output current of the VTB pin is not exceeded and the divided voltage is in the range of the ADC measurement.
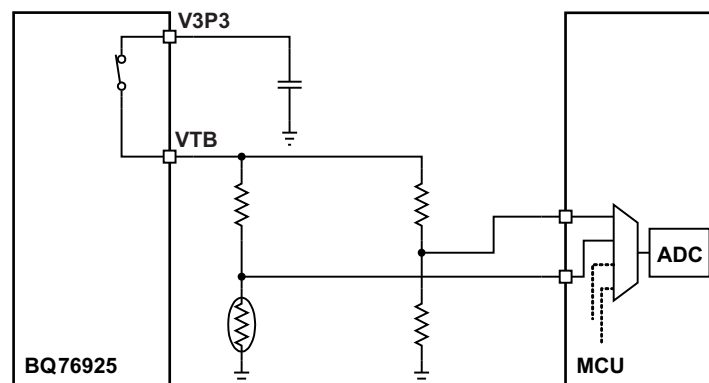

Figure 5. Ratiometric Temperature Measurement

5   Power Management

Power can be managed in the BQ76925 by disabling functions that are not used or when they are idle. The POWER_CTL register contains enable bits for five functions:

- Current comparator
- Current amplifier
- Cell voltage amplifier
- Themistor bias
- Reference voltage

See the *BQ76925 Host-controlled Analog Front End Data Sheet* for how these bits affect current consumption of the device.

The BQ76925 can also be shutdown to a very-low current state (< 1.5 µA) under control of the MCU by writing a 1 to the SLEEP bit in the POWER_CTL register. In this state, all functions and features, including the 3.3 V regulated output at the V3P3 pin, are shut off. After the voltage at the V3P3 drops to about 0 V, the ALERT pin wakes up the device if it is pulled high. The I²C interface pins do not hold up the regulator voltage if the lines are driven high, but if the MCU holds up the lines the pull up resistors to V3P3 may hold up the voltage and prevent shutdown.

6   Low Dropout (LDO) Regulator

The LDO regulator in the BQ76925 must be used with an external pass transistor when load currents are higher than 4 mA, as described in the data sheet. The external pass transistor must be high gain to ensure stability. ZXTP25040DFH and IRLML9303 are example transistors. R_{VCTL} must be 200 kΩ. TI recommends Z1 to protect the gate-source or base emitter of the pass transistor.

The LDO is designed with a particular loop bandwidth for a given external capacitor. With its low-loop bandwidth, the regulator can respond slowly to a high-pulse load. A larger C_{V3P3} reduces the output delta from load switching, but increases the regulator settling time. Another artifact of the circuit with the external transistor occurs when the C_{V3P3} is increased to, for example, 10 µF, the gain bandwidth product of the error amplifier circuit is reduced. With very-low quiescent load during startup, the V3P3 voltage shoots to higher than 3.3 V and takes time to settle. If more quiescent output current is drawn during startup, the output rises to a higher voltage but settles faster to the right voltage. No failure of the BQ76925 happens due to this behavior if the voltages are kept within the BQ76925 limits. Attached circuitry must be checked for maximum and minimum voltage limits.

The BAT filter selection also has an effect on the regulator. R_{VCTL} and the transistor emitter or source must be connected directly to the BAT pin. The LDO load current flows through R_{BAT} so its size is limited. A smaller R_{BAT} improves load regulation. A larger filter on BAT improves the line regulation by reducing transients. The ideal filter has a low R_{BAT} and high C_{BAT}.

Figure 6 shows an R_{V3P3} - C_{V3P3-2} filter. Adding this filter helps isolate the load from the V3P3 transients caused by the load and transients on BAT.
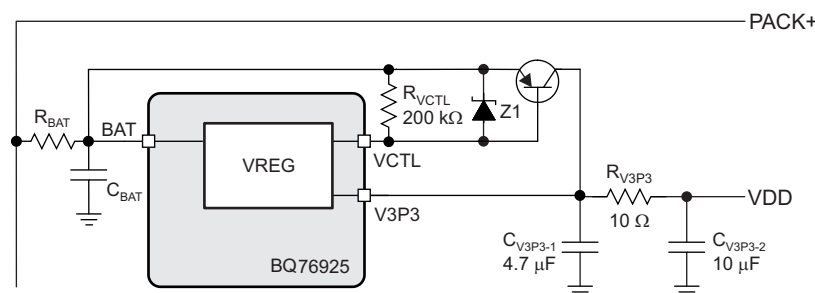

Figure 6. V3P3 Load Filter

7 Balancing and Open Cell Detection

The BQ76925 balancing system operates under control of the MCU. Balancing does not automatically duty cycle like some AFEs. The MCU is free to set the duty cycle for balancing and measurement. It can also measure during balancing, which enables the open-cell detection method described in the data sheet. The designer must note that an open wire during balancing can result in the VCn inputs exceeding the absolute maximum cell input voltage range of the cell input VCn. Any open wire test must be run at an appropriately low voltage to avoid stressing the BQ76925.

8 References

- *BQ76925 Host-controlled Analog Front End Data Sheet*
- *MSP430G2x32, MSP430F2x02 Mixed Signal Microcontroller Data Sheet*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (March 2019) to B Revision **Page**

- Changed ZXTP2504DFH part number to ZXTP25040DFH in the *Section 6* 11

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