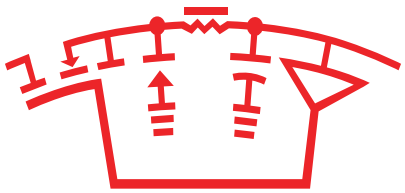

Power Supply Design Seminar

Tips, Tricks and Advanced Applications of Linear Regulators

TEXAS INSTRUMENTS

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Topic 5
Stephen Ziel
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This topic explores some common tips and tricks to maximize the performance of your low-dropout (LDO) regulators and covers how to improve noise, the power-supply rejection ratio (PSRR), thermal dissipation and system efficiency. I will also discuss more complex topics such as parallel LDOs, including brand-new material on multiple-input-single-output LDO designs. This topic is valuable for anyone who is looking to maximize performance in their LDO designs or systems.

Introduction

Linear and LDO regulators are a very common power-supply architecture, owing to their simplicity and low cost. As engineers continue designing more linear regulators into their systems, questions inevitably arise on how to maximize performance for each particular application. How can you optimize your LDO for noise-sensitive applications? Can you improve the thermal performance of your regulator? How much input voltage is enough?

Sometimes the questions are more complex. What if you need higher performance than even the best LDOs on the market? How can you parallel your LDOs to obtain more output current, achieve less noise, or spread the thermal dissipation? How many parallel LDOs would you need to do this?

What if you need higher power on your output than what any of your input supplies provide? Can you use LDOs to combine power from multiple sources to deliver to a single load?

If you have ever asked any of these questions, then this topic is for you.

Linear Regulators vs. Switching Converters

There are two types of power supplies: linear regulators and switching converters. A switching converter places the switching elements either fully on and off, and filters the resulting waveform to generate a regulated output voltage (V_{OUT}) (see **Figure 1**). A linear regulator places a metal-oxide semiconductor field-effect transistor (MOSFET)-based pass element in the saturation region, or a bipolar junction transistor-based pass element in the active region, to control V_{OUT} (see **Figure 2**).

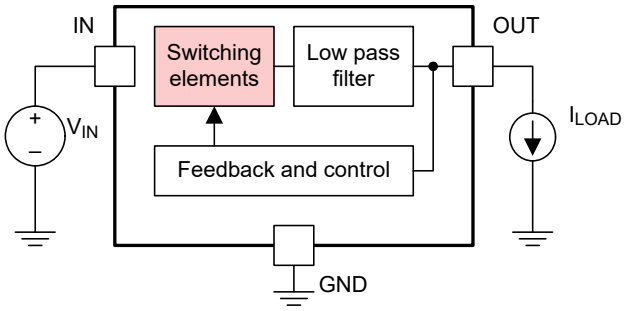


Figure 1. *Switching converter architecture.*

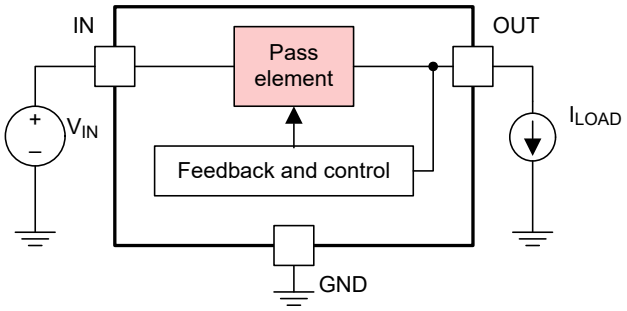


Figure 2. *Linear regulator architecture.*

Linear regulators are often cheaper, simpler and generate less output noise than switching converters, while switching converters can be more efficient at higher loads (see **Figure 3**). Classic linear regulators require the input voltage (V_{IN}) to be at least 1 V higher than V_{OUT} for the device to properly regulate V_{OUT}. This difference between V_{IN} and V_{OUT}, also called the headroom voltage, significantly degrades the linear regulator's efficiency.

A special class of linear regulators, called LDO regulators, exists to achieve high efficiency (see **Figure 4**). LDOs enable a headroom voltage well under 1 V; some high-end LDOs only require 50 mV to 100 mV of headroom. Most linear regulators designed today are LDOs, and for that reason, I'll use the term LDOs in this paper.

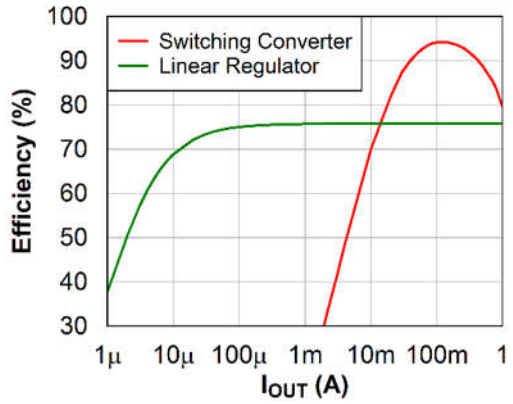


Figure 3. *Efficiency comparison of a switching converter vs. a linear regulator.*

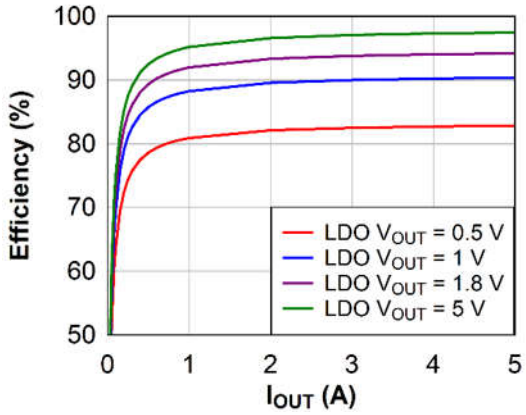


Figure 4. *LDO efficiency rises with V_{OUT} for a constant headroom voltage.*

LDO Regulator Structure and Characteristics

The basic structure of an LDO includes a reference voltage, error amplifier, pass device (usually a MOSFET) and feedback resistors (see **Figure 5**). There may also be input and output capacitors and a filter network between the reference voltage (V_{REF}) and error amplifier.

During operation, the feedback resistors sense and divide V_{OUT}. The error amplifier magnifies the difference between V_{REF} and the sensed V_{OUT}, and adjusts the pass device to tightly control V_{OUT}.

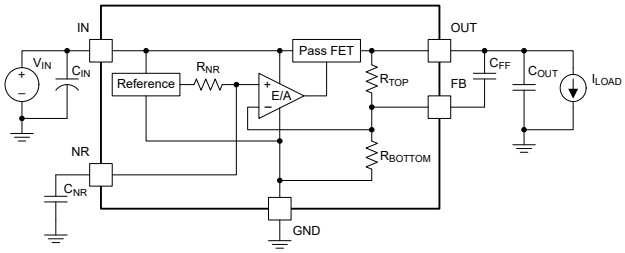


Figure 5. *Linear regulator block diagram.*

LDO characteristics include:

- The dropout voltage (V_{DO}). V_{DO} is the minimum headroom voltage required for the LDO to regulate V_{OUT} under DC operating conditions. The small VDO of modern LDOs enable >90% efficiency when V_{OUT} > 1 V.
- Power dissipation (P_D). LDOs dissipate power across the pass device, requiring adequate thermal management to prevent the junction temperature from exceeding the allowable limits listed in the device-specific data sheet.
- Noise and PSRR. The low output noise of an LDO is a combination of the internal (or intrinsic) noise that the LDO generates and the external (input) supply noise that the LDO filters. Intrinsic noise is dominated by noise from V_{REF}, magnified by the error amplifier. The LDO uses internal feedback loops to maintain a steady V_{OUT}, despite variations on V_{IN}. The LDO's ability to filter input supply noise is its PSRR.
- Quiescent current (I_Q). I_Q is the current necessary to run the internal circuitry of the LDO. Minimizing this current is important to maximizing regulator efficiency under light loads.
- Stability. LDOs use internal feedback loops to maintain stability under a wide range of operating conditions listed in the data sheet. Modern LDOs are stable under no-load conditions, with minimal headroom voltage, using low equivalent series resistance (ESR) capacitors with a wide range of output capacitance. Some LDOs are inherently stable without any additional components, but most require at least one output capacitor to prevent the LDO from oscillating.

- Turnon time. The total turnon time is the time it takes an LDO to reach its minimum regulation, from the moment power is instantaneously applied to V_{IN} or the LDO is enabled using an enable pin.

For more details on I_Q, stability and turnon time, see [1-8].

Intrinsic Noise in LDOs

Data sheets express LDO noise in two different ways [9]:

- A spectral noise density (in microvolts per square root hertz) vs. frequency plot.
- A root-mean-square (RMS) noise voltage measured in RMS microvolts within the electrical characteristics table.

The RMS noise voltage equals the spectral noise density integrated over a specific frequency range (often 10 Hz to 100 kHz or 100 Hz to 100 kHz) (see Figure 6). You can compare the noise performance of various LDOs using the published RMS noise voltage. If your application is sensitive to a specific range of frequencies, it is better to review those frequencies in the spectral density plot.

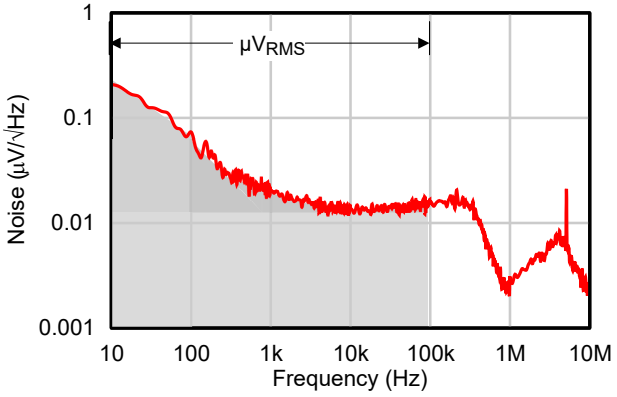


Figure 6. *Noise spectral density vs. total integrated noise.*

When designing LDOs into noise-sensitive environments, it helps to understand what does not impact the output noise of the LDO. Typically, output current (see Figure 7) and V_{IN} (see Figure 8) will not affect the noise performance of the LDO. While the load current does affect the noise curves of some ultra-low-I_Q LDOs, the vast majority of LDOs on the market will follow Figure 7.

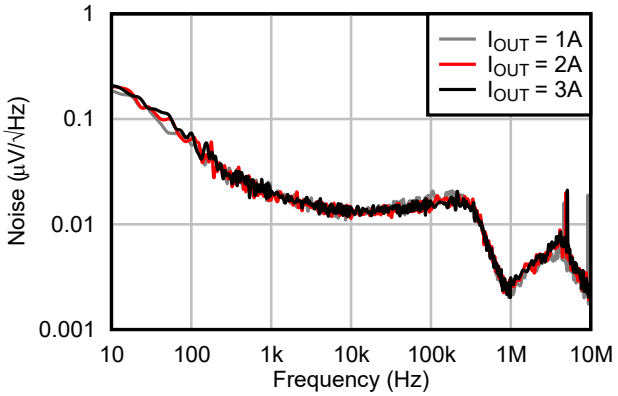


Figure 7. *LDO noise is insensitive to load current.*

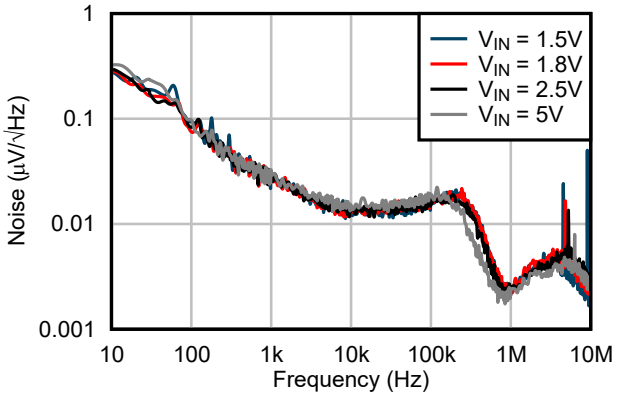


Figure 8. *LDO noise is insensitive to variations of V_{IN} above V_{DO}.*

Very large output capacitance values may improve LDO noise but only at high frequencies, and may or may not show up in the data sheet's RMS noise measurement. Significant output capacitance is necessary to meaningfully impact RMS noise metrics (typically specified below 100 kHz) (see Figure 9).

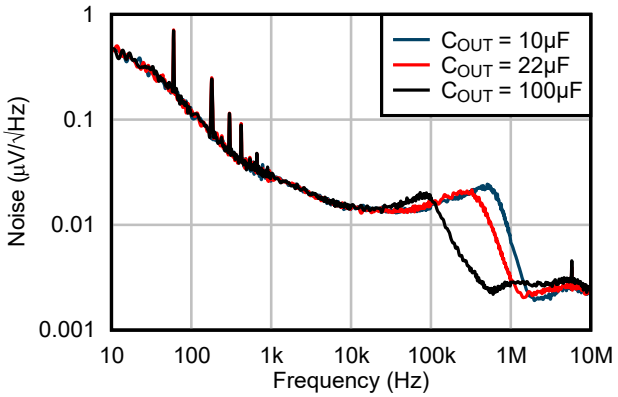


Figure 9. *LDO noise is insensitive to low and moderate values of C_{OUT}.*

The gain of the internal error amplifier increases when using feedback resistors to program V_{OUT} (see **Figure 10**). The error amplifier gain also magnifies the noise from V_{REF} (typically the largest source of noise inside an LDO) (see **Figure 11**).

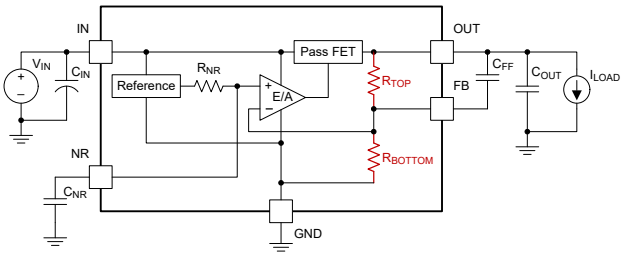


Figure 10. *V_{OUT} changes the gain of the error amplifier when operating in non-unity-gain feedback.*

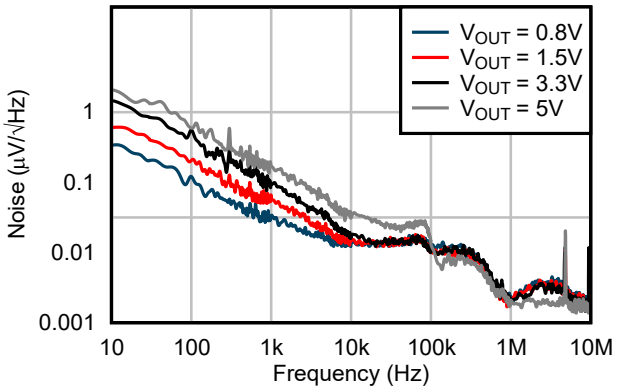


Figure 11. *LDO noise is sensitive to changes in V_{OUT} when operating in non-unity-gain feedback.*

Newer ultra-low-noise LDOs incorporate unity-gain feedback configurations to eliminate the increased noise (see **Figure 12**). The RMS plot for these LDOs remain flat across a wide range of output voltages (see **Figure 13**).

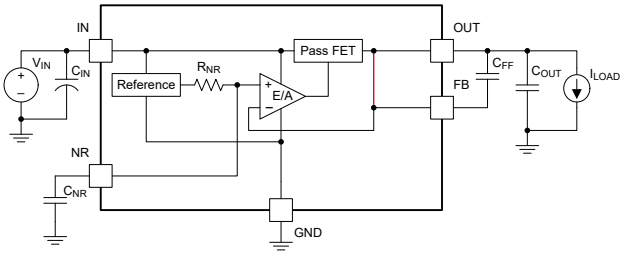


Figure 12. *The error amplifier gain is insensitive to V_{OUT} when operating in unity-gain feedback.*

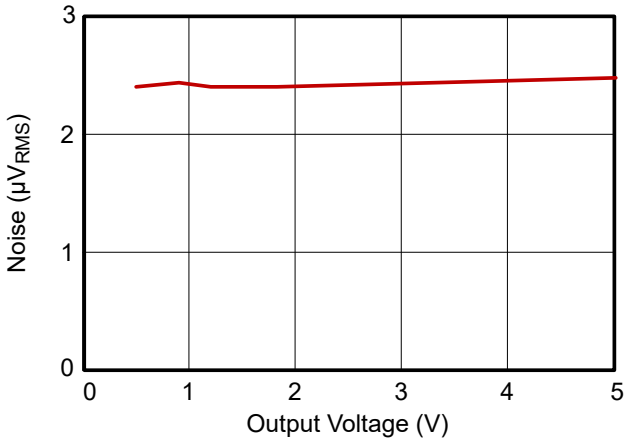


Figure 13. *LDO noise is insensitive to changes in V_{OUT} when operating in unity-gain feedback.*

A feedforward capacitor (C_{FF}) across the top setpoint resistor can reduce the noise of the LDO (see **Figure 14**) [**8**, **10**]. At higher frequencies, V_{FB} and V_{OUT} are effectively shorted by C_{FF}, preventing the reference noise from being magnified by the gain of the error amplifier (see **Figure 15**). If the LDO is already operating in unity-gain feedback (see **Figure 16**), the C_{FF} will not impact the noise curve.

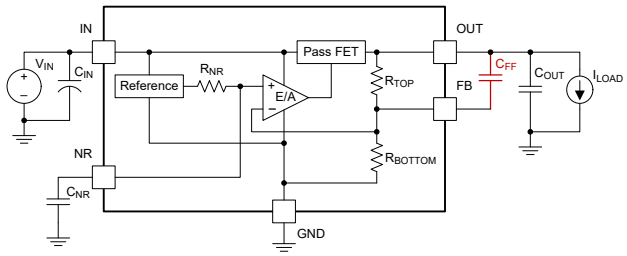


Figure 14. *C_{FF} placed across R_{TOP} emulates unity-gain feedback in the mid-band frequency range.*

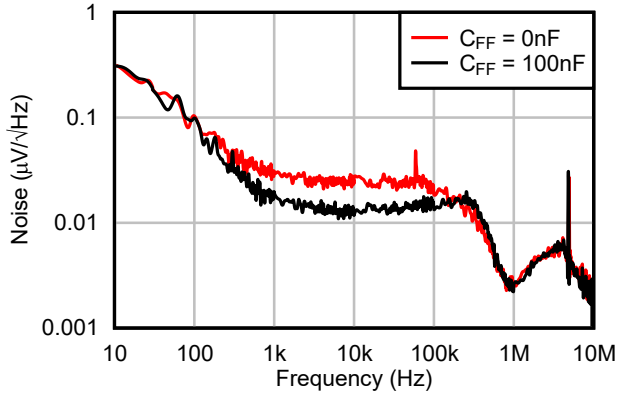


Figure 15. *C_{FF} placed across R_{TOP} reduces mid-band-frequency LDO noise.*

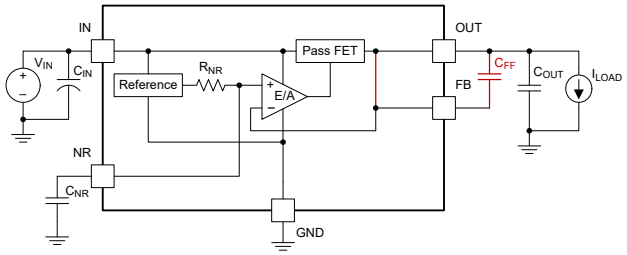


Figure 16. *C_{FF} has no effect on LDO noise when operating in unity-gain feedback.*

Placing a noise reduction (NR) low-pass filter between V_{REF} and the error amplifier attenuates the reference noise before it is gained up by the amplifier (see **Figure 17** and **Figure 18**) [8]. In most cases, the NR resistor is internal to the LDO; the NR capacitor may or may not be internal as well. Using the C_{FF} and NR filter simultaneously will achieve the lowest noise for a single LDO.

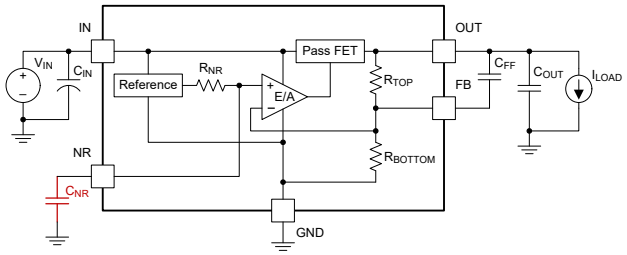


Figure 17. *An NR capacitor (C_{NR}) filters V_{REF} before the error amplifier.*

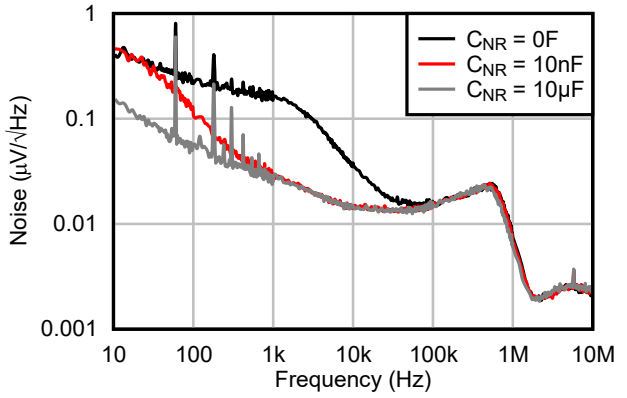


Figure 18. *The NR filter improves noise performance in the low- and mid-band frequency range.*

PSRR

The PSRR represents the regulator's ability to filter out changes in V_{IN}, expressed in **Equation 1** as a log ratio of the output noise to the input noise [11]:

$$\text{PSRR} = 20 \times \log\left(\frac{\text{VIN}_{(AC)}}{\text{VOUT}_{(AC)}}\right) \quad (1)$$

There are three regions in any PSRR curve (see **Figure 19**) [8, 12] affected by the circuit elements shown in **Figure 20**. The PSRR of V_{REF} dominates the PSRR of the LDO at low frequencies. In mid-band frequencies, the gain of the error amplifier dominates the PSRR performance. At high frequencies, the LDO runs out of bandwidth, and the capacitive divider formed by the parasitic capacitance of the pass device and the output capacitance determine the PSRR.

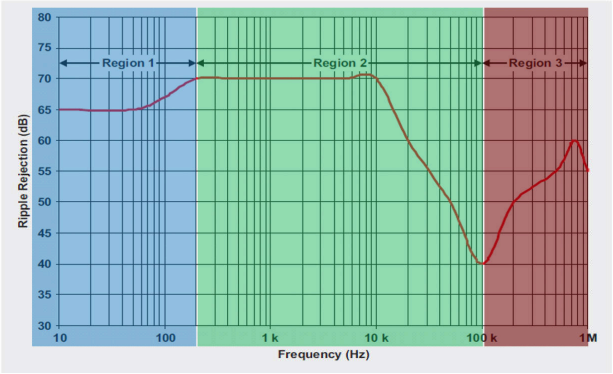


Figure 19. *Typical PSRR across frequency, with the regions highlighted in blue, green and gray.*

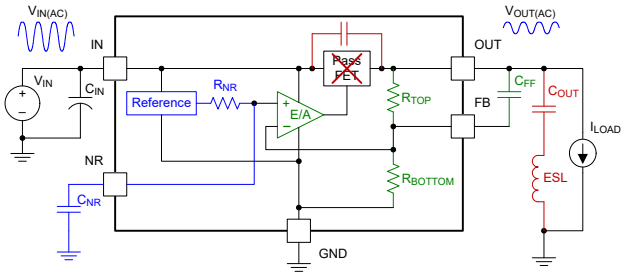


Figure 20. *Constituent elements of an LDO and associated impact on the PSRR curve.*

Maximizing the LDO PSRR in noise-sensitive environments is preferable when V_{IN} is excessively noisy. Thus, understanding what does and does not increase the PSRR performance is important in these applications. If an LDO accepts a bias voltage (V_{BIAS}) and the applied V_{BIAS} exceeds the minimum required value listed in the data sheet, then in general V_{BIAS} (see **Figure 21**) negligibly impacts the LDO's PSRR.

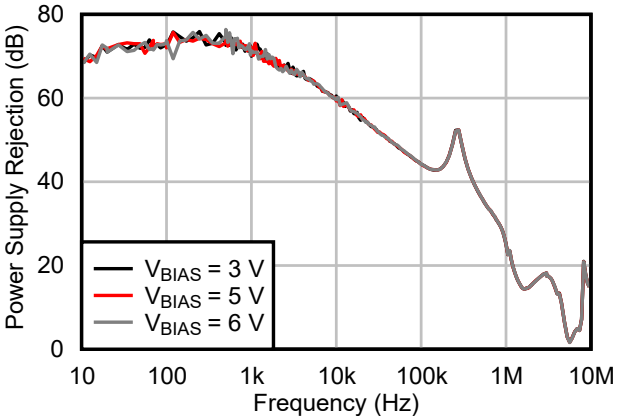


Figure 21. *LDO PSRR is insensitive to V_{BIAS} above dropout.*

Differences in V_{OUT} (see **Figure 22**) and output capacitance (see **Figure 23**) affect the LDO's internal feedback loops, which may minimally affect the LDO's PSRR. While V_{OUT} is usually fixed, you have control over the output capacitance selection and layout. Minimizing the equivalent series inductance (ESL) in the capacitor and the parasitic board inductance in the layout will decrease the impedance of the capacitor and increase the resonant frequency of the output capacitor, resulting in a better noise filter. As the resonant frequency increases, so does the PSRR of the LDO at higher frequencies.

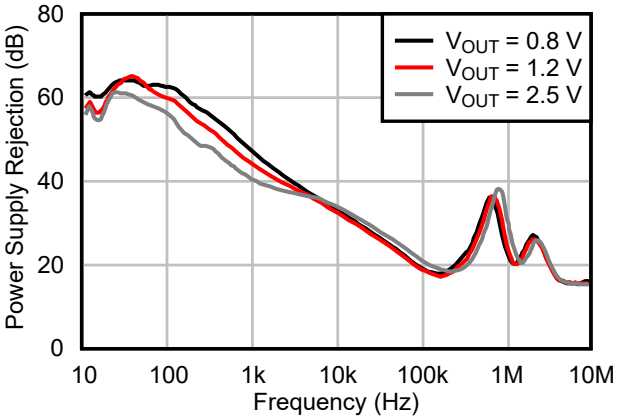


Figure 22. *LDO PSRR is minimally sensitive to V_{OUT}.*

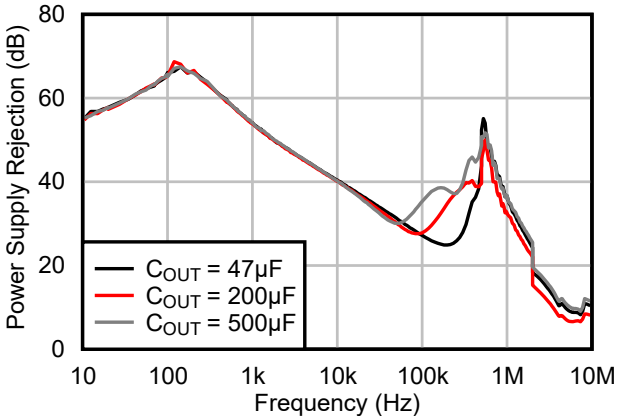


Figure 23. *LDO PSRR is insensitive to small and moderate values of C_{OUT}.*

The headroom voltage (V_{IN} – V_{OUT}) (see **Figure 24**) has a significant effect on PSRR. Operating close to the minimum headroom voltage, or V_{DO}, results in very little PSRR. Increasing the headroom voltage raises the open-loop gain, resulting in better PSRR performance. Thus, PSRR is typically specified with more headroom voltage than V_{DO} alone. Common values are 300 mV, 500 mV or even 1 V of headroom, after which PSRR performance usually plateaus (see **Figure 25**).

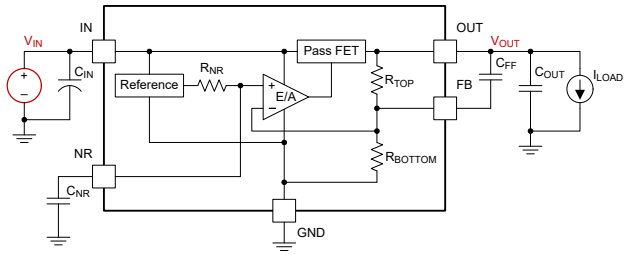
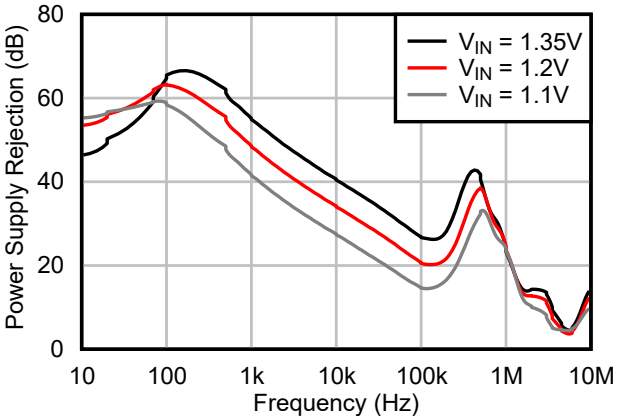


Figure 24. *The headroom voltage (V_{IN} – V_{OUT}) influences the PSRR of the LDO.*



V_{OUT} = 0.8 V

Figure 25. *Raising the headroom voltage also raises the LDO PSRR.*

Increasing the load current negatively affects the PSRR of the LDO (see **Figure 26** and **Figure 27**). Always review the PSRR curves in the LDO data sheet for the data that best matches your load current. PSRR test data captured with small loads applied are no indication of PSRR performance when operating near the full load of the LDO; the data is also insufficient unless this minimal load is your intended operating condition. Either request the PSRR data from Texas Instruments or use an evaluation module (EVM) to capture the data directly using your application's exact conditions.

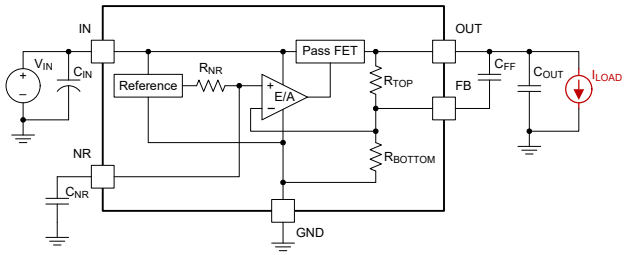


Figure 26. *Increasing the load current influences the PSRR of the LDO.*

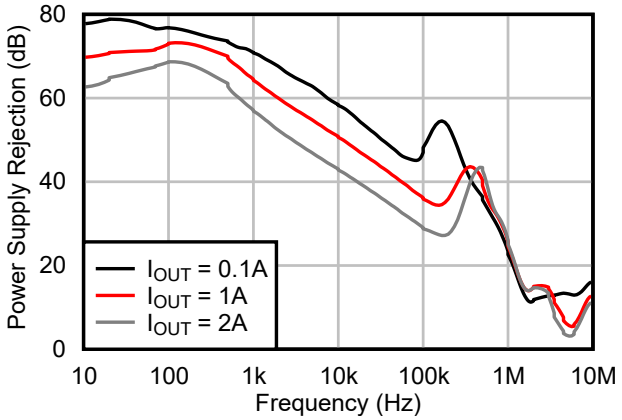


Figure 27. *Raising the load current decreases the LDO PSRR.*

The V_{REF} of the LDO has a finite PSRR, so noise on V_{IN} can negatively affect V_{REF}. If left unchecked, this noise can be magnified by the error amplifier and propagate to the V_{OUT} of the LDO, resulting in degraded PSRR performance. Filtering V_{REF} using the NR filter previously discussed (see **Figure 17**) improves the PSRR of the LDO in the low- to mid-band frequencies. Only a small amount of NR capacitance makes a big impact on the PSRR curve (see **Figure 28**).

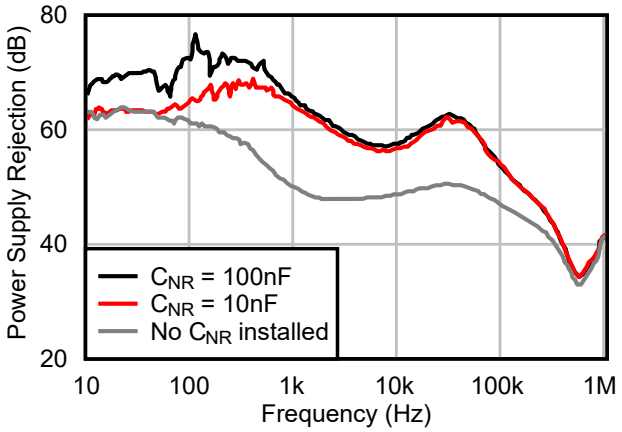


Figure 28. *The NR resistor-capacitor filter improves LDO PSRR.*

In most cases, adding a C_{FF} increases the LDO feedback bandwidth and improves the PSRR of the LDO (see **Figure 14** and **Figure 29**) [10]. If the LDO is operating in unity gain feedback, the C_{FF} will short out and have no effect on the PSRR curve (see **Figure 16**).

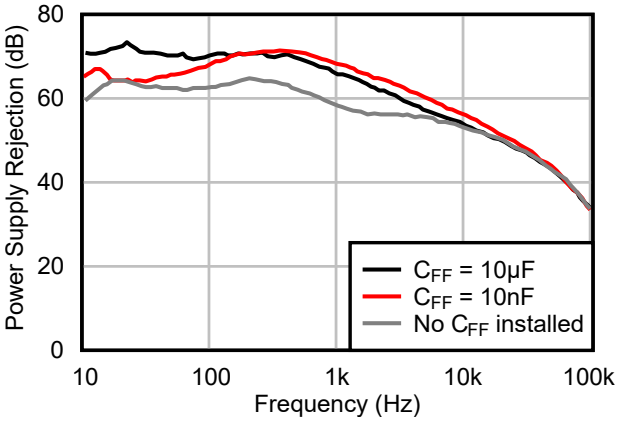


Figure 29. *Placing C_{FF} across R_{TOP} improves PSRR.*

Thermal Metrics

The junction-to-ambient thermal impedance ($R_{\theta JA}$) is an LDO thermal performance metric used to determine the LDO junction temperature (T_J) as a function of its P_D. While direct comparisons of thermal performance between LDOs are necessary, $R_{\theta JA}$ is heavily dependent on the layout of the printed circuit board (PCB) [13, 14]. The Joint Electron Device Engineering Council (JEDEC) committee has standardized a method to measure and report semiconductor thermal metrics [15]. This committee has defined an industry standard for a device's $R_{\theta JA}$ given a set of specific board design and layout requirements. The JEDEC PCB layout uses a four-layer board, with internal 1-ounce copper layers alternating between GND and V_{DD} (see **Figure 30**). The top 2-ounce copper layer uses traces routed to each input pin with GND fill everywhere else (see **Figure 31**), and the bottom 2-ounce copper layer is a GND pour. The JEDEC standard also defines the size of the PCB precisely.

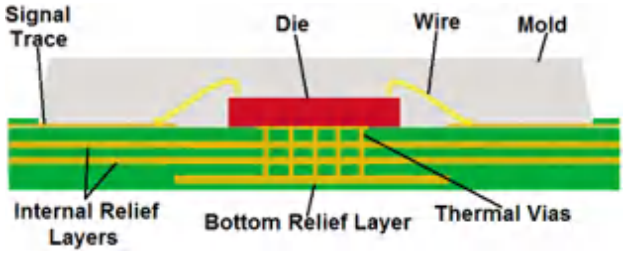


Figure 30. *JEDEC standard PCB layout.*

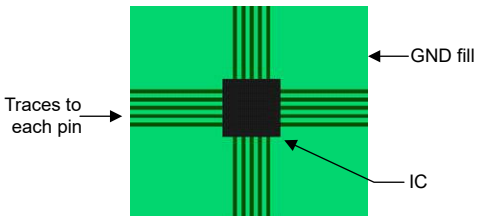


Figure 31. *JEDEC standard top-side routing and GND fill.*

Fortunately, most PCB designs are larger than the JEDEC specification and include additional ground planes and thermal vias in the ground pads of the LDOs. The real-world $R_{\theta JA}$ is often lower than the published JEDEC $R_{\theta JA}$ by as much as 25% to 50% of published $R_{\theta JA}$ values.

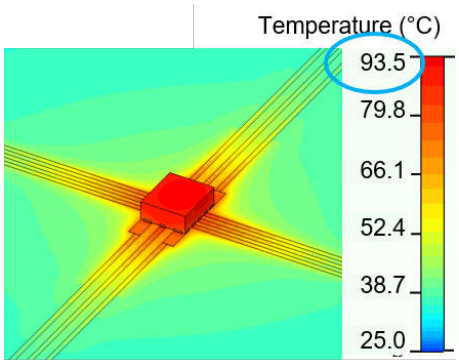
Consider the case of an LDO mounted onto an EVM dissipating 1 W. **Equation 2** and **Equation 3** define the P_D of an LDO, while **Equation 4** defines the T_J of an LDO:

$$P_D = (V_{IN} - V_{OUT}) \times (I_{OUT} + I_Q) \quad (2)$$

$$P_D \approx (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

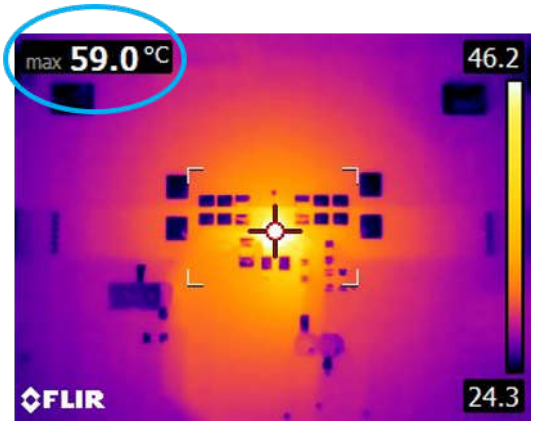
$$T_J = T_A + (\theta_{JA} \times P_D) \quad (4)$$

The JEDEC specification layout yields $R_{\theta JA}$ = 68.5°C/W (see **Figure 32**), while actual measurements of the LDO mounted onto the EVM are closer to 34.7°C/W (see **Figure 33**). To reduce the $R_{\theta JA}$ in a design, you should maximize both the number of thermal vias within the thermal pad and the PCB copper around the device. Place local thermal vias around the LDO to reduce $R_{\theta JA}$ further.



JEDEC simulation: θ_{JA} = 68.5°C/W

Figure 32. *JEDEC thermal simulation.*



EVM measurement: θ_{JA} = 34.7°C/W

Figure 33. *Thermal measurement of Figure 32 using an EVM.*

During the design phase, use the published $R_{\theta JA}$ as a guide. When capturing test data on physical hardware, another set of JEDEC thermal parameters called the Psi parameters are more useful. Psi parameters provide an estimate of the junction temperature almost independent of the board layout (see **Figure 34**). The most common parameter is the junction-to-top (Ψ_{JT}) Psi parameter. Revisiting **Figure 33**, **Equation 5** and **Equation 6** estimate T_J as 63.5°C:

$$T_J = T_C + \Psi_{JT} \times P_D \quad (5)$$

$$T_J = 59\ °C + 4.5\ °C/W \times 1\ W = 63.5°C \quad (6)$$

Small Psi parameter values are common for LDOs, as most of the internal integrated circuit is the pass device, which is dissipating the heat. Therefore, an infrared image is usually pretty close to the actual T_J for LDOs.

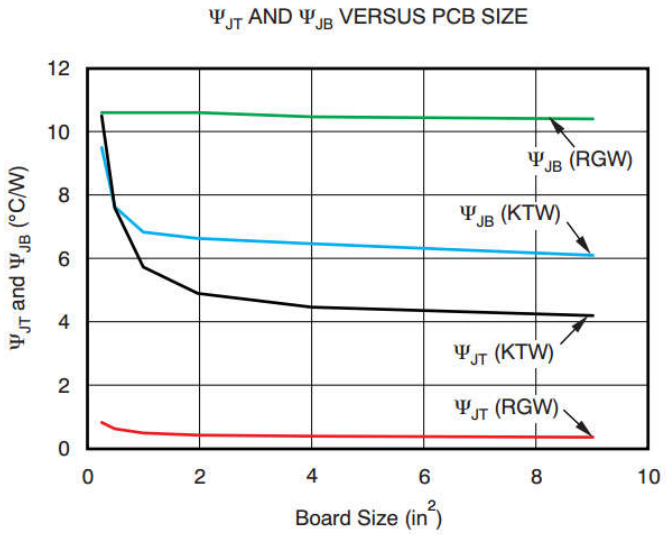


Figure 34. *Ψ_{JT} and Ψ_{JB} vs. PCB size.*

Load Transient Response Near Dropout

It is important to understand the minimum V_{IN} necessary to achieve low loss and high efficiency for an LDO. If the LDO operates with DC current loading, V_{IN} must be at least V_{OUT} + V_{DO} to maintain regulation. In these examples (see **Figure 35** and **Figure 36**), the V_{DO} of the TPS7A14 LDO is typically 45 mV. The minimum V_{IN} may increase, however, if the application experiences a load transient on V_{OUT}. LDOs need more headroom if the application has transient conditions to respond to.

Because the headroom voltage drops in the presence of a load transient, V_{OUT} deviation and recovery times will increase (see **Figure 36**). During a low to high current step, the LDO will experience a larger droop and delayed response to reach steady state. During a high to low transition, V_{OUT} may become warped from a lack of headroom. V_{OUT} in **Figure 35** is a key example of this behavior when the load steps from high to low. The peak deviation on V_{OUT} matches the perturbation on V_{IN}, and the recovery slightly undershoots the steady-state 800-mV setpoint.

You must know your transient requirements if you wish to minimize V_{IN} to maximize efficiency. The transient requirements include the amplitude of the load transient pulse and the ramp rate of the pulsed load. You can

test with your own components installed on an EVM to assess whether the LDO performance meets your needs or if you need to raise or lower the V_{IN}.

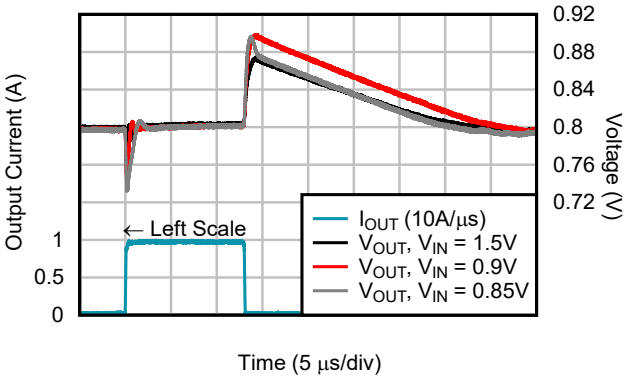


Figure 35. *LDO transient performance near dropout.*

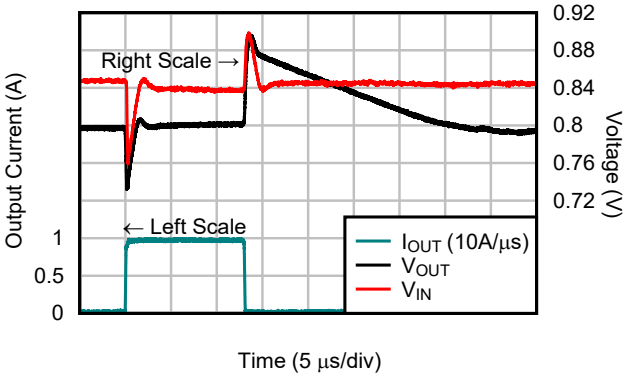


Figure 36. *LDO transient performance vs. headroom voltage.*

Parallel LDOs

Parallel LDOs are becoming more popular and offer numerous advantages over single LDO and competing switching-converter options. Parallel LDOs can provide increased load current, reduced system noise, improved PSRR and thermal spreading, and reduced headroom requirements for a given load current [16]. Thus, designers are now exploring parallel LDOs as a solution to many different design challenges.

Switching converters and polyphase modules typically require bulky magnetics, unlike parallel LDO systems where the tallest component is the small output capacitor [17]. Moreover, bandwidth limitations of switching converters [18] may require additional output capacitance to hold up V_{OUT} during a high-speed transient response. Unlike switching converters, modern LDOs and parallel LDO systems have bandwidths into the megahertz frequencies and are not limited to $F_{SW}/5$ or $F_{SW}/10$.

The switching converter V_{OUT} ripple voltage may be unwanted for some applications, often requiring larger capacitor banks to reduce the amplitude of the ripple voltage. LDOs and parallel LDO systems do not have ripple voltage, eliminating this concern. Switching converters typically require additional electromagnetic interference (EMI) filters to meet EMI compliance, adding cost and schedule to a design. Parallel LDO systems do not inherently need EMI filtering, enabling cost-optimized designs with shorter design cycles.

With the current driver dominating laser phase noise, low-noise parallel LDOs offer state-of-the-art current drivers, with high performance, ultra-low noise laser driver applications using as many as 10 parallel LDOs.

It may be difficult or impractical to use switching converters in applications with a narrow headroom voltage (or when V_{IN} - V_{OUT} is very small) if the maximum duty cycle inhibits the regulation of V_{OUT} from V_{IN}. While single LDOs offer a solution at light loads, parallel LDOs offer a solution for heavier load currents.

Texas Instruments has modernized the design and analysis of parallel LDO circuits using ballast resistors [16], [17], [19], placing this new mathematical foundation for parallel LDOs into a downloadable software tool [20] that enables you to rapidly design these parallel LDOs using worst-case analysis techniques.

Parallel LDOs Using Ballast Resistors – Design and Analysis

Unfortunately, it is not possible to directly connect output voltages together to parallel LDOs. Each LDO has a slightly different V_{OUT}, and the LDO in the parallel system with the highest V_{OUT} tries to provide the entire load until it enters the current limit. In this state, the other LDOs in a parallel system will not contribute to the load. While

in the current limit, the dominant LDO voltage will droop, which causes the LDO with the next-highest V_{OUT} to try and provide the entire load until it also enters the current limit. This process will repeat indefinitely and result in an oscillation on the output. There is a need for a method to isolate each LDO from each other while simultaneously providing a combined load to the output. Ballast resistors offer a classic solution to this design challenge (see **Figure 37** and **Figure 38**).

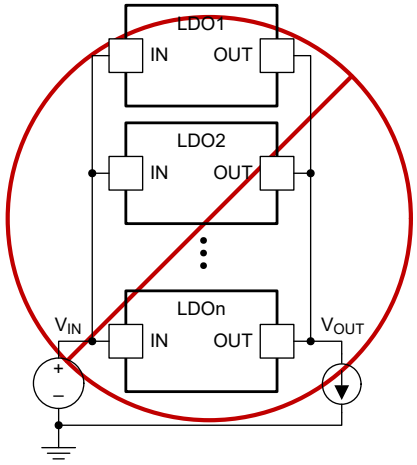


Figure 37. *Incorrect method of paralleling LDOs.*

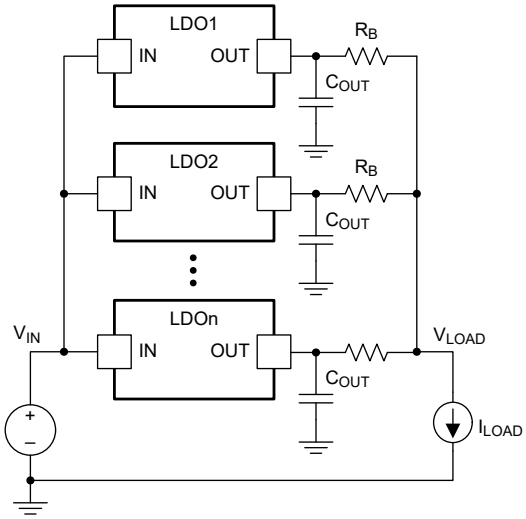


Figure 38. *Correct method of paralleling LDOs.*

Figure 39 shows how to redraw parallel LDOs using ballast resistors. Each LDO is represented by an ideal voltage source representing the typical V_{OUT} in series with an error voltage (V_E) term. V_E is made up of tolerances from the device-specific data sheet such as line and load regulation, the offset voltage (V_{OS}) of the error amplifier (which may include the line and load regulation), and tolerances from feedback resistors if the LDO does not operate in unity-gain feedback. If the LDO does operate in unity gain, V_E is the same as V_{OS}. Notice that **Figure 39** defines the output voltage and output current of each LDO as V_{OUT} and I_{OUT}, while the voltage and current after the ballast resistors are V_{LOAD} and I_{LOAD}, respectively. This is the terminology when referring to the LDO outputs or system loads for a parallel LDO design.

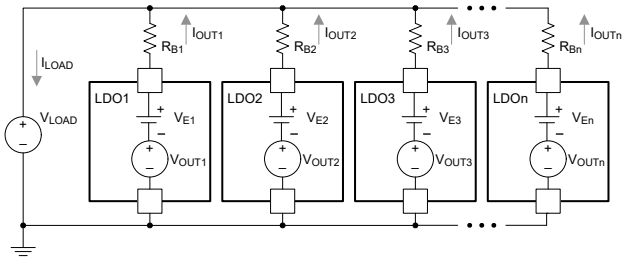


Figure 39. *Equivalent model for n parallel LDOs using ballast resistors.*

In most designs, the parallel LDOs must meet a V_{LOAD} requirement in addition to providing more current to the load. To help with this, you'll need a set of equations with known and controllable inputs (such as R_B, V_{OUT}, I_{LOAD} and V_E) to solve for outputs you must meet (such as V_{LOAD}). Solving the mesh current analysis on **Figure 39** yields **Equation 7** through **Equation 10**:

$$R_B = \frac{\max\limits_{1<x<n} V_{En} - \min\limits_{1<x<n} V_{En}}{\Delta I_{MAX}} \quad (7)$$

$$I_{LOAD} = \sum_{n=1}^{n} \frac{V_{OUTn} - V_{LOAD} + V_{En}}{R_{Bn}} \quad (8)$$

$$V_{LOAD} = \frac{\sum_{n=1}^{n} \frac{V_{OUTn} + V_{En}}{R_{Bn}} - I_{LOAD}}{\sum_{n=1}^{n} \frac{1}{R_{Bn}}} \quad (9)$$

$$I_{OUTn} = \frac{V_{OUTn} - V_{LOAD}}{R_{Bn}} + \frac{V_{En}}{R_{Bn}} \quad (10)$$

Notice that V_{LOAD} appears as an input in **Equation 10**; however, the intention is to solve for V_{LOAD} for comparison against your system requirements. Setting

the ballast resistors and output voltages to the same value and recalculating will result in **Equation 11**. **Equation 7** through **Equation 11** form the foundation of a new analysis set on parallel LDOs using ballast resistors.

If $R_{B1} = \ldots = R_{Bn}$ and $V_{OUT1} = \ldots = V_{OUTn}$:

$$I_{OUTn} = \frac{I_{LOAD} - \left(\Sigma_{n=1}^{n} \frac{V_{En}}{R_B}\right)}{n} + \frac{V_{En}}{R_B} \quad (11)$$

As R_B increases, the current sharing ΔI_{MAX} among each LDO improves. Increasing R_B will also increase the load regulation (V_{OUT} - V_{LOAD}). Thus, it is more difficult to meet the regulation band requirements with a larger R_B. There is an optimum value of ballast resistance that satisfies both V_{LOAD} and ΔI_{MAX}, which **Equation 7** through **Equation 11** can also help you find (see **Figure 40**).

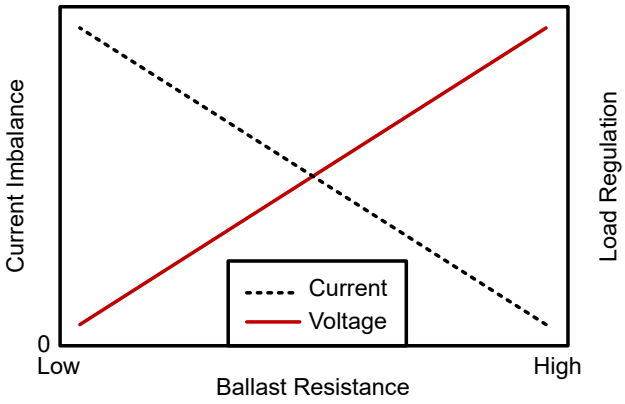


Figure 40. *Impact of the ballast resistance on the maximum current imbalance and load regulation.*

Two methods exist to building the ballast resistor into the system, each with their pros and cons. One method is to use the PCB copper and another method is to use a discrete resistor. To design the PCB trace, you can use the Institute of Printed Circuits (IPC)-2221 standard, which is readily available online. While this approach has the largest footprint (see **Figure 41**) and widest tolerance (see **Figure 42**), it also has the lowest production cost and offers the highest temperature solution. A discrete resistor solution provides a smaller form factor with low tolerance, but it must be derated in accordance with the resistor derating curve (see **Figure 43**).

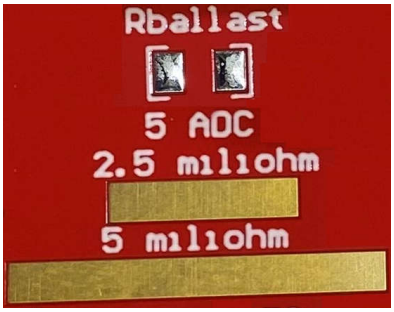


Figure 41. *Comparing a 1206-sized discrete resistor (top) with PCB trace resistors (middle and bottom).*

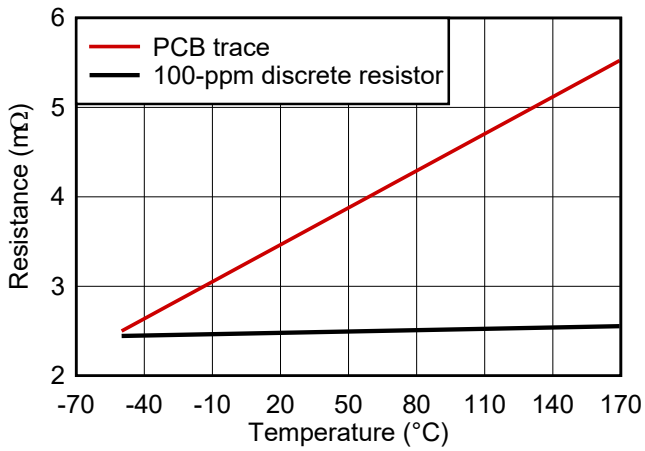


Figure 42. *Tolerance comparison of a PCB trace and 100-ppm discrete resistor over temperature.*

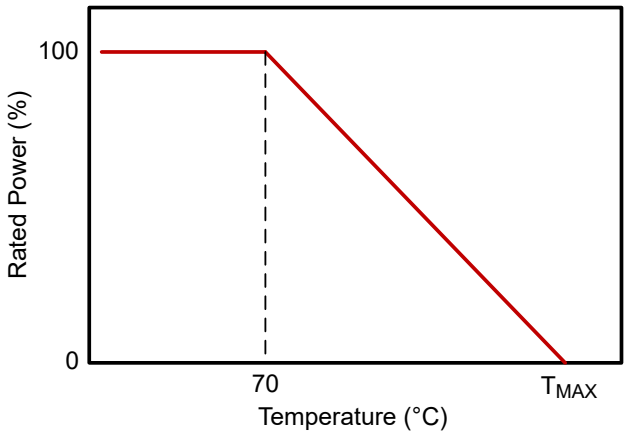


Figure 43. *Typical discrete resistor derating curve across temperature.*

The PCB itself has power plane resistance in series with each R_B; thus, you can reduce R_B by this series PCB resistance to optimize the design. You will need to assess two paths: from the LDO to the load and back (see **Figure 44**) and between each LDO (see **Figure 45**).

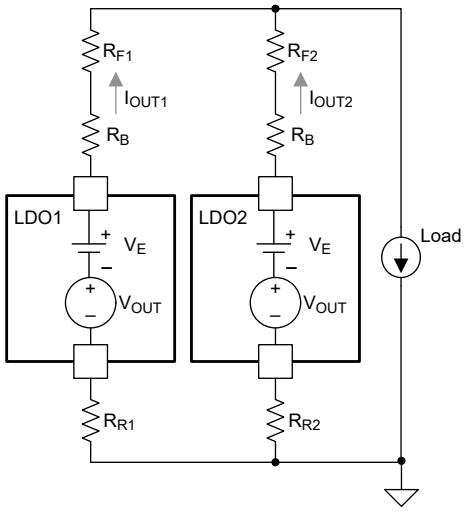


Figure 44. *Impact of nonideal PCB impedance between the parallel LDOs and the load.*

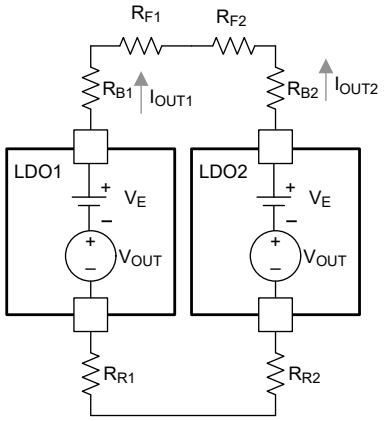


Figure 45. *Impact of nonideal PCB impedance between each parallel LDO.*

Optimizing the discrete R_B by subtracting the parasitic PCB impedance is strictly optional and is only used in cases that require maximum performance. Many parallel LDO designs use sufficiently high R_B such that the PCB DC resistance is an insignificant percentage of R_B. Performing this optional step will achieve small (if any) performance improvements when R_B is ≥ 50 mΩ.

Texas Instruments developed an easy-to-use calculator available for download to quickly design parallel LDOs (see **Figure 46**). There is no Visual Basic in the tool, which should make it accessible for most engineers. The calculator performs a worst-case analysis using **Equation 7** through **Equation 11** to find the minimum number of parallel LDOs and the optimum ballast resistance necessary to meet a set of system requirements. The tool includes pre-populated common LDOs being paralleled in the industry, along with their data-sheet values, to enable quick comparisons of different LDOs for your application. Simply enter your system requirements and the calculator provides the optimum ballast resistance and minimum LDOs required to meet your requirements.

Not included: Abs Max voltage assessment or DC setpoint analysis
This calculator assumes the same LDO IC, ballast resistor, and output voltage is used for all LDO's in parallel

TPS7A57

LDO Specifications

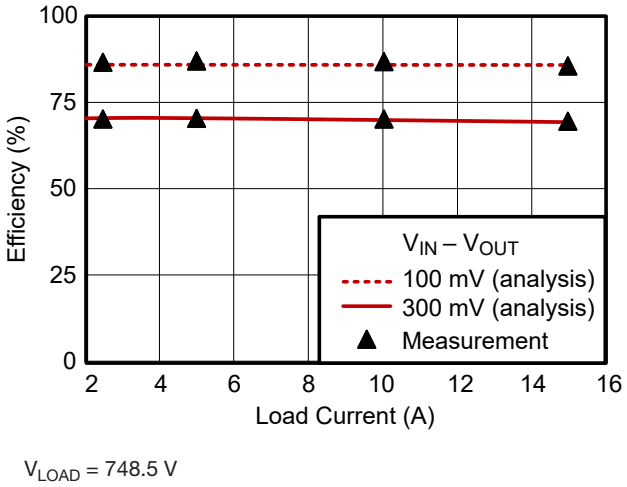
Parameter	Value	Units	Optional User Entry	Units
V_E, high	2	mVdc		mVdc
V_E, low	-2	mVdc		mVdc
Thermal Impedance T_{JA}	21.9	°C / W		°C / W

Parallel LDO System Requirements

Parameter	Value	Units		Units
T_A	85	°C		°C
Maximum T_J per LDO	125	°C		°C
V_{IN}	1.25	Vdc		Vdc
V_{OUT}	0.75	Vdc		Vdc
Allowable load regulation	0.02	Vdc		Vdc
System Noise Requirement (10 Hz - 100 kHz)	2.45	µVrms		µVrms
Total System Load:	8.48	A		A
Minimum Ballast Resistance needed	0.8	mΩ		
Optimum Ballast Resistance	5.608043	mΩ		
Ballast Resistance Selected	5.608043	mΩ		mΩ
	N =			
Minimum number of parallel LDO's required:	3			

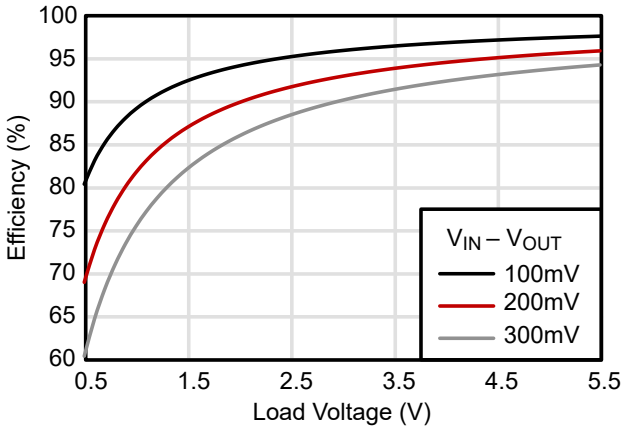
Figure 46. *The parallel LDO calculator enables immediate calculation of the optimum ballast resistance and minimum number of parallel LDOs to meet a set of system requirements using worst-case analysis.*

Figure 47 through **Figure 51** show test data on parallel LDOs using one of our newer devices. The analysis uses **Equation 7** through **Equation 11** to calculate the efficiency, and measurements against the analysis provide excellent correlation. The efficiency of parallel LDOs is similar to the efficiency of single LDOs (see **Figure 47**). The higher V_{LOAD} is, the higher the efficiency for a given headroom voltage (see **Figure 48**).



V_{LOAD} = 748.5 V

Figure 47. *Efficiency analysis and measurement of parallel LDOs.*



I_{OUT} = 10 A

Figure 48. *Parallel LDO efficiency vs. load voltage and headroom voltage.*

The thermal image in **Figure 49** showcases the thermal spreading advantage of parallel LDOs. In this application, the LDOs are dissipating nearly 7 W with a 76°C increase in temperature – an excellent result for any linear regulator system.

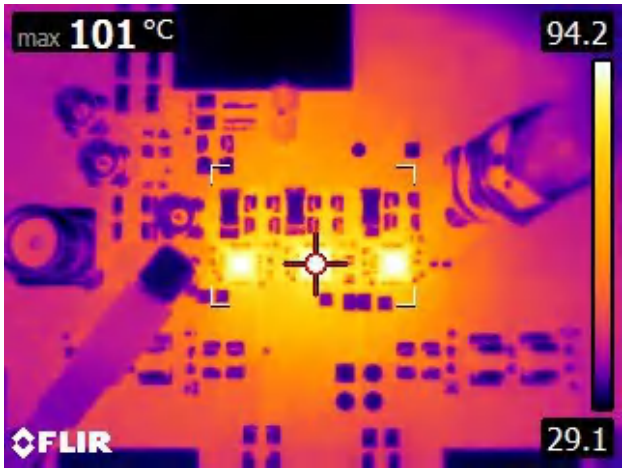


Figure 49. *Thermal image of three parallel TPS7A57 LDOs dissipating 6.75 W for 30 minutes.*

Figure 50 shows the noise performance of parallel vs. single LDOs, yielding noise results that are close to the theoretical square-root-of-three reduction for three parallel LDOs.

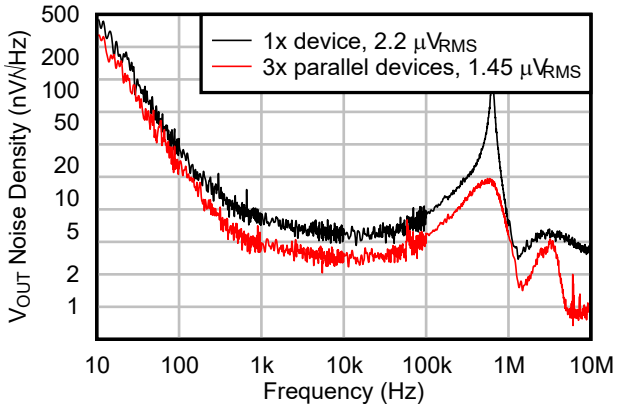


Figure 50. *Parallel LDO output voltage noise density vs. frequency.*

Figure 51 shows the PSRR curve comparison of single vs. parallel LDOs, with the PSRR of a single LDO providing 4.5 A to the load. **Figure 51** also shows three parallel LDOs, each providing about the same current, delivering 13.5 A to the load. As expected, their PSRR curves are the same.

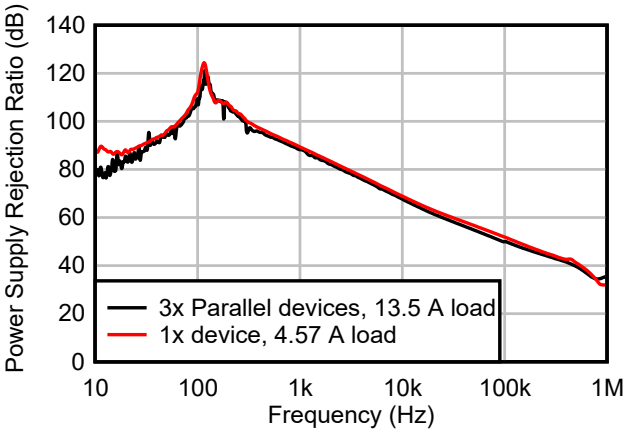


Figure 51. *PSRR vs. frequency and I_{OUT} for three parallel TPS7A57 LDOs and one single TPS7A57 LDO.*

Figure 52 shows load transient comparisons of single LDO solutions vs. parallel LDO solutions. When operating under low headroom, the single LDO transient response suffers from large voltage deviation and delayed recovery to steady state. Sharing the load among three parallel LDOs relaxes the headroom requirements and significantly enhances the output voltage deviation and recovery.

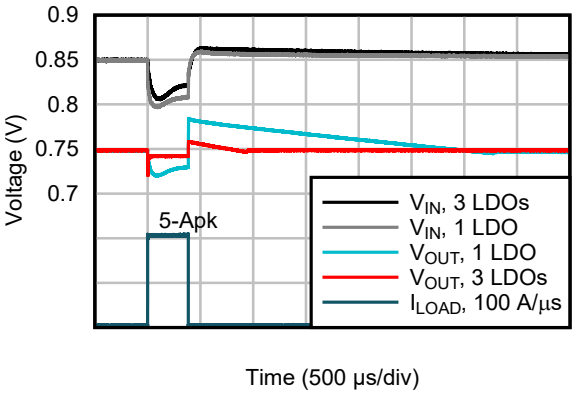


Figure 52. *Parallel vs. single LDO transient performance.*

Constant Current Regulation

It is possible to configure LDOs (single or parallel) as a current source to drive noise-sensitive electronics for any of the reasons that I have already covered (see **Figure 53**).

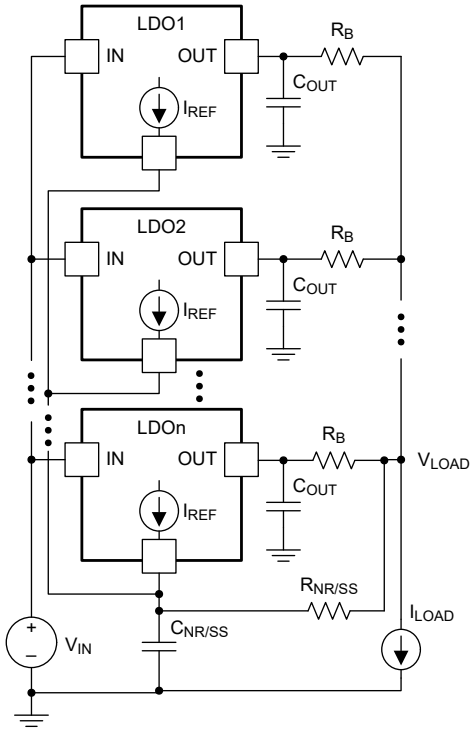


Figure 53. *Configuring single or parallel LDOs using precision current references to generate a constant current source.*

The LDOs in **Figure 53** operate in unity gain feedback and generate a precision current source. Traditionally, V_{REF} (and V_{OUT}) are generated by the precision current reference flowing into a resistor ($R_{NR/SS}$) connected across $C_{NR/SS}$. To configure the LDOs to operate as current sources, simply rotate $R_{NR/SS}$ off of ground and tie it to V_{LOAD}. You will need a small R_B, even if you are using only one LDO. The voltage drop across $R_{NR/SS}$ must equal the voltage drop across R_B. **Equation 12** calculates the $R_{NR/SS}$ you'll need for your system:

$$R_{NR/SS} = \frac{I_{OUT} \times R_B}{N \times I_{REF}} = \frac{I_{LOAD} \times R_B}{N^2 \times I_{REF}} \quad (12)$$

Test data comparisons between three parallel TPS7A57 LDOs configured as constant current sources provide excellent correlation to the analysis using the equations derived in this topic (see **Figure 54**).

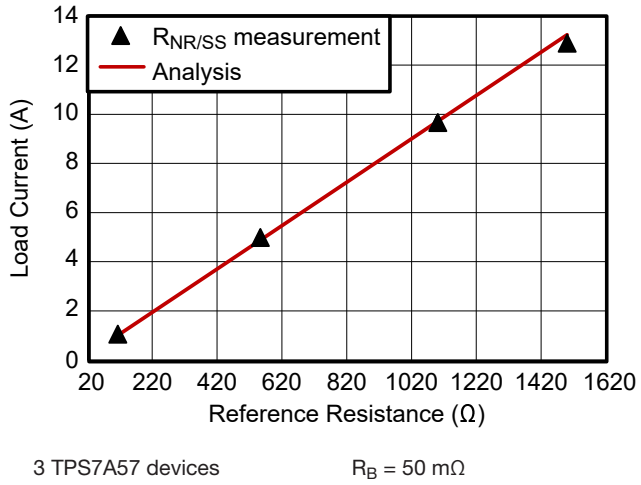


Figure 54. *Analysis and measurements of load current vs. $R_{NR/SS}$.*

MISO LDOs

Traditional single-input-single-output (SISO) converters are incapable of powering a heavy load when insufficient power is available on V_{IN}. Ideally, you want to combine the power from multiple input supplies to meet the load power requirements. Such a power supply is called a MISO power supply (see **Figure 55**).

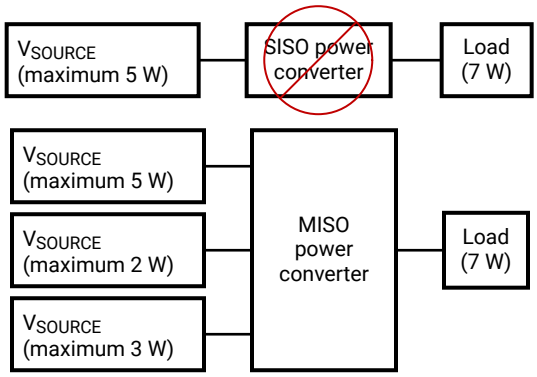


Figure 55. *Power system showcasing a need for MISO power supplies to combine input power to meet a load requirement.*

Designing a MISO parallel LDO is easy if you need to share power equally among different input supplies. Recalling the previous discussion on parallel LDOs, use the calculator and equations to obtain R_B and connect the different input supplies to each LDO V_{IN}. If you need to adjust how much current to source from each input, revisit the parallel LDO design process.

If you need unequal current sharing among different input supplies, you can change the ballast resistors to control the current from each LDO. MISO LDO design is slightly iterative, as you no longer have a closed-loop formula (see **Figure 56**). Fundamentally, this process iteration is simple:

1. Obtain your requirements.
2. Make some assumptions on V_{LOAD}.
3. Make some assumptions on V_E.
4. Calculate R_B.
5. Perform statistical simulations.
6. Check the design results against your requirements.
7. Fabricate the design.

Most designs only need a few iterations, and the process is typically complete in less than 10 minutes. Let's discuss each step individually.

In step No. 1, obtain your basic requirements for noise and PSRR using the approach previously discussed so that you know how many LDOs to parallel. You will also need to assess how many input supplies you wish to draw power from and the maximum power you can claim from each supply.

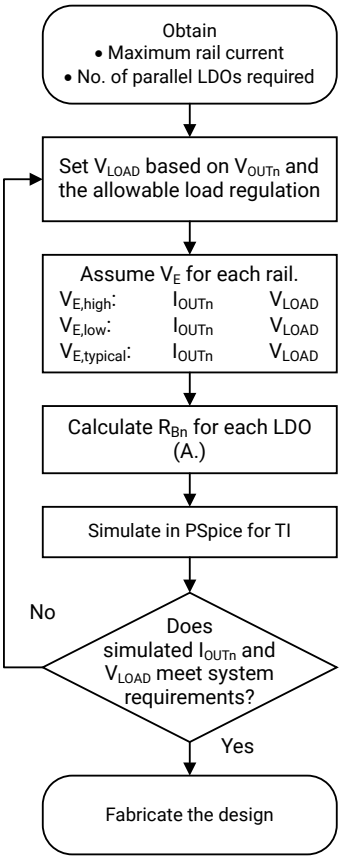
In step No. 2, you need to assign an allowable V_{LOAD} from your V_{OUT} and load regulation requirements. For instance, if V_{OUT} of each LDO is 1 V and you can allocate a maximum 10-mV load regulation drop across the ballast resistors, then the V_{LOAD} will be 0.99 V.

In step No. 3, you need to assume a V_E for each LDO. On the first pass through, it is easiest to set the V_E of each LDO to its nominal value. Setting V_E to be high for an LDO will naturally increase the output current of that LDO and slightly decrease the V_{LOAD}. To raise V_{LOAD}, you will need to reduce the V_E assumption for an LDO, although this will also lower the typical output current of that LDO.

In step No. 4, take the results from step Nos. 1 through 3 and calculate the R_B for each LDO.

This is not a worst-case analysis, so it is a good idea to perform step No. 5 and simulate the system using PSpice for TI. Not only can you obtain statistical distributions for each design parameter (such as V_{LOAD} or individual LDO output currents – see **Figure 57**) but you can also perform sensitivity analysis (see **Figure 58**). This sensitivity analysis will help identify which component you should focus on to improve V_{LOAD} or output currents.

If the simulation results do not meet your system requirements, you can perform step No. 6 by adjusting your V_{LOAD} specification and V_E assumptions and reiterate through steps No. 2 through 5. Recalculate the ballast resistors and simulate the system again. A few iterations are usually sufficient. With steps No. 1 through 6 complete, you can move to the final step No. 7 and fabricate the hardware.



A. $$R_{Bn} = \frac{V_{OUTn} - V_{LOAD}}{I_{OUTn}} + \frac{V_{En}}{I_{OUTn}} \quad (13)$$

Figure 56. *MISO LDO design process.*

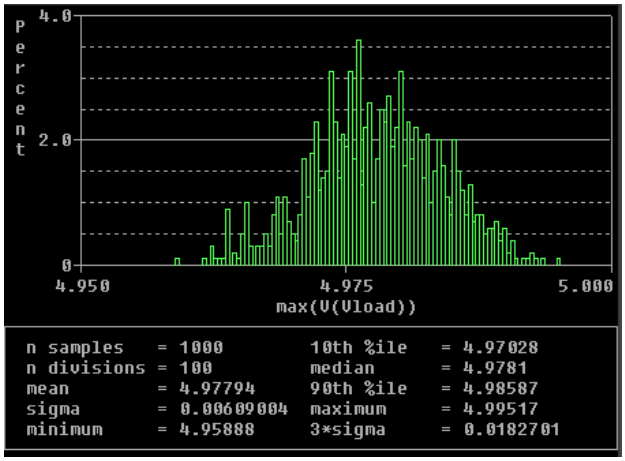


Figure 57. *PSpice for TI Monte Carlo analysis results.*

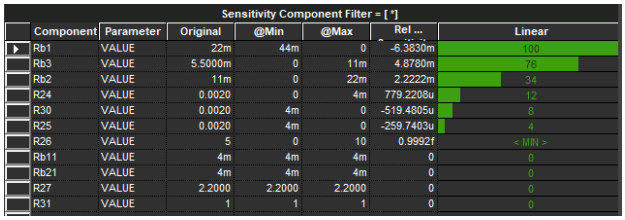


Figure 58. *PSpice for TI sensitivity analysis results.*

I collected test data comparing the two types of parallel LDOs. For SISO parallel LDOs, I left each R_B the same; each LDO provides approximately the same current to the load. The MISO parallel LDOs are designed to deliver different values of current using the iterative process. I selected ballast resistors to provide approximately 1.6 A, 3.1 A and 4.6 A and connected different input supplies to each LDO. I selected V_{IN} to maintain the same P_D for each LDO.

In **Figure 59**, you can see noise measurements showing identical results between the two configurations.

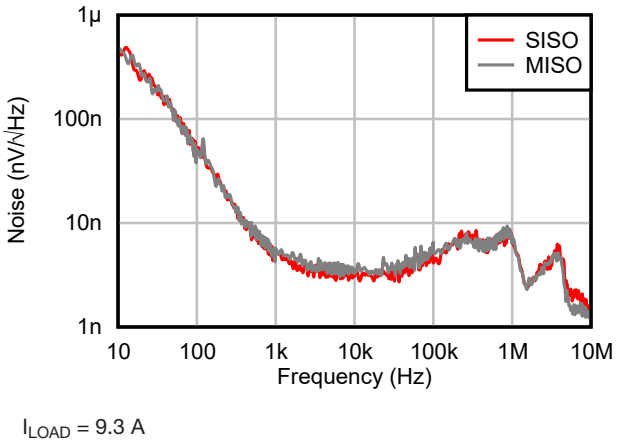


Figure 59. *Noise spectral density measurements of SISO parallel LDOs vs. MISO parallel LDOs.*

Thermal measurements after applying five minutes of power are also the same (compare **Figure 60** and **Figure 61**). The only difference is small errors in applied V_{IN} for each LDO.

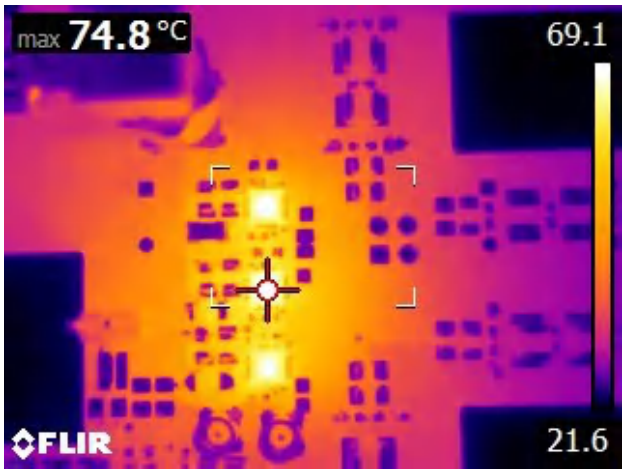


Figure 60. *Thermal image of MISO parallel TPS7A57 LDOs dissipating 4.65 W (load applied for five minutes).*

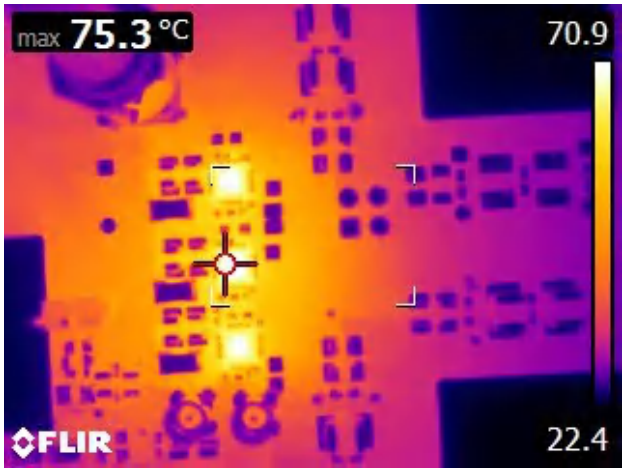


Figure 61. *Thermal image of SISO parallel TPS7A57 LDOs dissipating 4.65 W (load applied for five minutes).*

Transient responses between the two systems show a slight advantage to the SISO parallel LDO (see **Figure 62**). The actual transient response is nearly identical; it is the DC load regulation that is different. The MISO LDO increased the ballast resistors from the SISO LDO starting point to set the different values of input current. This has the net effect of slightly worse load regulation in the MISO LDO's transient response.

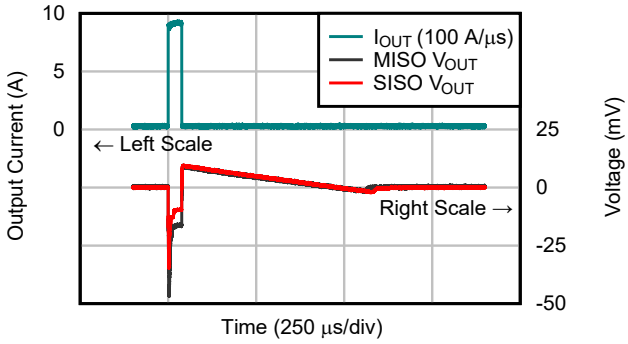


Figure 62. *MISO vs. SISO parallel LDO transient response.*

Note

AC-coupled, V_{OUT} = 748.5 mV

Conclusions

In this paper, I documented for the first-time a framework for MISO parallel LDOs, including a MISO parallel LDO flow chart, enabling parallel LDOs to merge power from multiple input sources to supply unified power at a single load.

I also expanded upon two topics:

- The impact of headroom voltage (or V_{IN} - V_{OUT}) on load transient response and efficiency, providing insight into how much V_{IN} is needed to meet both DC and transient operating conditions. More headroom voltage yields better transient performance but worse efficiency. Thus, you must understand the transient and efficiency requirements when optimizing an LDO to meet both specifications.
- How to configure both single as well as parallel LDOs as constant current sources. Such low-noise current sources are important in applications such as providing ultra-low-noise, high-current laser drivers.

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