TPS56C230 4.5-V to 18-V, 12-A Synchronous Step-Down Converter

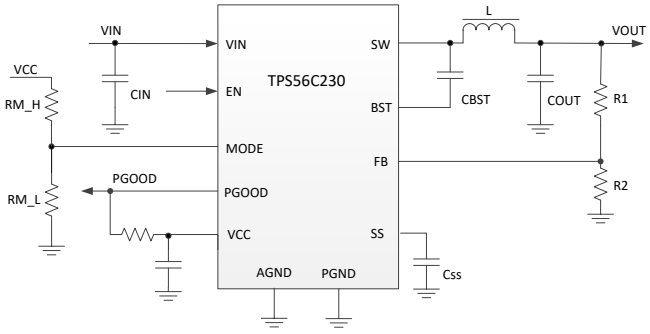
1 Features

- Input voltage range: 4.5 V to 18 V
- Output voltage range: 0.6 V to 5.5 V
- Supports 12-A continuous output current
- D-CAP3™ architecture control for fast transient response
- ±1% feedback voltage accuracy (25°C)
- Integrated 17-mΩ and 5.9-mΩ FETs
- Selectable Eco-mode™ and Forced Continuous Conductive Mode (FCCM) by MODE pin
- 500-kHz switching frequency
- Adjustable soft-start time with default 1.2 ms
- Integrated Power Good indicator
- Built-in output discharge function
- Cycle-by-cycle over current protection
- Non-latched over-voltage, under-voltage, over-temperature and under voltage lock-out protections
- -40°C to 125°C Operating Junction Temperature
- 20-pin 3.0-mm × 3.0-mm HotRod™ VQFN package
- Pin to pin compatible with 8-A *TPS568230*
- Create a Custom Design Using the TPS56C230 With the WEBENCH® Power Designer

2 Applications

- DTV and Set-top box
- PC and Industrial PC
- Wired networking
- Distributed power systems

Simplified Schematic



3 Description

The TPS56C230 is a high efficiency synchronous buck converter with integrated FETs. System designers can use the device in a wide variety of applications since it draws low standby current and requires few external components.

The TPS56C230 employs D-CAP3 control that provides fast transient response and excellent line and load regulation with internal compensation. It also has a proprietary circuit that enables the device to support low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors.

TPS56C230's MODE pin can be used to set Eco-mode or FCCM mode for light-load operation. Eco-mode maintains high efficiency during light load operation, and FCCM mode operations keeps output ripple small at light load. The device supports both internal and external soft-start time option. It has an internal fixed soft-start time 1.2 ms, but if the application needs a longer soft-start time, the external SS pin can be used to achieve it by connecting a external capacitor.

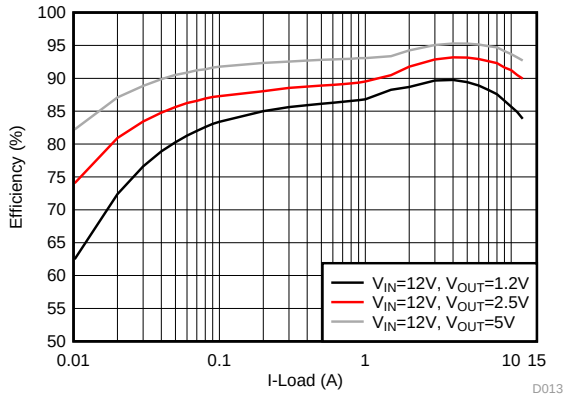
The TPS56C230 integrates power good indicator and provides output discharge function. It provides complete protection including OVP, UVP, OCP, OTP and UVLO. The device is available in a 20-pin 3.0-mm x 3.0-mm HotRod package and the junction temperature is specified from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS56C230	VQFN (20)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Output Current Eco-mode



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2019) to Revision A	Page
• Changed marketing status from Advance Information to production data..	1

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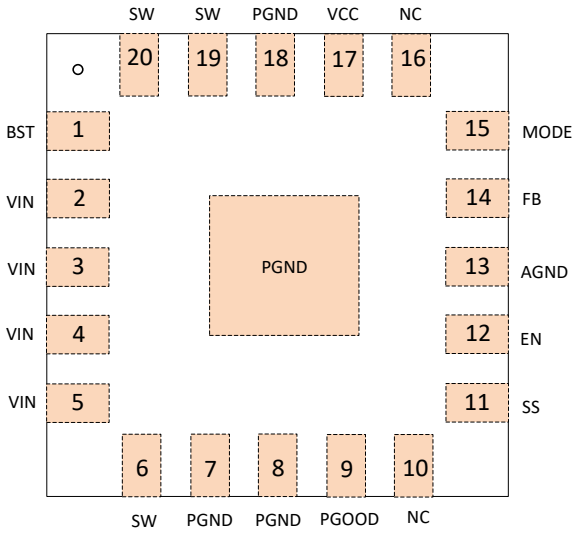
5 Pin Configuration and Functions

RJE Package
20-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	1	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BST and SW, 0.1 uF is recommended.
VIN	2,3,4,5	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
SW	6,19,20	O	Switching node connection to the inductor and bootstrap capacitor for buck. This pin voltage swings from a diode voltage below the ground up to input voltage of buck.
PGND	7,8,18,Pad	G	Power GND terminal for the controller circuit and the internal circuitry.
PGOOD	9	O	Open drain power good indicator. It is asserted low if output voltage is out of PG threshold, over voltage or if the device is under thermal shutdown, EN shutdown or during soft start.
SS	11	I	Soft-Start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the soft-start time is about 1.2ms.
NC	10,16		Not connect. Can be connected to GND plane for better thermal achieved.
EN	12	I	Enable input of buck converter
AGND	13	G	Ground of internal analog circuitry. Connect AGND to GND plane with a short trace.
FB	14	I	Feedback sensing pin for Buck output voltage. Connect this pin to the resistor divider between output voltage and AGND.
MODE	15	I	Light load operation mode selection pin. Connect this pin to a resistor divider from VCC and AGND for different MODE options shown in Table 1
VCC	17	O	The driver and control circuits are powered from this voltage. Decouple with a minimum 1 μF ceramic capacitor as close to VCC as possible.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Input voltage	VIN	–0.3	20	V
		BST	–0.3	25	V
		BST-SW	–0.3	6	V
		EN, MODE, FB, SS	–0.3	6	V
		PGND, AGND,	–0.3	0.3	V
	Output voltage	SW	–1	20	V
		SW (10-ns transient)	–3	22	V
		PGOOD	–0.3	6	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22- V C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Input voltage	VIN	4.5	18	V
		BST	–0.3	23.5	V
		BST-SW	–0.3	5.5	V
		EN, MODE, FB, SS	–0.3	5.5	V
		PGND, AGND	–0.3	0.3	V
	Output voltage	SW	–1	18	V
		PGOOD	–0.3	5.5	V
I_{OUT}	Output current			12	A
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS56C230 RJE (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	42.3	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance (4-layer custom board) (2)	28.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.
(2) 70 mm x 70 mm, 4 layers, thickness: 1.5 mm. 2 oz. copper traces located on the top and bottom of the PCB. 4 thermal vias in the PowerPAD area under the device package.

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Thermal Information (continued)

THERMAL METRIC(1)		TPS56C230 RJE (VQFN) 20 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	12.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.1	°C/W

6.5 Electrical Characteristics

T_J =-40°C to 125°C, V_{VIN} = 12 V, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
VIN	Input voltage range		4.5		18	V
I_{VIN}	Non-switching supply current	No load, V_{EN}=5V		400		μA
I_{VINSDN}	Shutdown supply current	No load, V_{EN}=0V		2		μA
VCC OUTPUT						
V_{CC}	VCC output voltage	V_{VIN}>5.0V	4.85	5	5.15	V
		V_{VIN}=4.5V		4.5		
I_{CC}	VCC current limit		20			mA
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 125°C	591	600	609	mV
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	T_J = 25°C		500		kHz
$t_{ON(MIN)}$	SW minumum on time	T_J = 25°C		60		ns
$t_{OFF(MIN)}$	SW minimum off time	T_J = 25°C, V_{FB} = 0.5 V			180	ns
MOSFET and DRIVERS						
$R_{DS(ON)H}$	High side switch resistance	T_J = 25°C		17		mΩ
$R_{DS(ON)L}$	Low side switch resistance	T_J = 25°C		5.9		mΩ
OUTPUT DISCHARGE and SOFT START						
R_{DIS}	Discharge resistance	T_J=25°C, V_{EN}=0V		350		Ω
t_{SS}	Soft start time	Internal soft-start time,SS floating		1.2		ms
I_{SS}	Soft start charge current			5		μA
POWER GOOD						
t_{PGDLY}	PGOOD start-up delay	PGOOD from low to high		1		ms
V_{PGTH}	PGOOD threshold	VFB falling (fault)		85		%
		VFB rising (good)		90		%
		VFB rising (fault)		115		%
		VFB falling (good)		110		%
V_{PG_L}	PGOOD sink current capability	I_{OL} =4mA			0.4	V
I_{PGLK}	PGOOD leak current	V_{PGOOD} =5.5V			1	μA
CURRENT LIMIT						
I_{OCL}	Over current threshold (valley)	T_J = 25°C	14	15	16	A
		T_J = -40°C to 125°C	13	15	17.5	A
I_{NOCL}	Negative over current threshold			4		A
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage		1.2	1.3	1.4	V
V_{ENL}	EN low-level input voltage		0.9	1.1	1.2	V
I_{EN}	Enable internal pull down current	V_{EN}=0.8V		2		μA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						

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Electrical Characteristics (continued)

T_J =-40°C to 125°C, V_{VIN} = 12 V, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OVP}	OVP trip threshold			125		%
t_{OVPDLY}	OVP prop deglitch			120		us
V_{UVP}	UVP trip threshold			60		%
t_{UVPDLY}	UVP prop deglitch			256		us
t_{UVPDEL}	Output Hiccup delay relative to SS time			1.5		cycle
t_{UVPEN}	Output Hiccup enable delay relative to SS time			10.5		cycle
UVLO						
$V_{UVLOVIN}$	VIN UVLO threshold	Wake up VIN voltage		4.2	4.4	V
		Shutdown VIN voltage	3.6	3.7		
		Hysteresis VIN voltage		0.5		V
OVER TEMPERATURE PROTECTION						
T_{OTP}	OTP trip threshold(1)	Shutdown temperature		150		°C
T_{OTPHSY}	OTP hysteresis(1)	Hysteresis		20		°C

(1) Not production tested

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6.6 Typical Characteristics

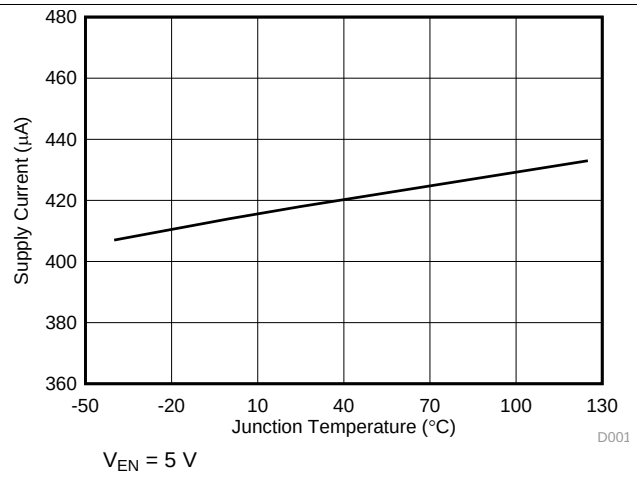

Figure 1. Supply Current vs Junction Temperature

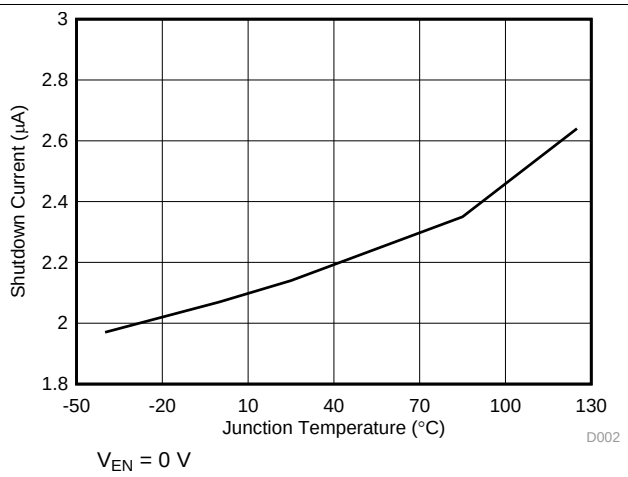

Figure 2. Shutdown Current vs Temperature

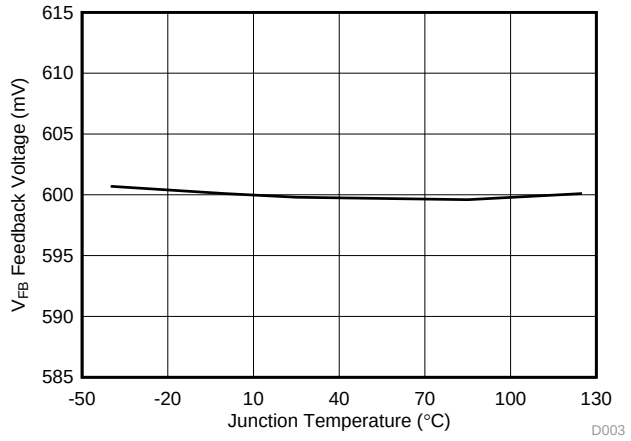

Figure 3. Feedback Voltage vs Junction Temperature

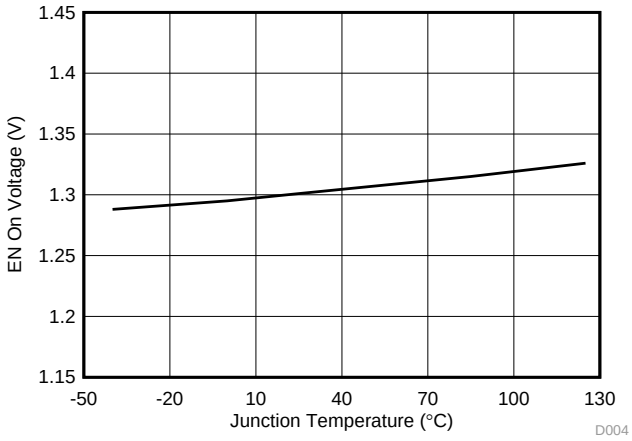

Figure 4. Enable On Voltage vs Junction Temperature

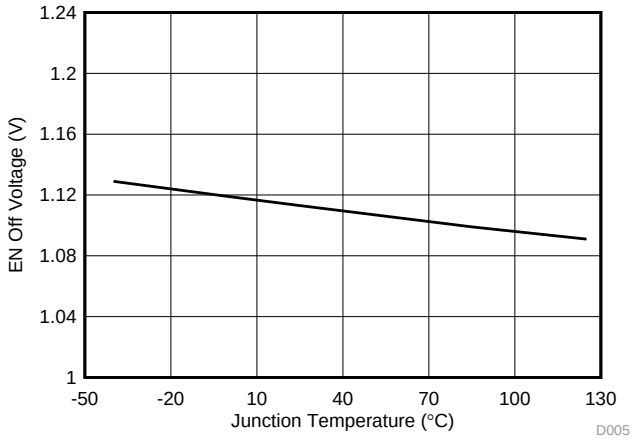

Figure 5. Enable Off Voltage vs Junction Temperature

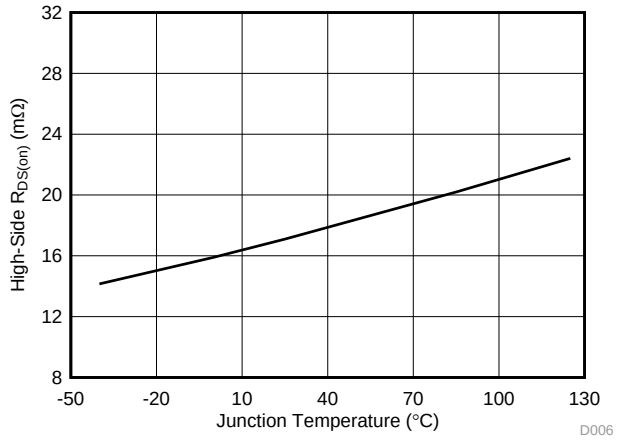

Figure 6. High-Side R_{DS}(on) vs Junction Temperature

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Typical Characteristics (continued)

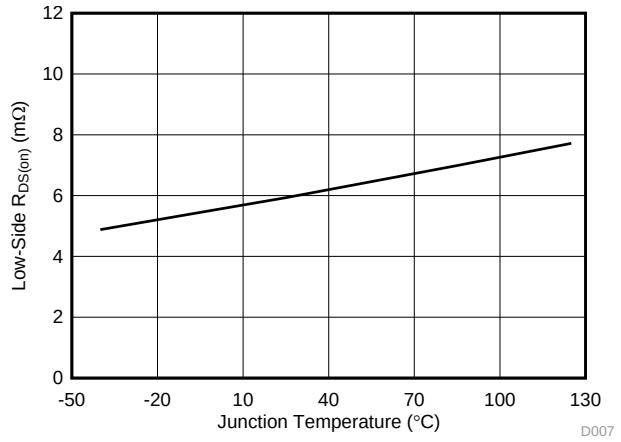

Figure 7. Low-Side $R_{DS(on)}$ vs Junction Temperature

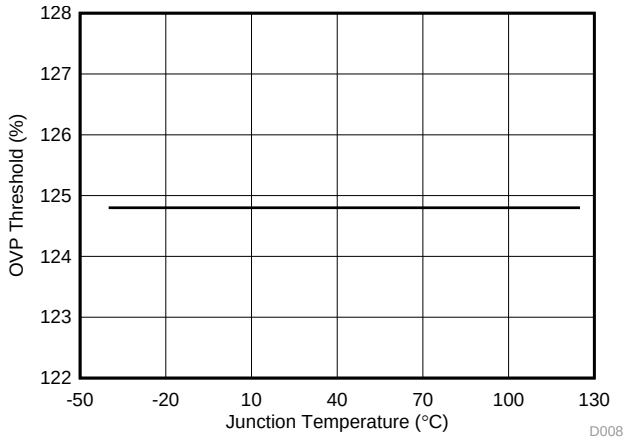

Figure 8. OVP Threshold vs Junction Temperature

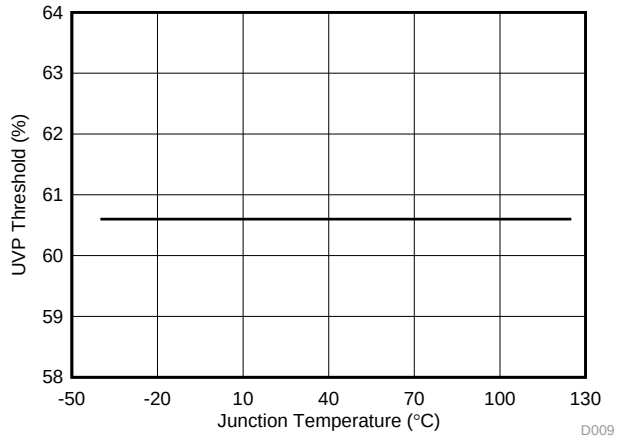

Figure 9. UVP Threshold vs Junction Temperature

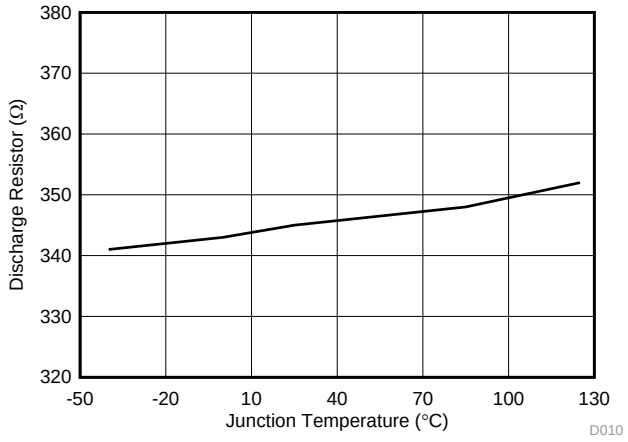

Figure 10. Discharge Resistor vs Junction Temperature

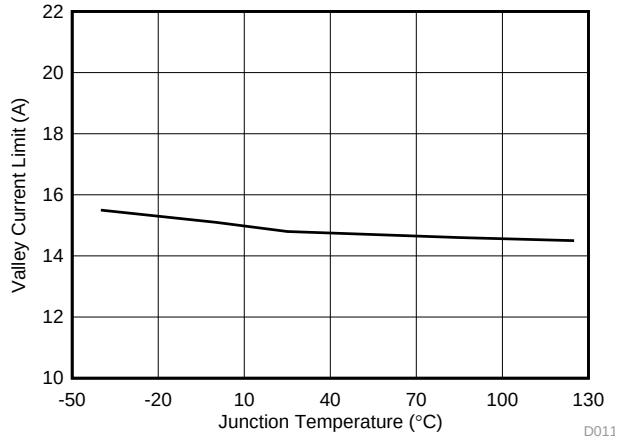

Figure 11. Valley Current Limit vs Junction Temperature

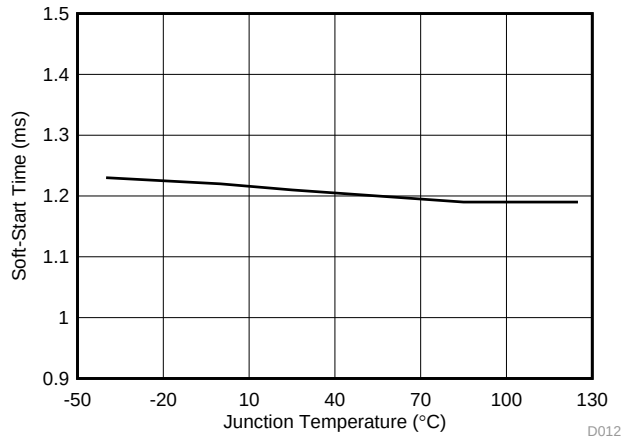

Figure 12. Soft-Start Time vs Junction Temperature

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Typical Characteristics (continued)

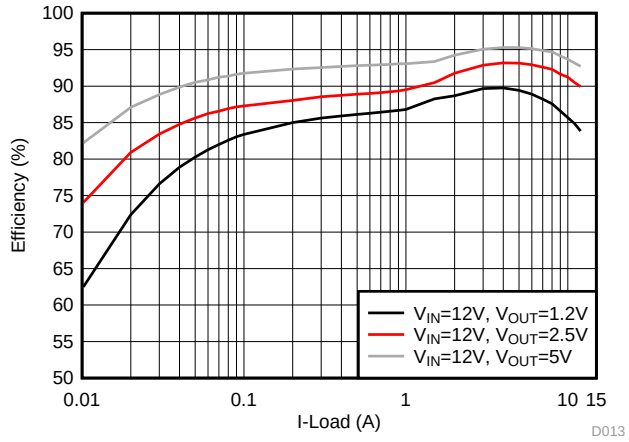


Figure 13. Efficiency vs Load Current, Eco-mode

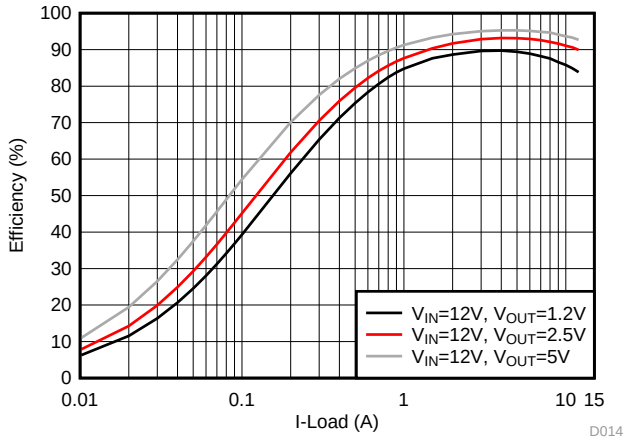


Figure 14. Efficiency vs Load Current, FCCM

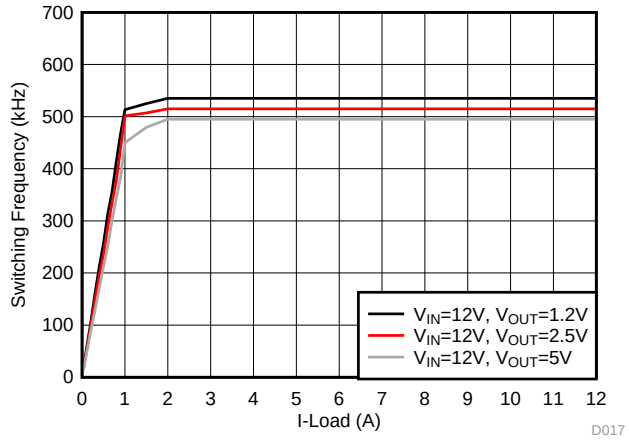


Figure 15. Switching Frequency vs Load Current, Eco-mode

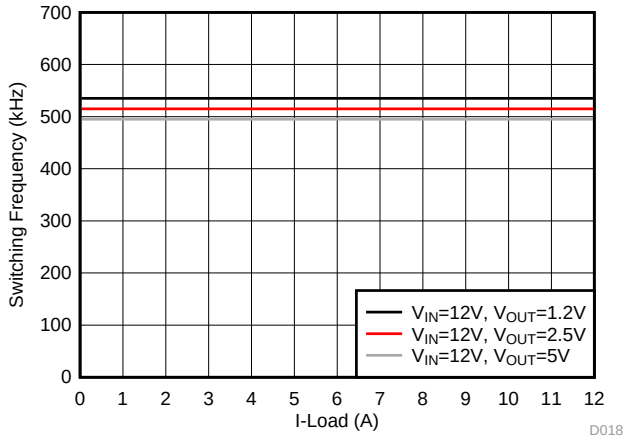


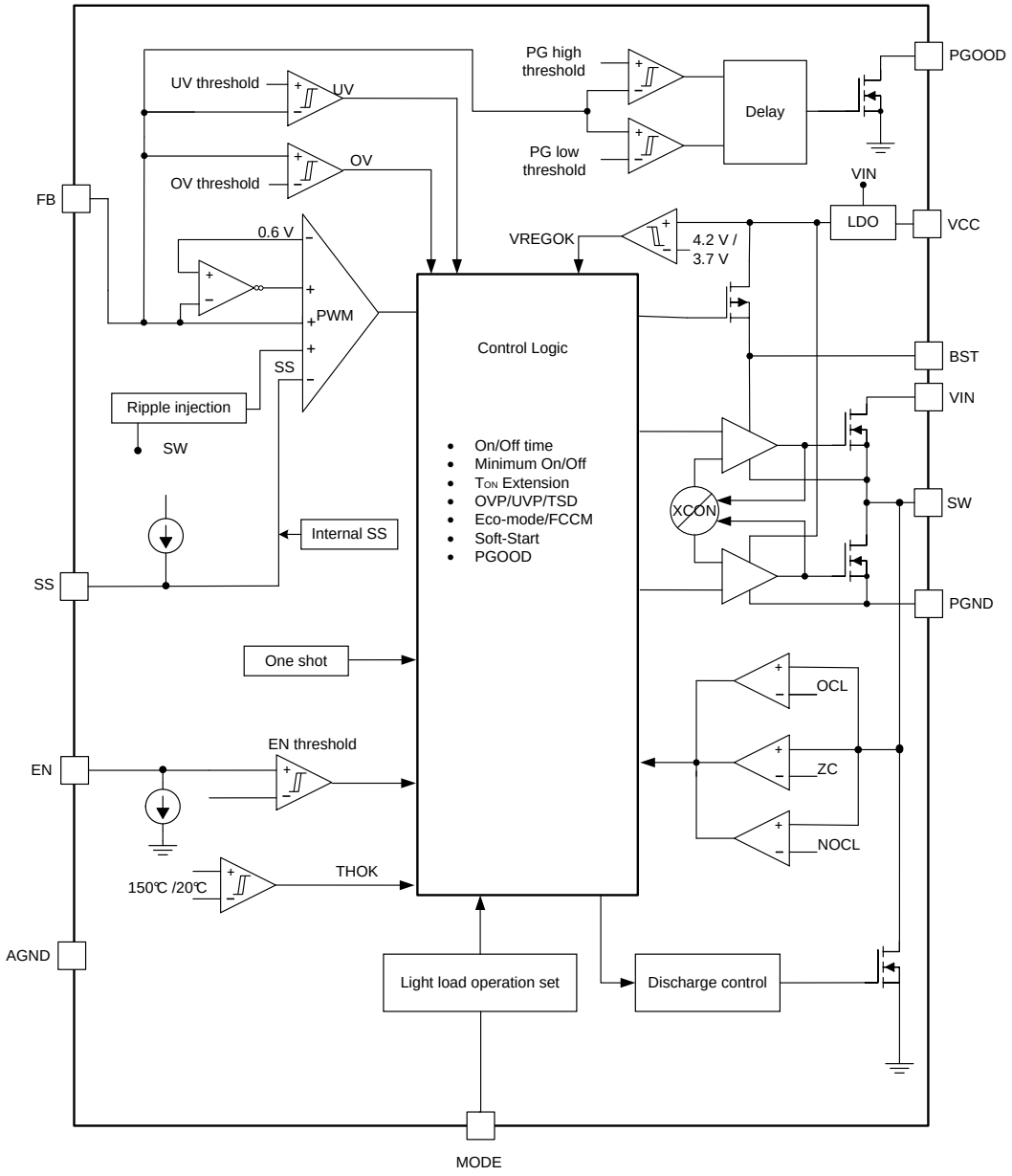
Figure 16. Switching Frequency vs Load Current, FCCM

7 Detailed Description

7.1 Overview

The TPS56C230 is high density synchronous buck converter which operates from 4.5-V to 18-V input voltage (V_{IN}), and the output voltage range is from 0.6 V to 5.5 V. It has 17-mΩ and 5.9-mΩ integrated MOSFETs that enable high efficiency up to 12 A. The device employs D-CAP3 mode control that enables low external component count, ease of design, optimization of the power design for cost, size and efficiency, and provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology supports seamless transition between CCM mode at heavy load conditions and DCM operation at light load conditions. Eco-mode allows the TPS56C230 to maintain high efficiency at light load and FCCM mode keeps the output ripple small at light load. The TPS56C230 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control

The main control loop of the buck is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 mode control. The D-CAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS56C230 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the converter output voltage, V_{OUT}, and is inversely proportional to the input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control topology.

For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS56C230 is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in Equation 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the internal output set-point resistor divider network and the internal gain of the TPS56C230. The low-frequency L-C double pole has a 180 degree drop in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and increases the phase to 90 degree one decade above the zero frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency (F_{SW}).

7.3.2 Soft Start

The TPS56C230 has an internal 1.2-ms soft-start time, and also an external SS pin is provided for setting longer soft start time if needed. When the EN pin becomes high, the soft-start function begins ramping up the reference voltage to the PWM comparator.

If the application needs a longer soft start time, it can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. The devices tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time (T_{SS}) is shown in Equation 2:

$$T_{ss}(ms) = \frac{C_{ss}\ (nF) \times V_{REF}(V)}{I_{ss}(uA)} \quad (2)$$

where

- V_{REF} is 0.6 V and I_{SS} is 5 μA

7.3.3 Large Duty Operation

The TPS56C230 can support large duty operation by its internal T_{ON} extension function. When $V_{IN}/V_{OUT} < 1.6$, and the V_{FB} is lower than internal V_{REF}, the T_{ON} will be extended to implement the large duty operation and also improve the performance of the load transient performance.

7.3.4 Power Good

The Power Good (PGOOD) pin is an open-drain output. Once the V_{FB} is between 90% and 110% of the target output voltage, the PGOOD is de-asserted and floats after a 1-ms de-glitch time. A pullup resistor of 100 kΩ is recommended to pull the voltage up to VCC. The PGOOD pin is pulled low when:

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Feature Description (continued)

- the FB pin voltage is lower than 85% or greater than 115% of the target output voltage
- in an OVP, UVP, or thermal shutdown event
- during the soft-start period.

7.3.5 Overcurrent Protection and Undervoltage Protection

The TPS56C230 has the overcurrent protection and undervoltage protection. The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, the output will shut off after a wait time of 256us and then re-start after the hiccup time (typically 10.5*Tss). When the over current condition is removed, the output voltage is recovered.

7.3.6 Overvoltage Protection

The TPS56C230 has the overvoltage protection feature and have the same implementation. When the output voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high, the output will be discharged after a wait time of 120 µs. When the over voltage condition is removed, the output voltage will be recovered.

7.3.7 Out-of-Bounds Operation

The TPS56C230 has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, OOB protection operates as an early protection mechanism. During the OOB operation, the device operates in force PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly towards the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

7.3.8 UVLO Protection

The undervoltage lockout (UVLO) protection monitors the VCC pin voltage to protect the internal circuitry from low input voltages. When the voltage is lower than UVLO threshold voltage, the device shuts off and outputs are discharged to prevent mis-operation of the device. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 500 mV (typical). This is a non-latch protection.

7.3.9 Output Voltage Discharge

The TPS56C230 has the discharge function by using internal MOSFET about 350Ω, which is connected to the output terminal SW. The discharge is slow due to the lower current capability of the MOSFET.

7.3.10 Thermal Shutdown

The TPS56C230 monitors the internal die temperature. If the temperature exceeds the threshold value (typically 150°C), the device shuts off and the output will be discharged. This is a non-latch protection, the device restarts switching when the temperature goes below the thermal shutdown threshold.

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7.4 Device Functional Modes

7.4.1 Light Load Operation

TPS56C230 has a MODE pin that can setup two different states of operation for light load operation. The light load running includes Eco-mode and FCCM mode.

7.4.2 Eco-mode™ Control

The Eco-mode control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$) can be calculated from Equation 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application). It is also important to select the inductor properly so that the valley current does not hit the negative low-side current limit.

7.4.3 Force CCM

Force CCM(FCCM) mode keeps the converter to operate in continuous conduction mode during light-load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency (FSW) is maintained at an almost constant value over the full load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

7.4.4 Mode Selection

The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in Table 1 . The voltage on the MODE pin recommended to be set by connecting this pin to the center tap of a resistor divider connected between VCC and AGND. A guideline for the top resistor (R_{M_H}) and the bottom resistor (R_{M_L}) as 1% resistors is shown in Table 1. It is recommended to choose the resistor to set the voltage at around 5%*VCC for Eco-mode or 15%*VCC for FCCM. It is important that the voltage for the MODE pin is derived from the VCC rail only since internally this voltage is referenced to detect the MODE option, and not to leave the mode pin floating. The MODE pin setting can be reset only by a VIN power cycling or EN toggle.

Table 1. MODE Pin Resistor Settings

Voltage on MODE	Recommended Resistor		LIGHT LOAD OPERATION
	R_{M_H}(kΩ)	R_{M_L} (kΩ)	
(0~10%)*VCC	330	15	Eco-mode
(10%~20%)*VCC	180	33	FCCM

Figure 17 below shows the typical start-up sequence of the device once the enable signal crosses the EN turn on threshold. After the voltage on VCC crosses the rising UVLO threshold it takes about 500us to read the first mode setting and approximately 100us from there to finish the last mode setting. The output voltage starts ramping after the mode reading is done.

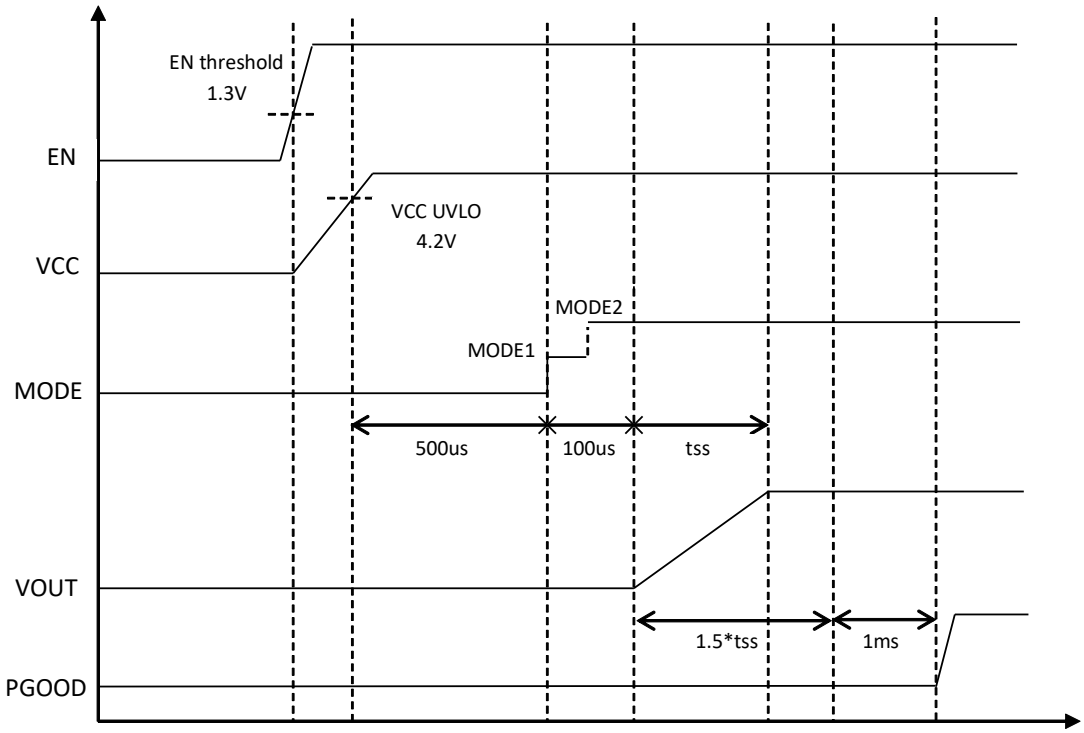

Figure 17. Power-Up Sequence

7.4.5 Standby Operation

The TPS56C230 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 2 µA when in standby condition. EN pin is pulled low internally, when floating, the part is disabled by default.

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8 Application and Implementation

NOTE

Information in the following application sections are not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The schematic of Figure 18 shows a typical application for TPS56C230 with 1.2-V output. This design converts an input voltage range of 4.5 V to 18 V down to 1.2 V with a maximum output current of 12 A.

8.2 Typical Application

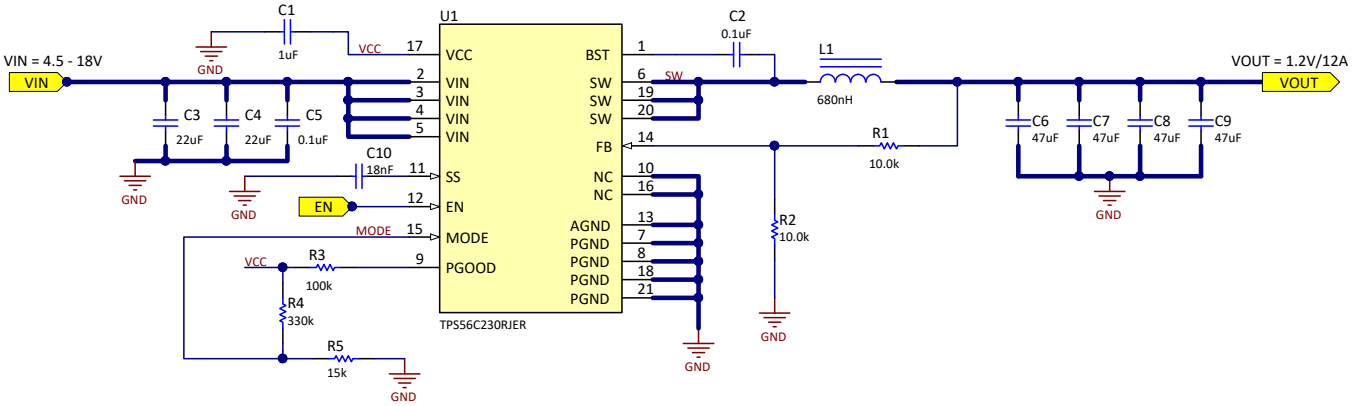

Figure 18. 1.2-V, 12-A Reference Design

8.2.1 Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1.2		V
I_{OUT}	Output current			12		A
ΔV_{OUT}	Transient response	1.2A - 10.8A load step, 2.5A/us		±5% x V_{OUT}		
V_{IN}	Input voltage		4.5	12	18	V
$V_{OUT(ripple)}$	Output voltage ripple	12A load		2% x V_{OUT}		
F_{SW}	Switching frequency			500		kHz
	Light load operating mode			Eco-mode		
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS56C230 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Set Point

To change the output voltage of the application, it is necessary to change the value of the upper feedback resistor. By changing this resistor the user can change the output voltage above 0.6 V. See Equation 4

$$V_{OUT} = 0.6 \times (1 + \frac{R_{UPPER}}{R_{LOWER}}) \quad (4)$$

8.2.2.3 MODE Selection

The light load running mode (Eco-mode or FCCM) are set by a voltage divider from VCC to GND connected to the MODE pin. See Table 1 for possible MODE pin configurations. For this design example ,the switching frequency is about 500kHz, the light load running mode is Eco-mode and the output current is 12 A.

8.2.2.4 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See Table 3 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 5 and Equation 6. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left(I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT} \right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2 \right)} \quad (5)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (6)$$

During transient and short-circuit conditions, the inductor current can increase up to the current limit of the device, so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.5 Output Capacitor Selection

After selecting the inductor, the output capacitor needs to be optimized. In D-CAP3, the regulator reacts within one cycle to the change in the duty cycle, so the good transient performance can be achieved without large amounts of output capacitance. The recommended output capacitance range is given in Table 3. Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

Table 3. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	F_{sw} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (PF)
0.6	10	0	500	0.47	66	330	-
1.2	10	10	500	0.68	66	330	-
2.5	20	63	500	1.2	66	330	
3.3	20	90	500	1.5	66	330	22-110
5.0	15	110	500	1.8	66	330	22-110

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8.2.2.6 Input Capacitor Selection

The TPS56C230 requires input decoupling capacitors on power supply input VIN, and the bulk capacitors are needed depending on the application. The minimum input capacitance required is given in Equation 7.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (7)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of 40 µF on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 8:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (8)$$

A 1-µF ceramic capacitor is needed for the decoupling capacitor on VCC pin.

8.2.3 Application Curves

Figure 19 through Figure 34 apply to the circuit of Figure 18. V_{IN} = 12 V. T_A = 25°C unless otherwise specified.

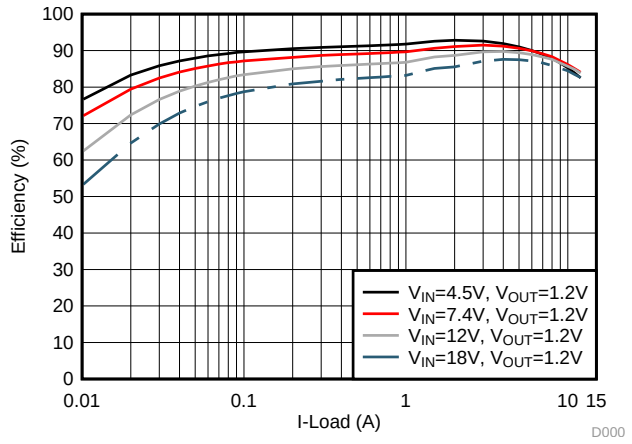


Figure 19. Efficiency Curve

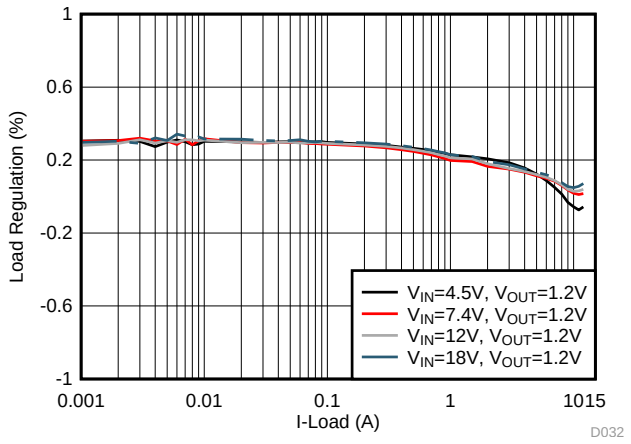
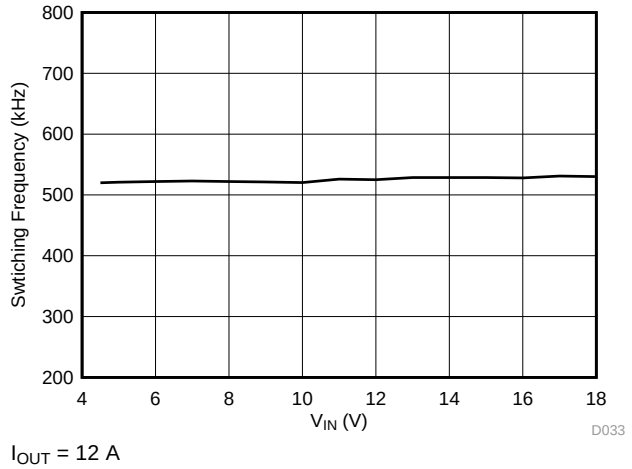


Figure 20. Load Regulation



I_{OUT} = 12 A

Figure 21. Switching Frequency vs Input Voltage

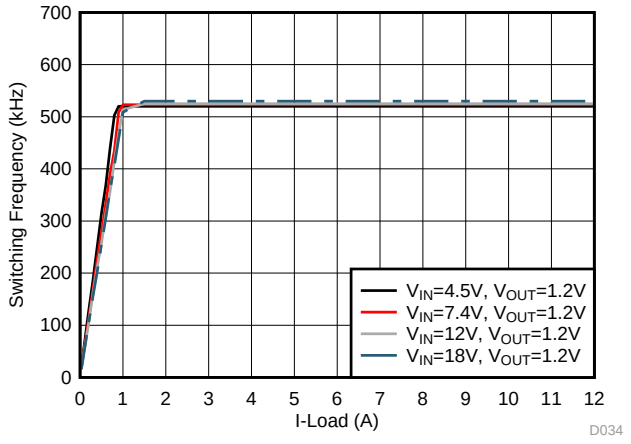
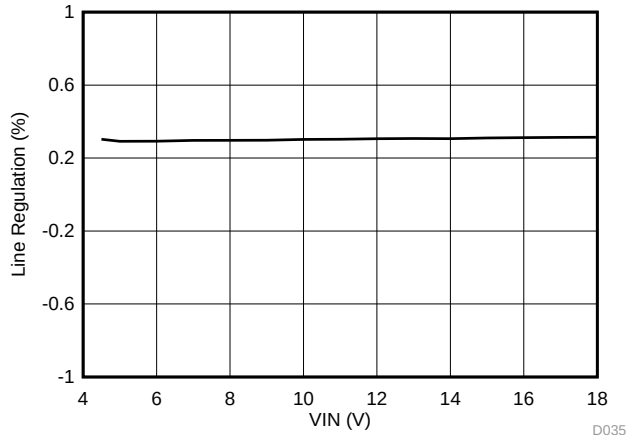
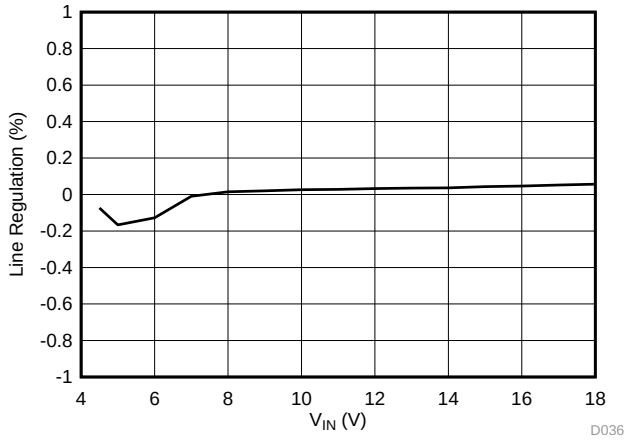


Figure 22. Switching Frequency vs Output Load



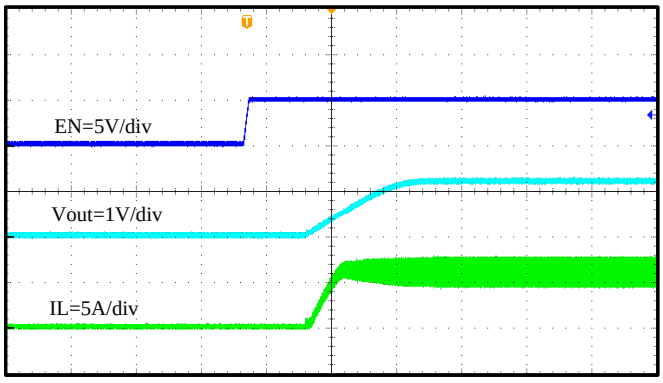
I_{OUT}=0.1A

Figure 23. Line Regulation



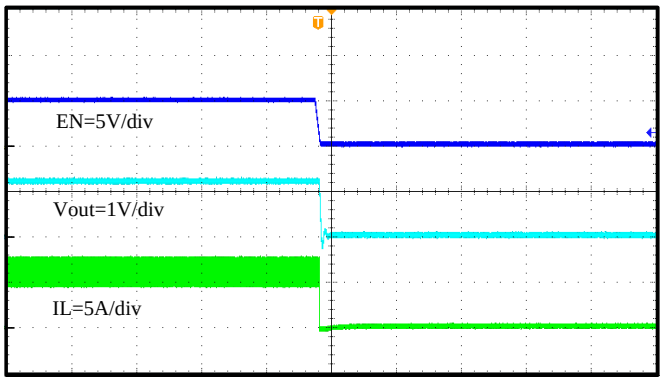
I_{OUT}=12A

Figure 24. Line Regulation



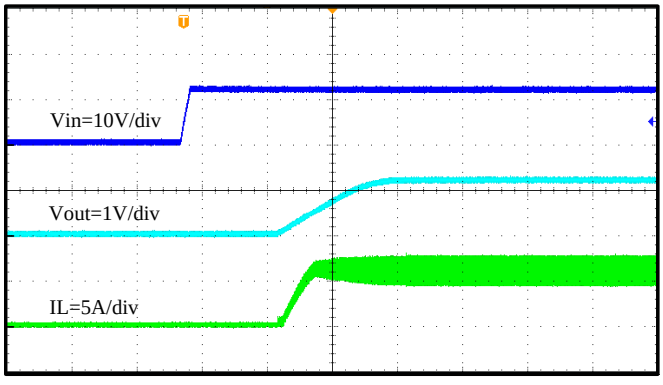
I_{OUT} = 6A

Figure 25. Start-Up Through EN



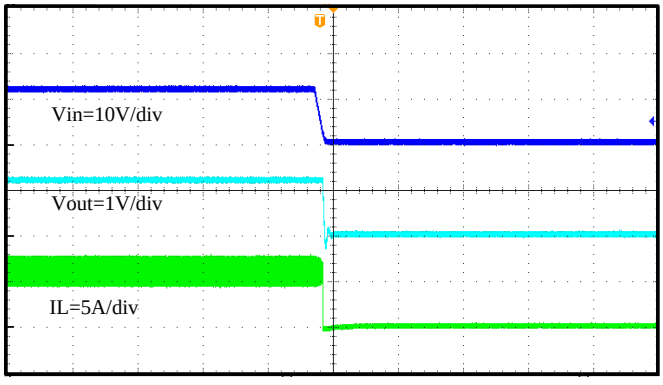
I_{OUT} = 6A

Figure 26. Shut-down Through EN



I_{OUT} = 6 A

Figure 27. Start Up Relative to V_{IN} Rising



I_{OUT} = 6 A

Figure 28. Shut Down Relative to V_{IN} Falling

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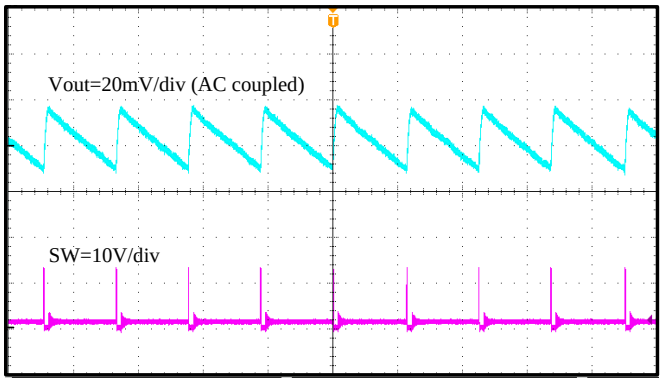
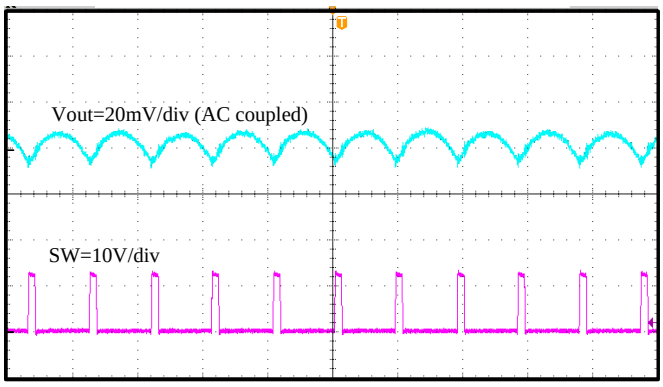


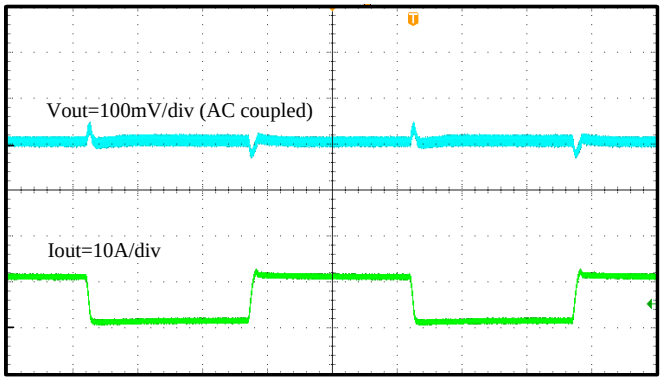
I_{OUT} = 0.1 A

Figure 29. Output Voltage Ripple



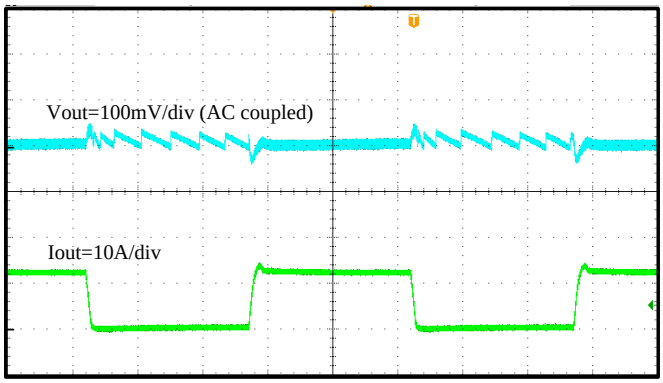
I_{OUT} = 12 A

Figure 30. Output Voltage Ripple



1.2 A to 10.8 A Slew Rate=2.5A/us

Figure 31. Transient Response



0 A to 12 A Slew Rate=2.5A/us

Figure 32. Transient Response

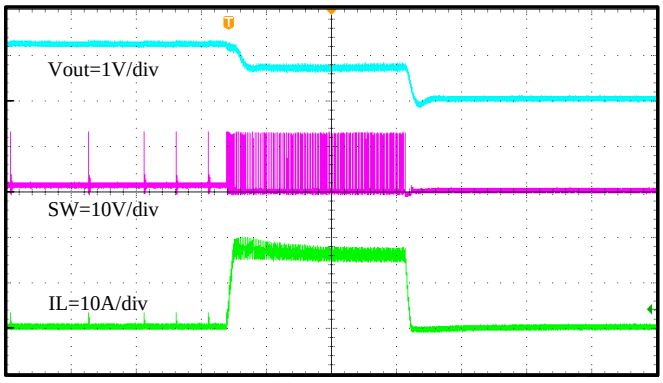


Figure 33. Normal Operation to Output Hard Short

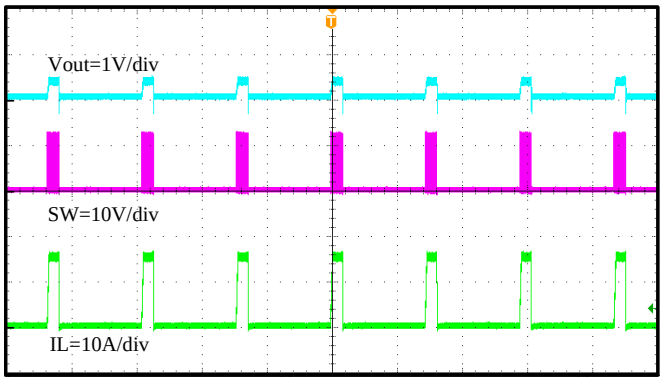


Figure 34. Output Hard Short Hiccup Protection

9 Power Supply Recommendations

The TPS56C230 is intended to be powered by a well regulated DC voltage. The input voltage range is 4.5 V to 18 V. TPS56C230 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS56C230 circuit, some additional input bulk capacitance is recommended. Typical values are 100 μF to 470 μF.

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10 Layout

10.1 Layout Guidelines

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane. 3-inch × 2.75-inch, two-layer PCB with 2-oz copper used as example.
- Place the decoupling capacitors right across VIN and VCC as close as possible.
- Place output inductors and capacitors with IC at the same layer, SW routing should be as short as possible to minimize EMI, and should be a width plane to carry big current, enough vias should be added to the GND connection of output capacitors and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane, >15 mil width trace is recommended to reduce line parasitic inductance.
- Feedback could be 20mil and must be routed away from the switching node, BST node or other high efficiency signal.
- VIN trace must be wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and GND and near input capacitors to reduce parasitic inductance and improve thermal performance

10.2 Layout Example

Figure 35 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in Figure 18.

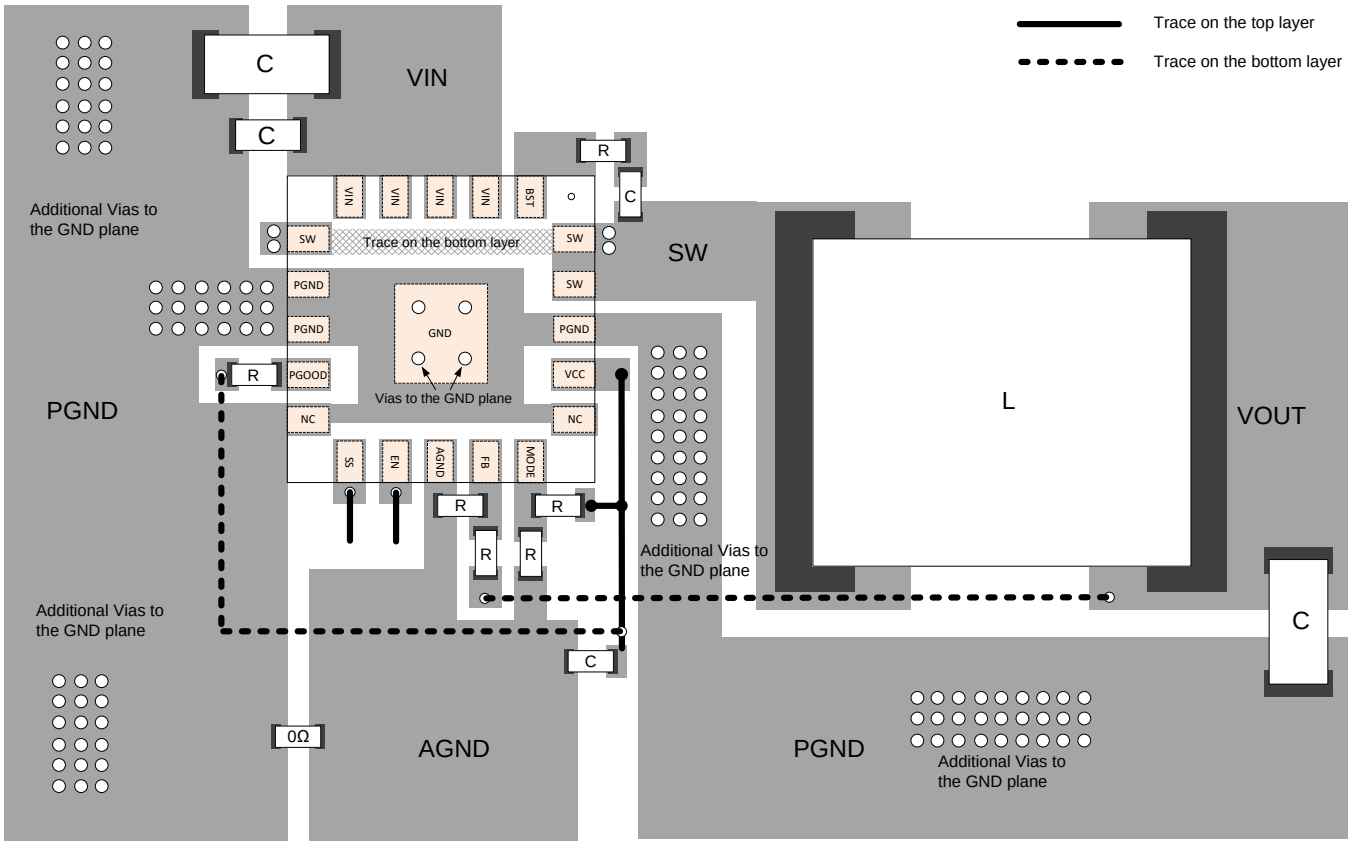

Figure 35. PCB Layout Recommendation Diagram

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS56C230 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

D-CAP3, Eco-mode, HotRod, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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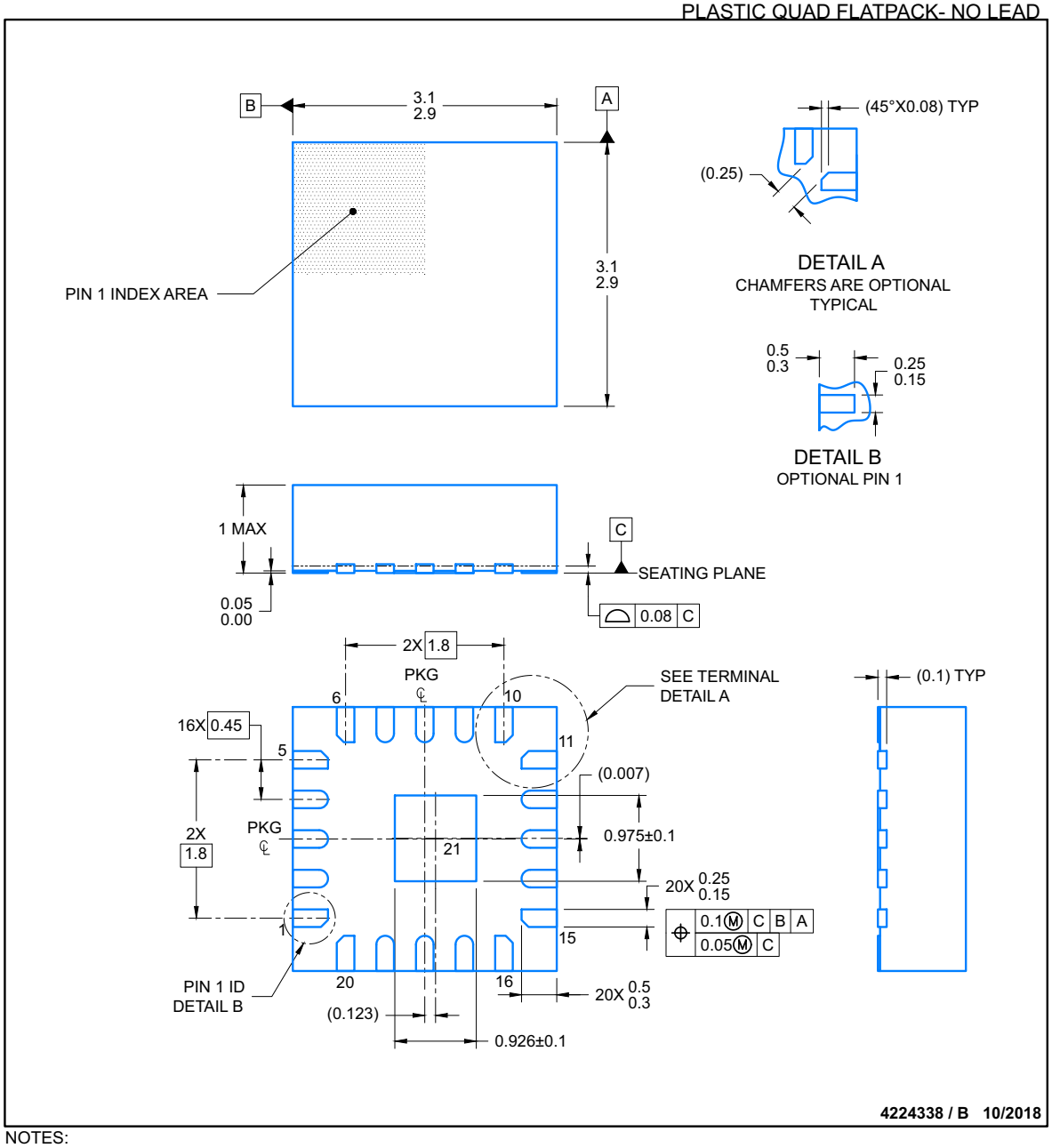
PACKAGE OUTLINE

RJE0020B — VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

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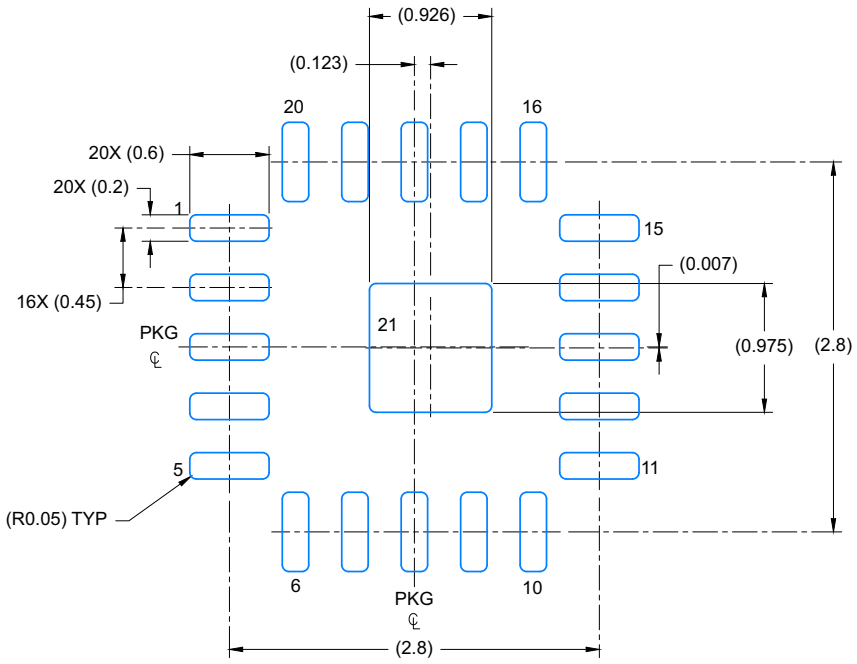
EXAMPLE BOARD LAYOUT

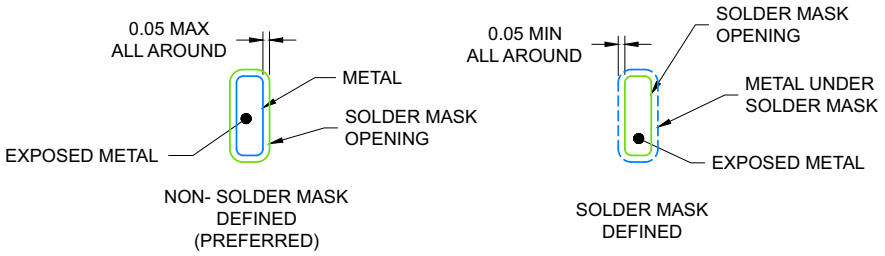
RJE0020B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224338 / B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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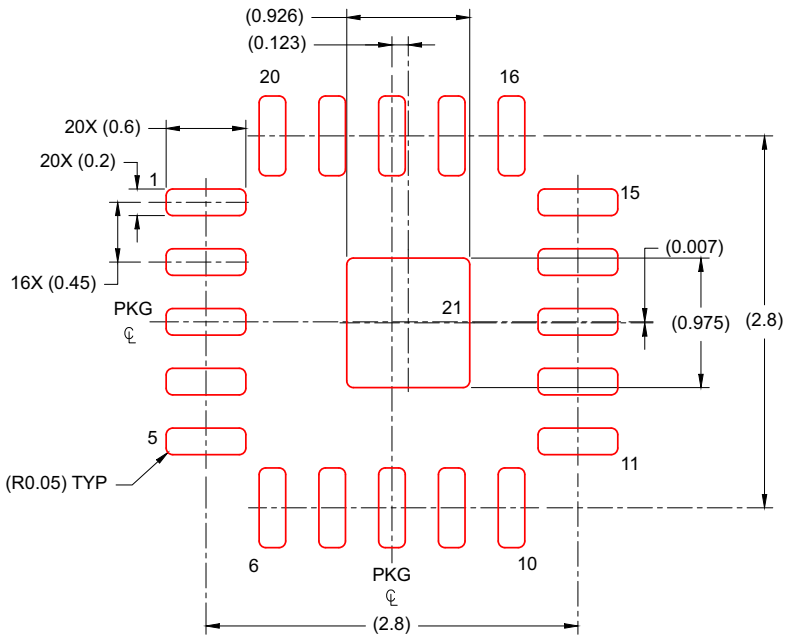
RJE0020B

EXAMPLE STENCIL DESIGN
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 20X

4224338 / B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56C230RJER	ACTIVE	VQFN-HR	RJE	20	3000	RoHS & Green	Call TI | SN | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	56C230	Samples
XTPS56C230RJET	OBSOLETE	VQFN-HR	RJE	20		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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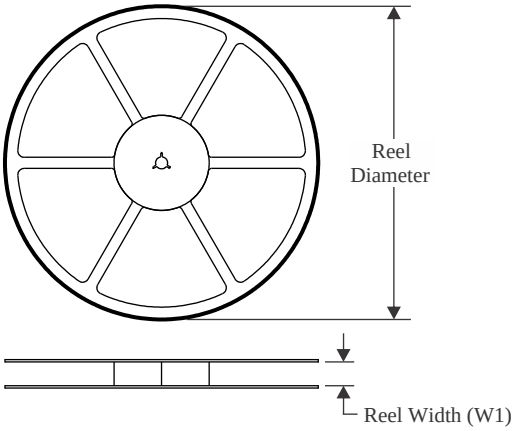
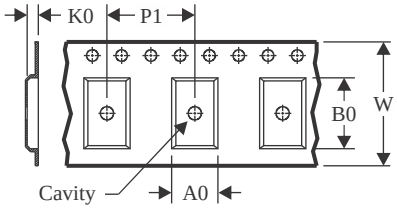
TAPE AND REEL INFORMATION

REEL DIMENSIONS

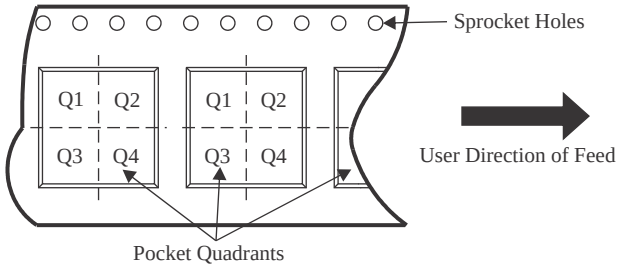


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

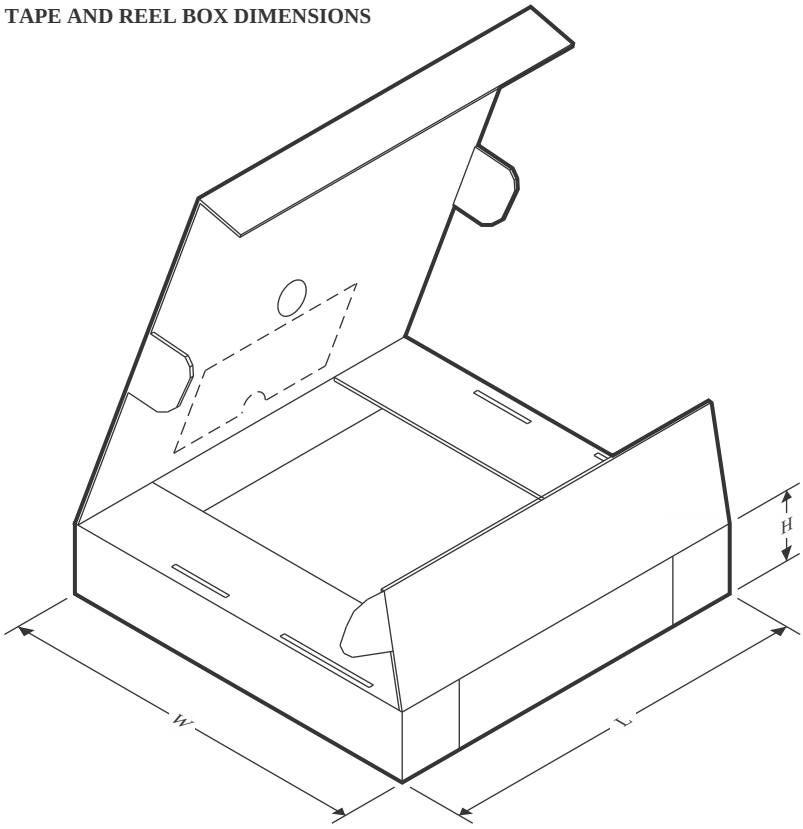
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56C230RJER	VQFN-HR	RJE	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56C230RJER	VQFN-HR	RJE	20	3000	346.0	346.0	33.0

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