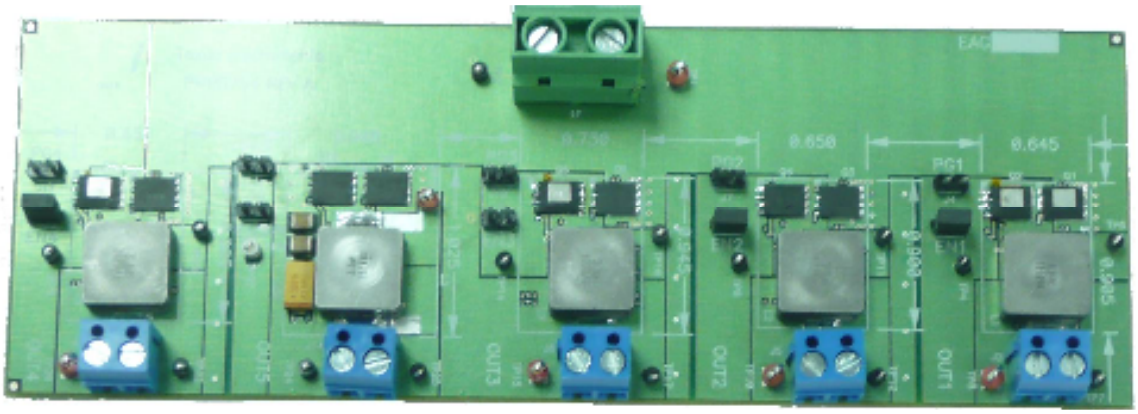
PMP5754 Test Report

Operating Parameters

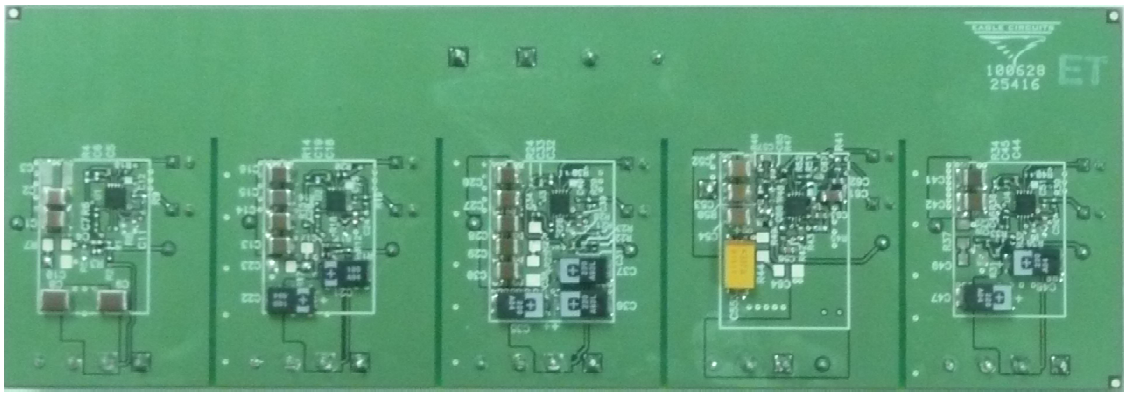
Parameter	Min	Typ	Max	Unit
V_{in}	12	18	20	V
V_{out}		4		V
		3.3		V
		2.5		V
		0.9		V
		-4		V
I_{out}	3		14	A
$F_{switching}$	300		1200	kHz

1 Board Images

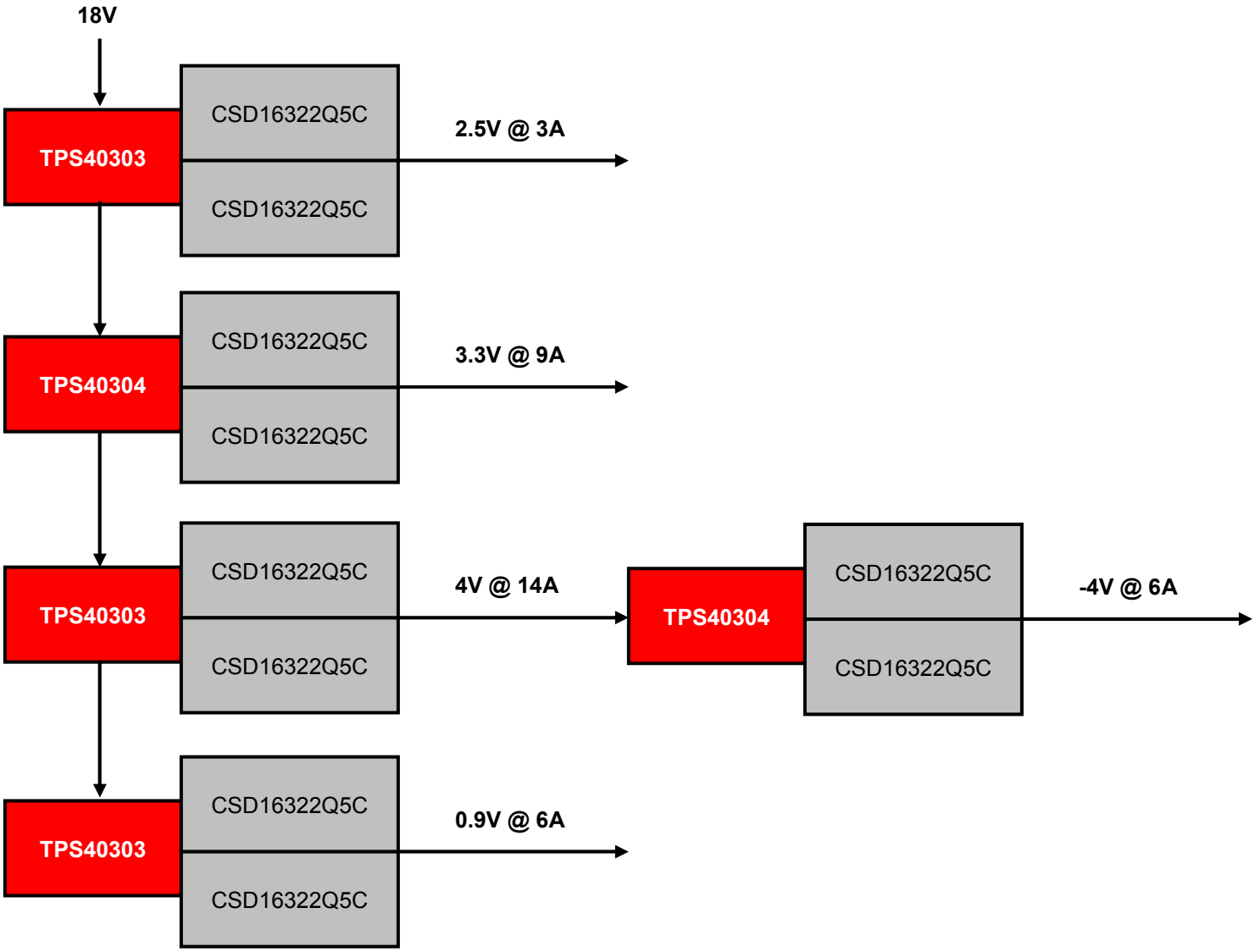
1.1 Top



1.2 Bottom



2 Block Diagram



3 TPS40303 – 4.0V @ 14A

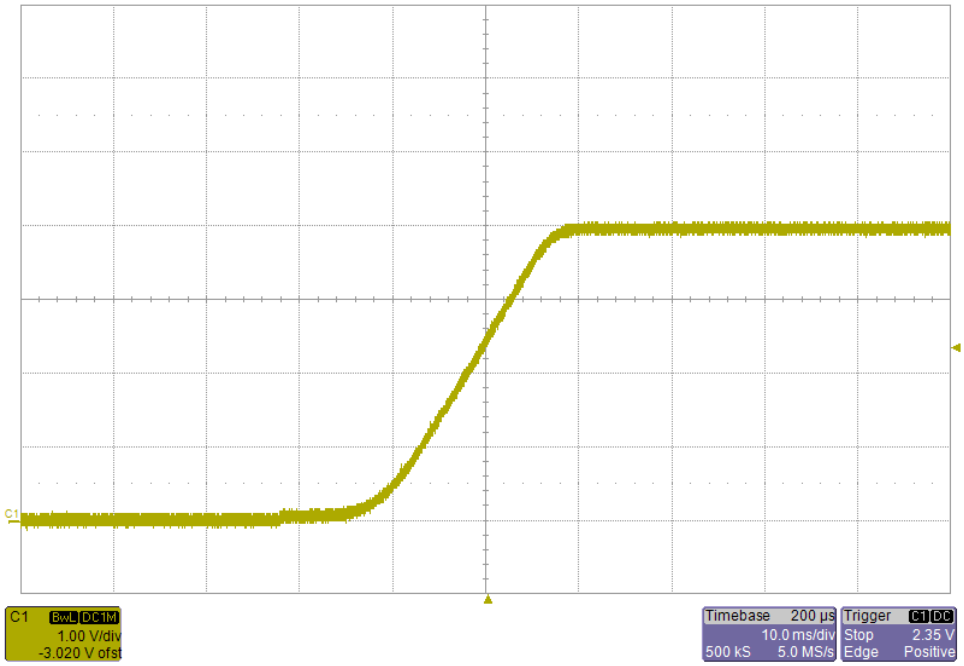
3.1 Performance Summary

Performance parameters below represent data obtained from the PMP5754 design; changes to the design, component selection or layout may result in varied performance.

Parameter	Test Conditions	Min	Typ	Max	Unit
Loop Bandwidth	V_{in}= 18V, I_{out}= 14A		29.28		kHz
Phase Margin	V_{in}= 18V, I_{out}= 14A		67.76		º
Output Voltage Ripple	I_{out}= 14A		9.5		mV
Maximum Efficiency			95		%
Load Regulation	V_{in} = 18V, I_{out}= 0A to 14A		0.4		%
Switching Frequency	I_{out}= 14A		306		kHz

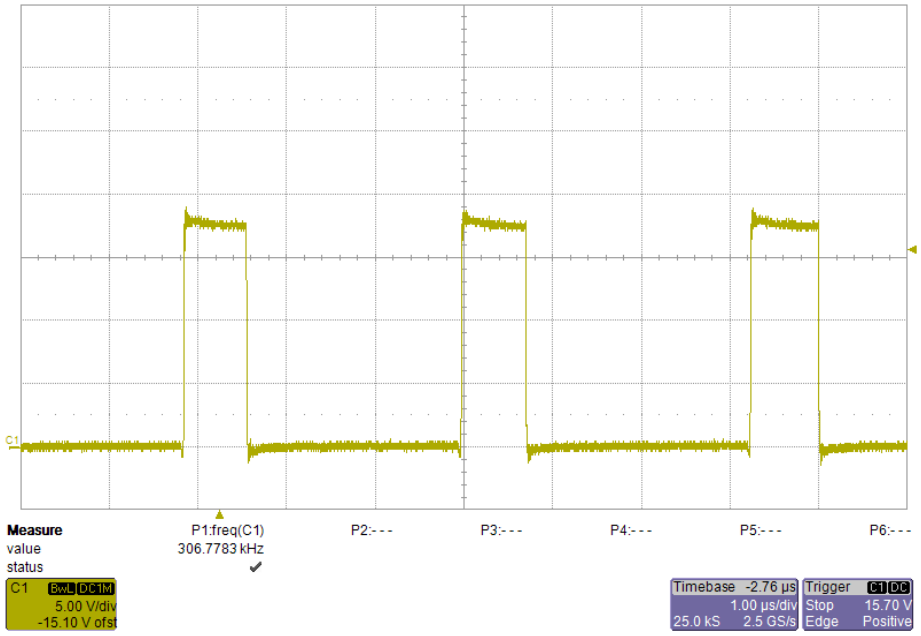
3.2 Start-up Waveform

V_{in} = 18V, V_{out} = 4.0V, I_{out} = 1A

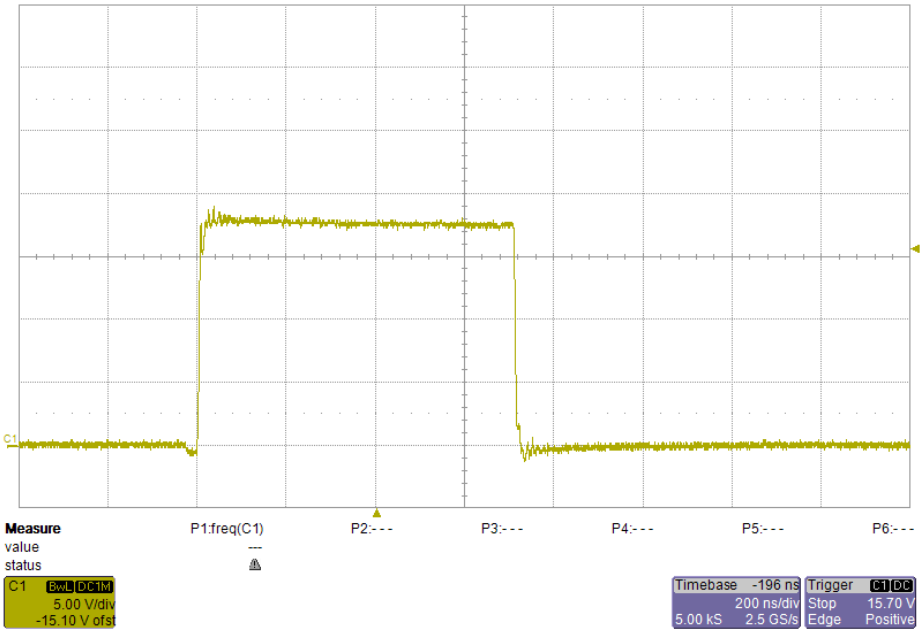


3.3 Switch Node

V_{in} = 18V, V_{out} = 4.0V, I_{out} = 14A

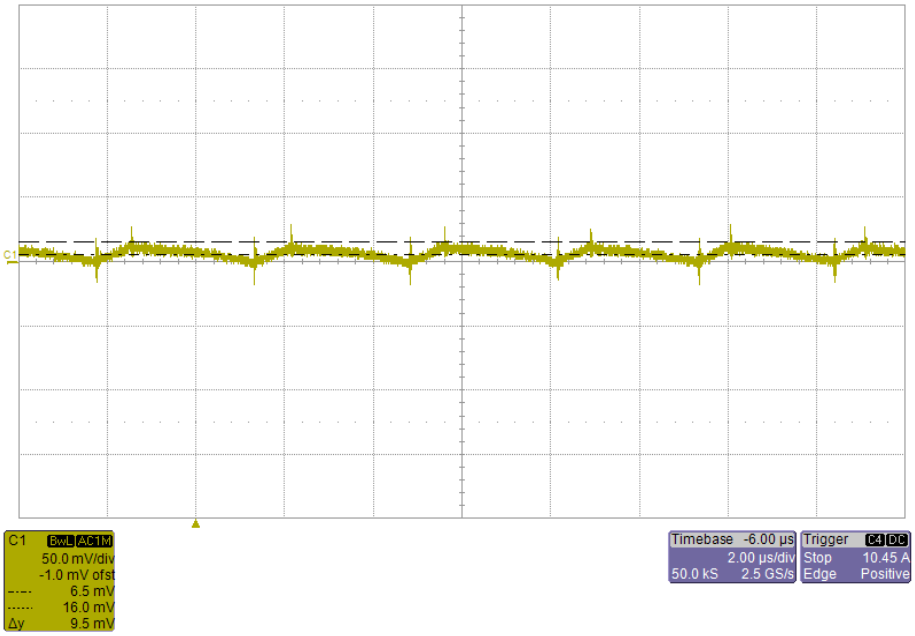


Zoom



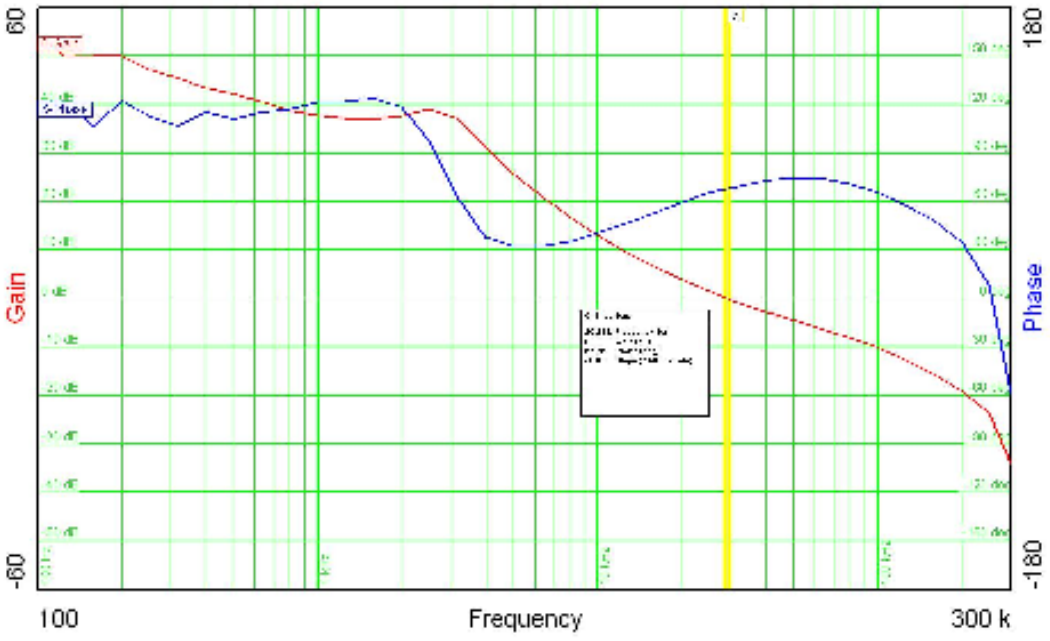
3.4 Output Voltage Ripple

V_{in} = 18V, V_{out} = 4.0V, I_{out} = 14A



3.5 Loop Response

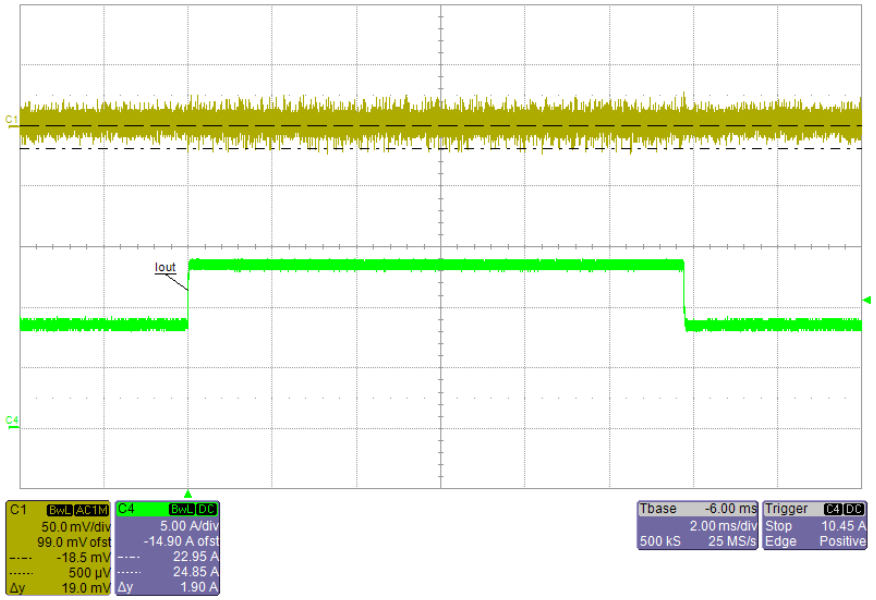
V_{in} = 18V, V_{out} = 4.0V, I_{out} = 14A



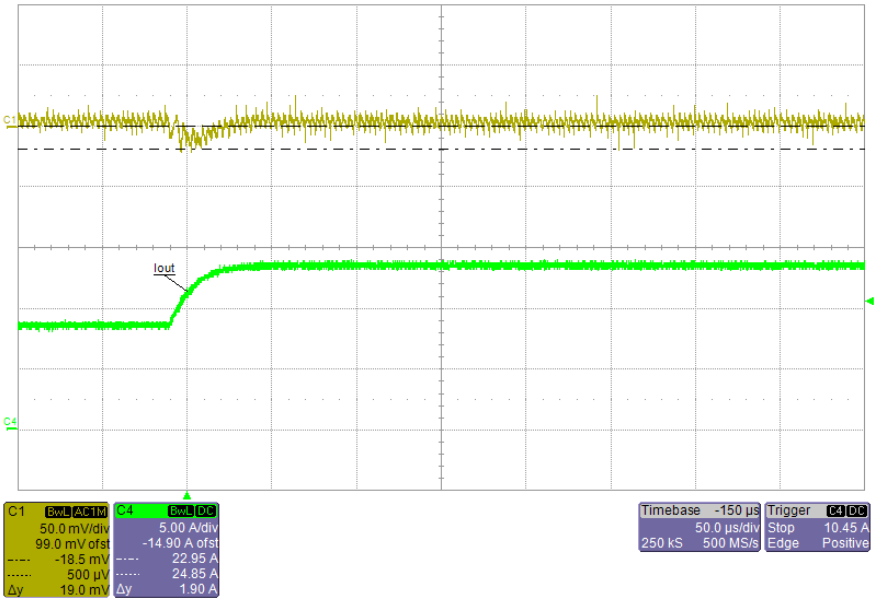
Phase Margin = 67.76 @ 29.28 kHz

3.6 Load Transient

V_{in} = 18V, V_{out} = 4.0V, I_{out} = 9A to 14A

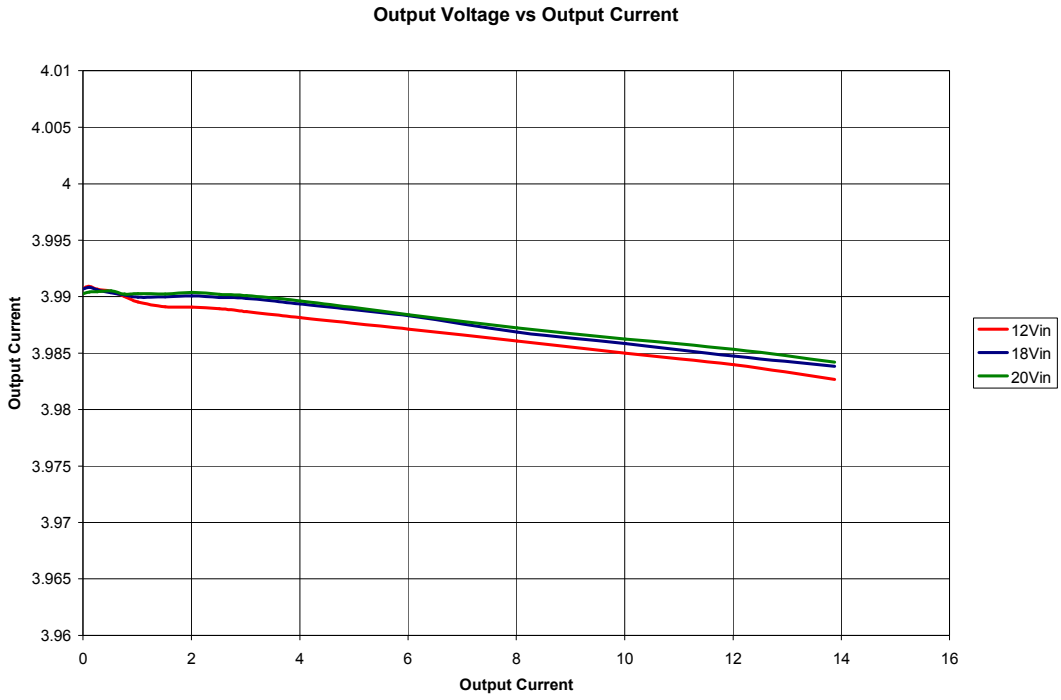


Zoom



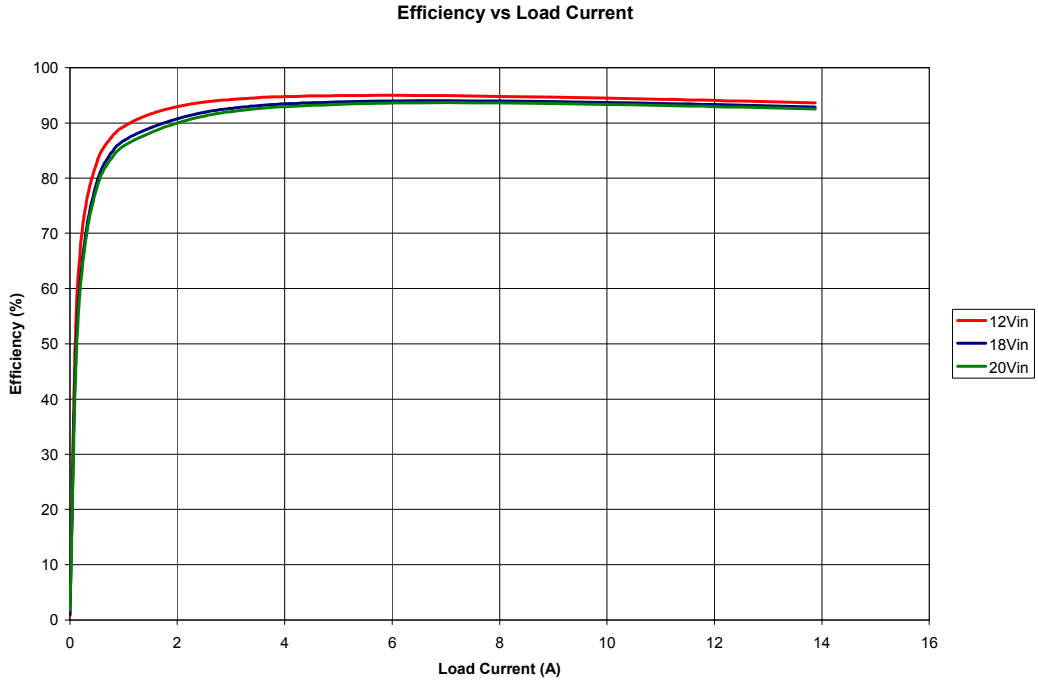
3.7 Load Regulation

V_{out} = 4.0V



3.8 Efficiency

V_{out} = 4.0V



4 TPS40304 – 3.3V @ 9A

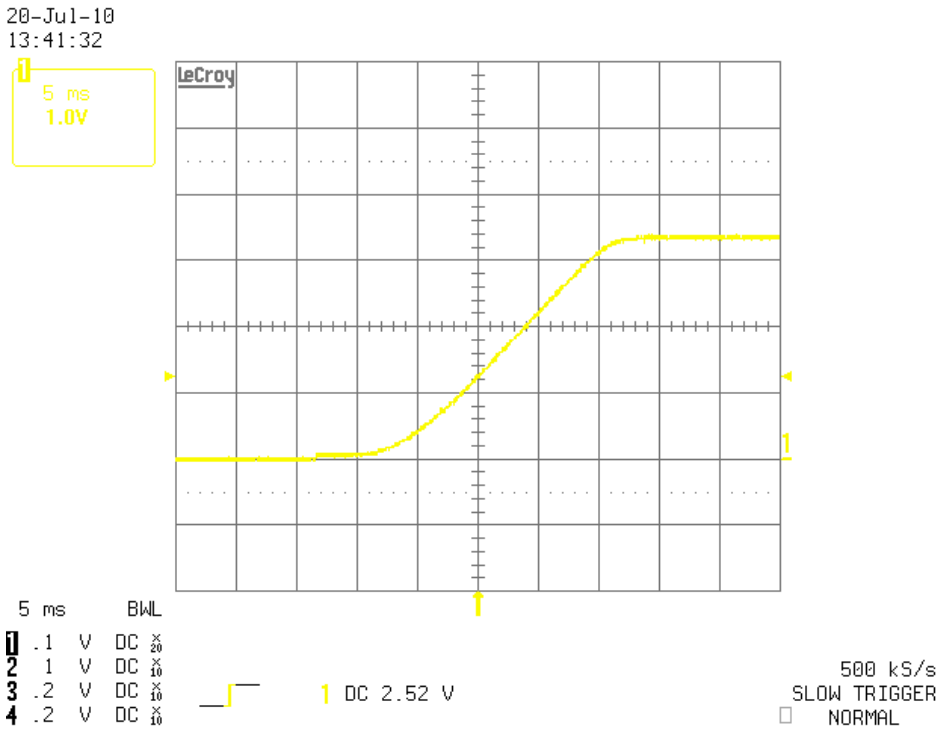
4.1 Performance Summary

Performance parameters below represent data obtained from the PMP5754 design; changes to the design, component selection or layout may result in varied performance.

Parameter	Test Conditions	Min	Typ	Max	Unit
Loop Bandwidth	V_{in}= 18V, I_{out}= 9A		70.69		kHz
Phase Margin	V_{in}= 18V, I_{out}= 9A		55.29		º
Output Voltage Ripple	I_{out}= 9A		10		mV
Maximum Efficiency			94.52		%
Load Regulation	V_{in} = 18V, I_{out}= 0A to 9A		0.9		%
Switching Frequency	I_{out}= 9A		609		kHz

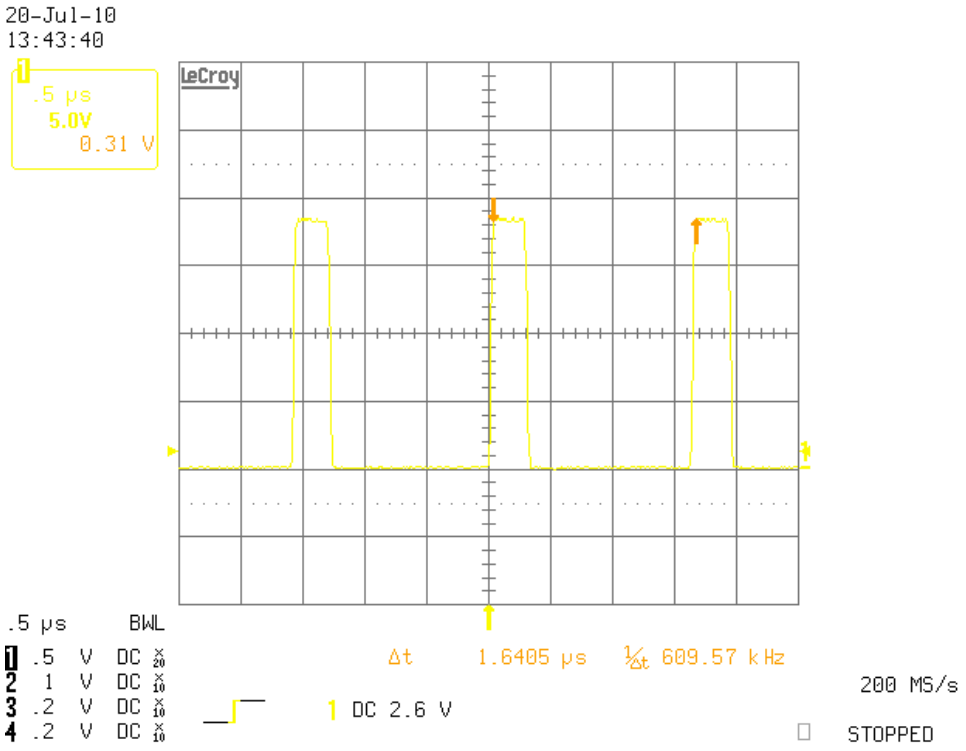
4.2 Start-up Waveform

V_{in} = 18V, V_{out} = 3.3V, I_{out} = 500mA

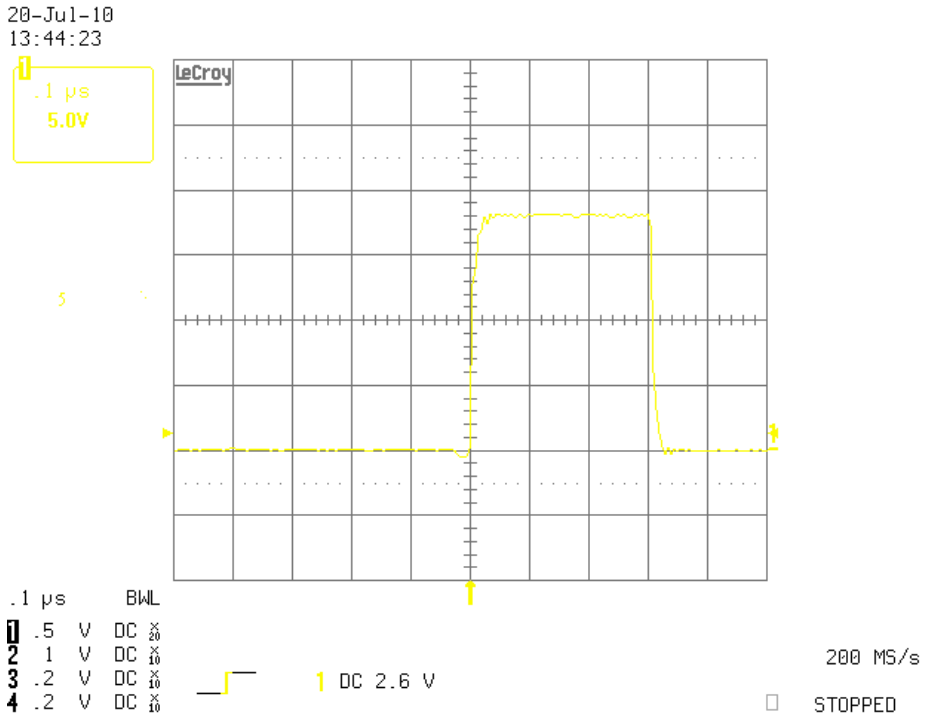


4.3 Switch Node

V_{in} = 18V, V_{out} = 3.3V, I_{out} = 9A

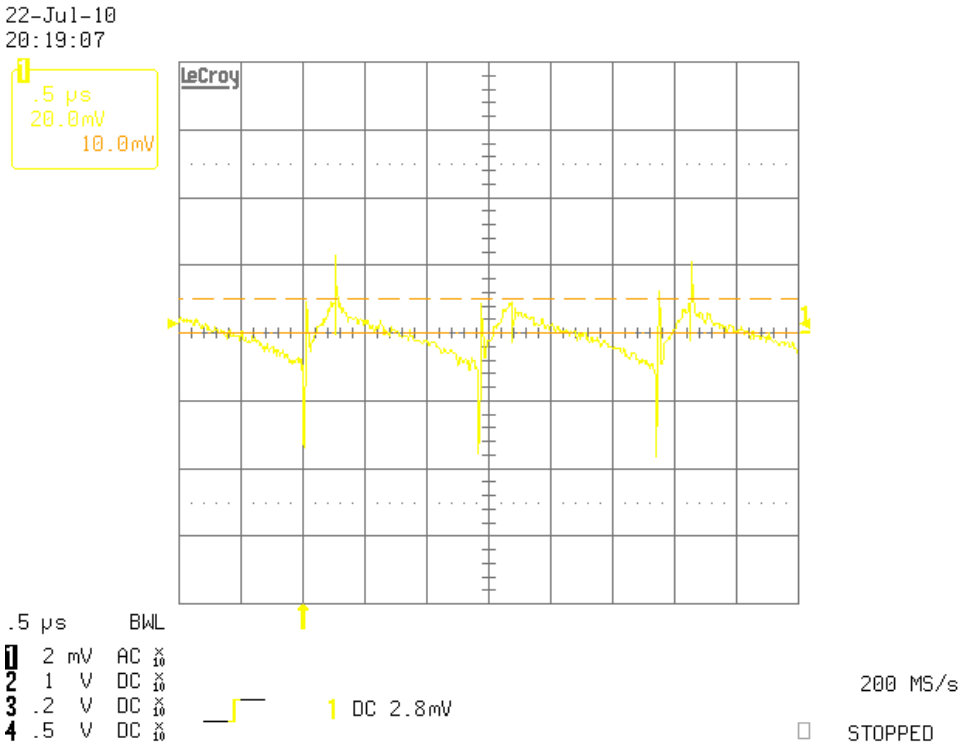


Zoom

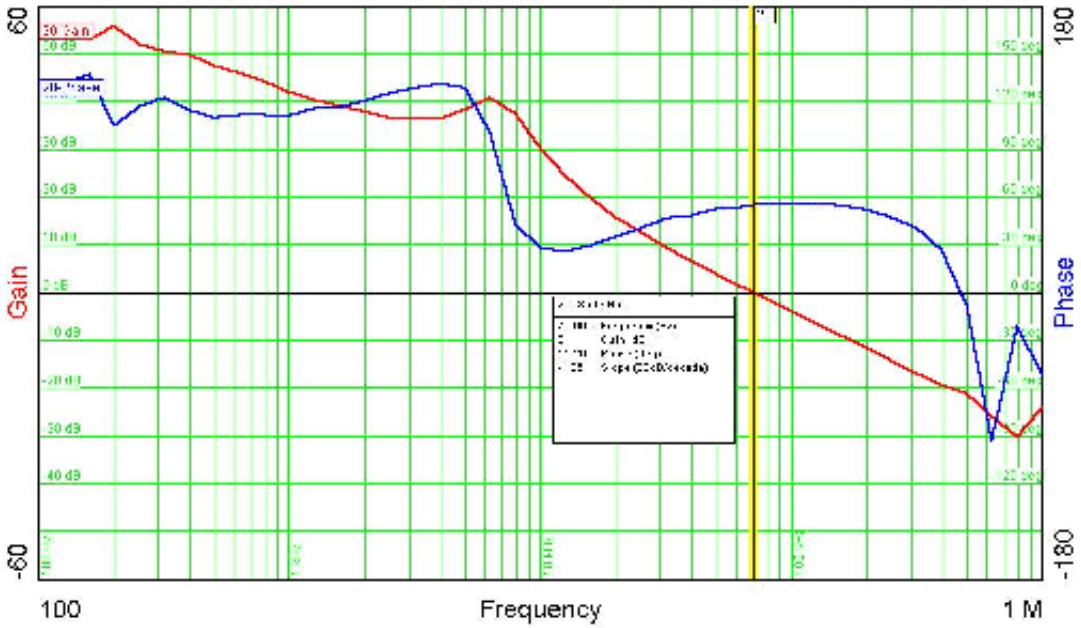


4.4 Output Voltage Ripple

V_{in} = 18V, V_{out} = 3.3V, I_{out} = 9A



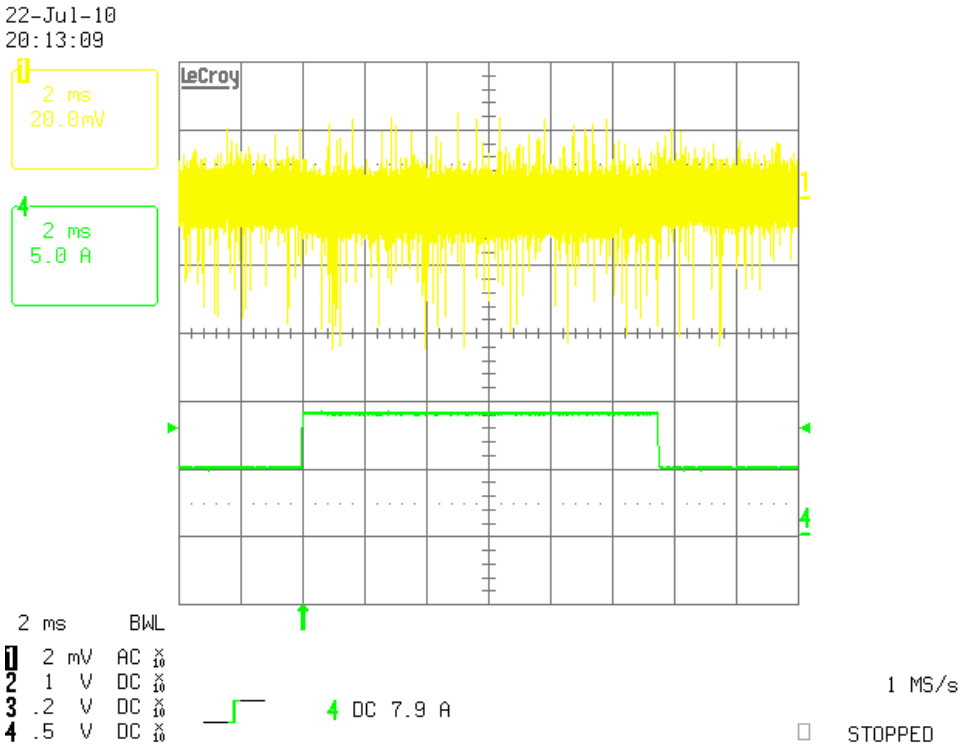
4.5 Loop Response



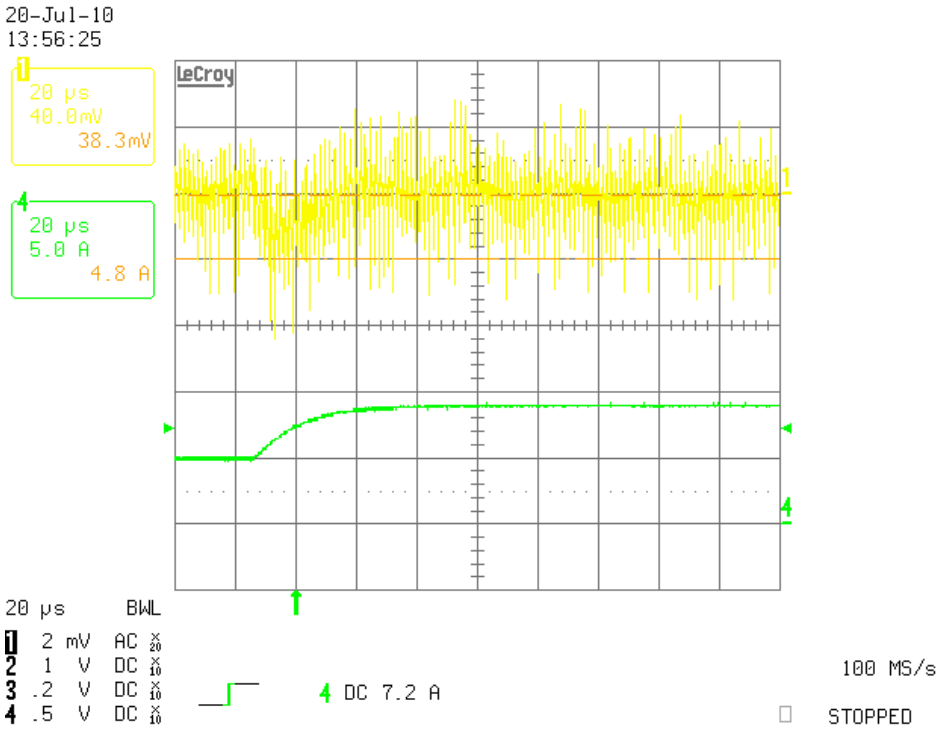
Phase Margin = 55.29 @ 70.69 kHz

4.6 Load Transient

V_{in} = 18V, V_{out} = 3.3V, I_{out} = 5A to 9A

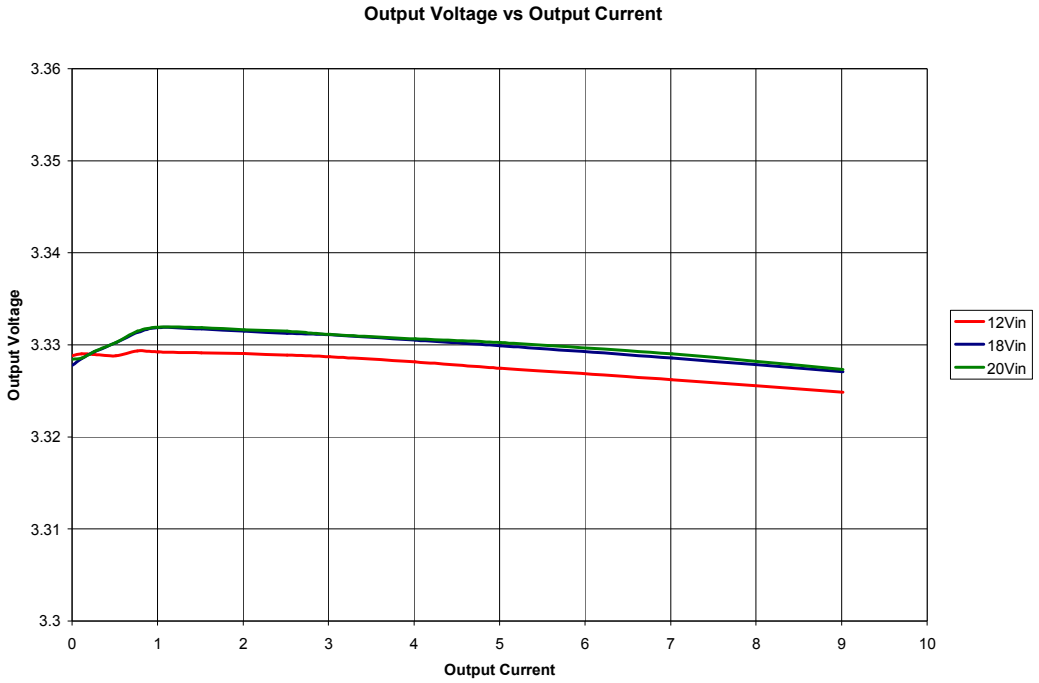


Zoom



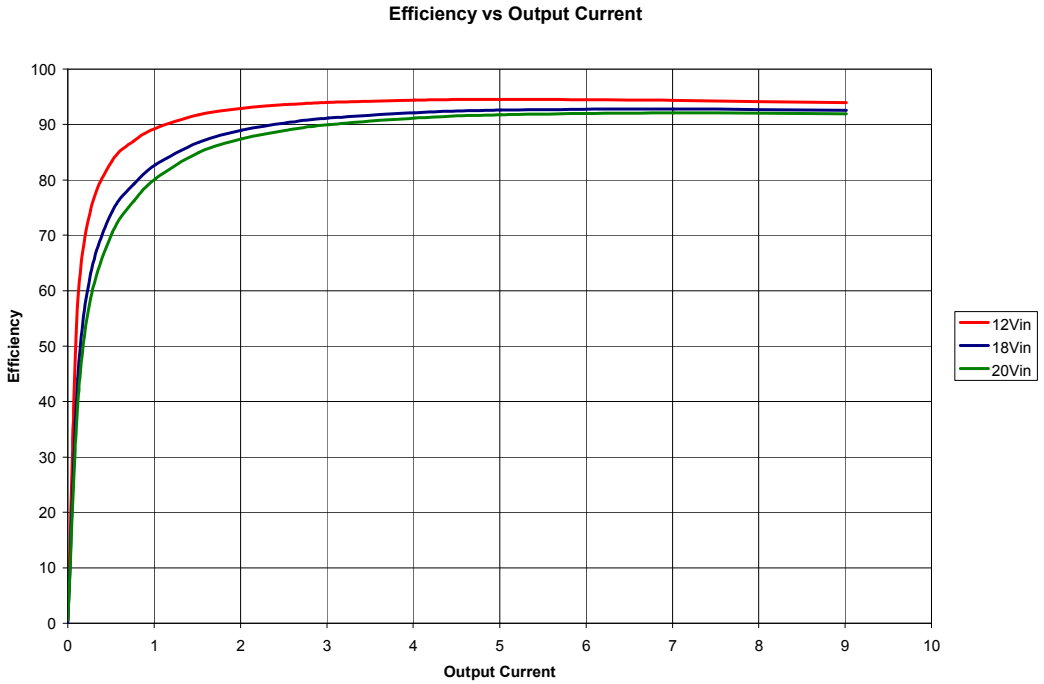
4.7 Load Regulation

V_{out} = 3.3V



4.8 Efficiency

V_{out} = 3.3V



5 TPS40304 – 2.5V @ 3A

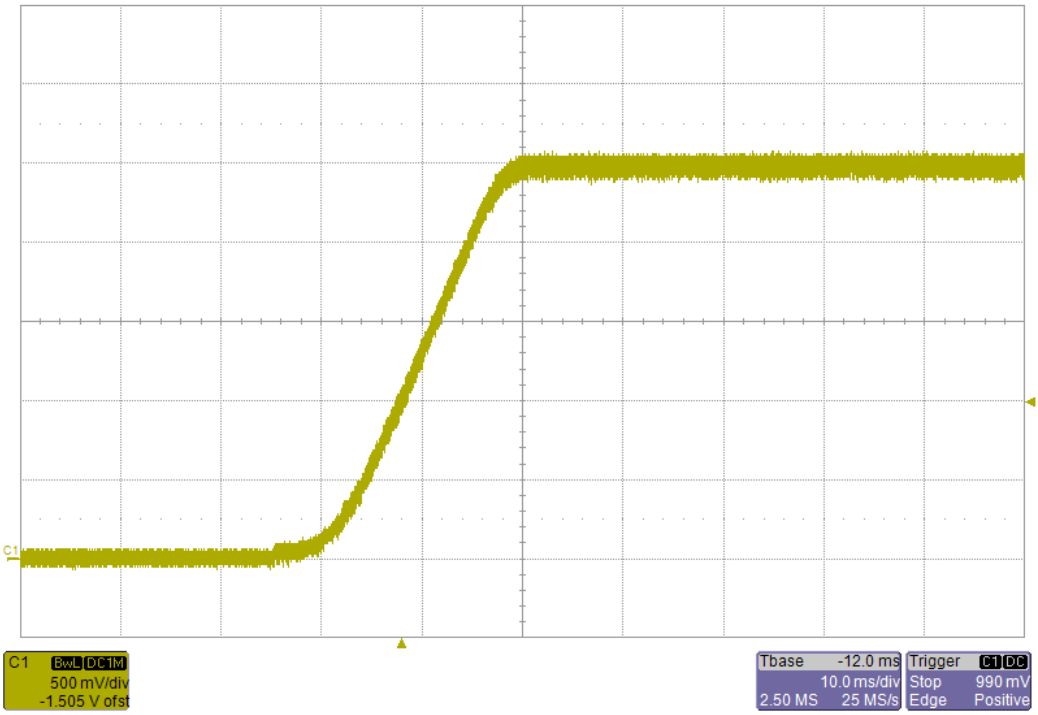
5.1 Performance Summary

Performance parameters below represent data obtained from the PMP5754 design; changes to the design, component selection or layout may result in varied performance.

Parameter	Test Conditions	Min	Typ	Max	Unit
Loop Bandwidth	V_{in}= 18V, I_{out}= 3A		72.52		kHz
Phase Margin	V_{in}= 18V, I_{out}= 3A		46.56		º
Output Voltage Ripple	I_{out}= 3A		6		mV
Maximum Efficiency			91.24		%
Load Regulation	V_{in} = 18V, I_{out}= 0A to 3A		0.4		%
Switching Frequency	I_{out}= 3A		624		kHz

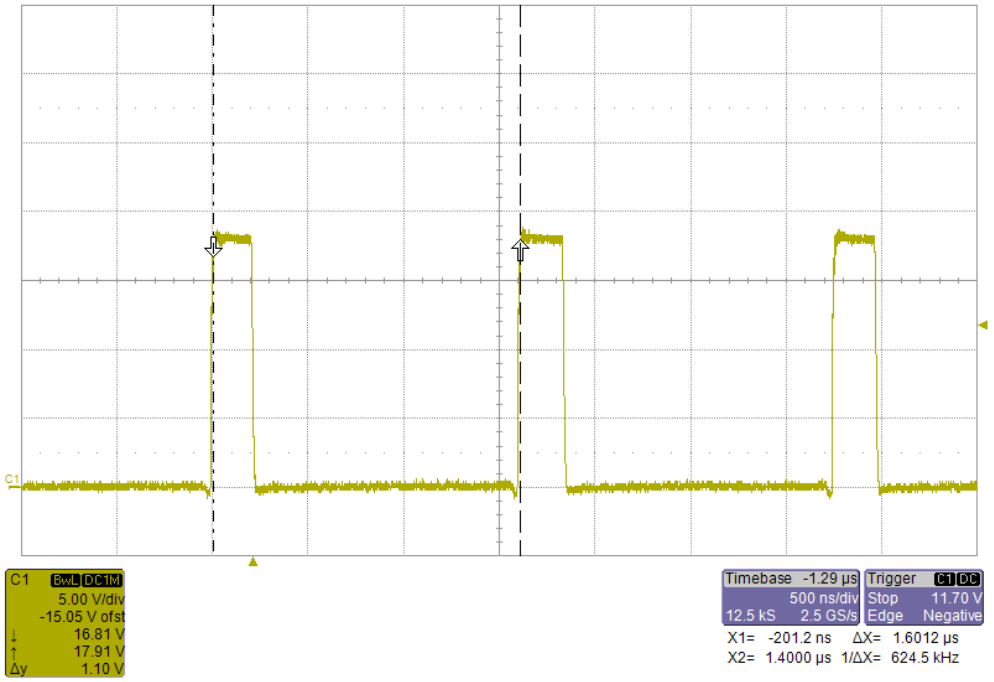
5.2 Start-up Waveform

V_{in} = 18V, V_{out} = 2.5V, I_{out} = 500mA

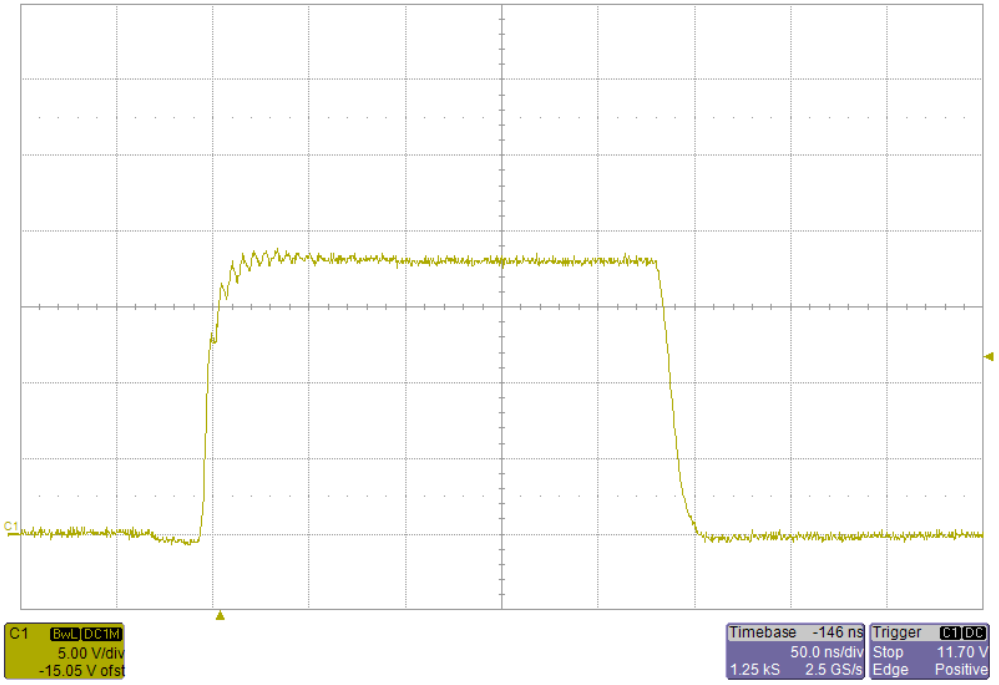


5.3 Switch Node

V_{in} = 18V, V_{out} = 2.5V, I_{out} = 3A

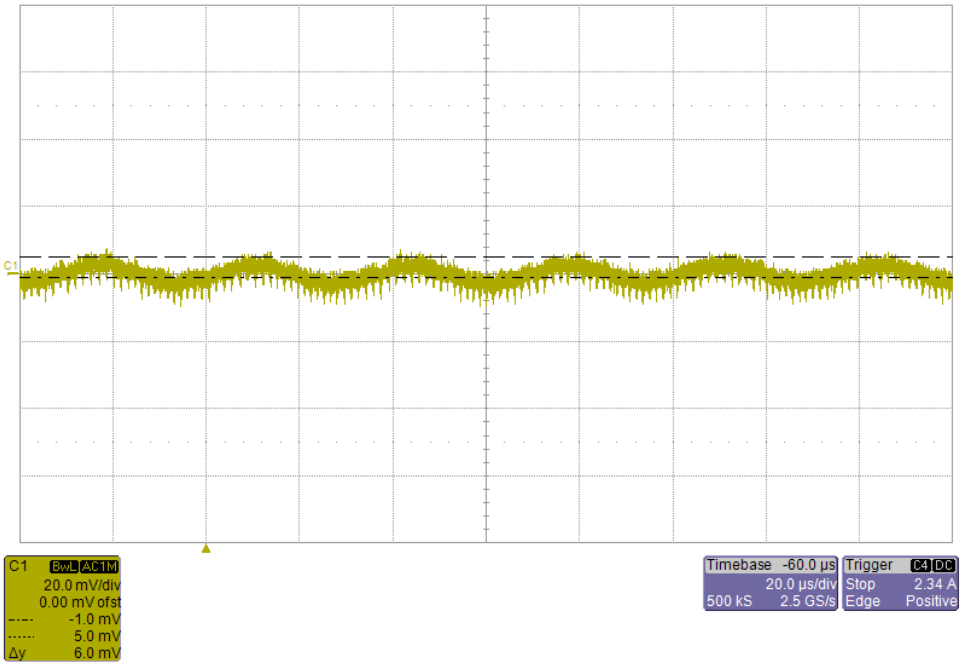


Zoom



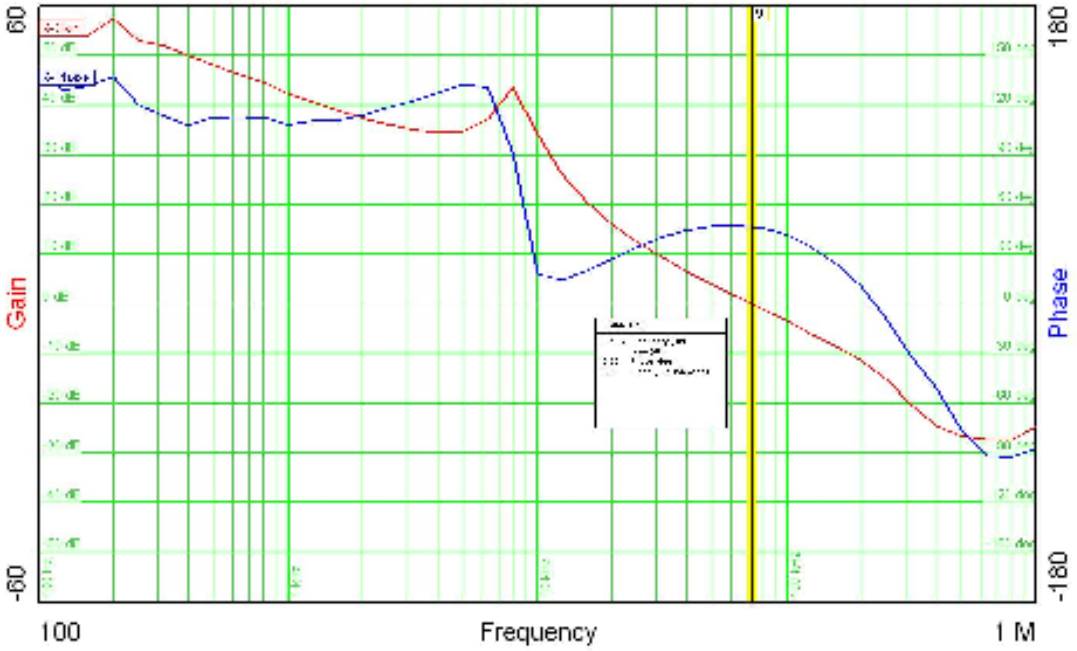
5.4 Output Voltage Ripple

V_{in} = 18V, V_{out} = 2.5V, I_{out} = 3A



5.5 Loop Response

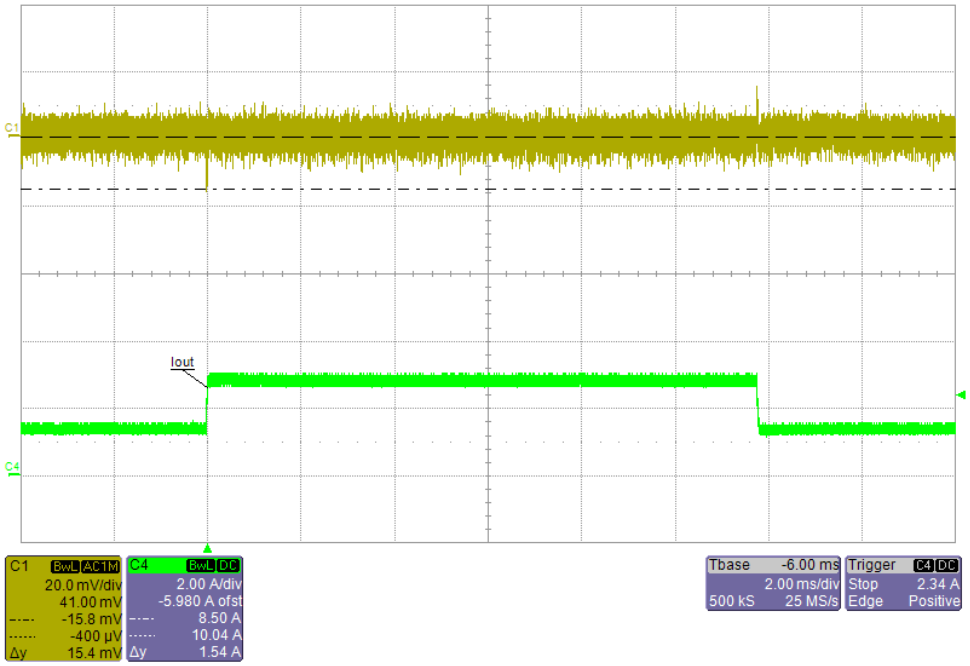
V_{in} = 18V, V_{out} = 2.5V, I_{out} = 3A



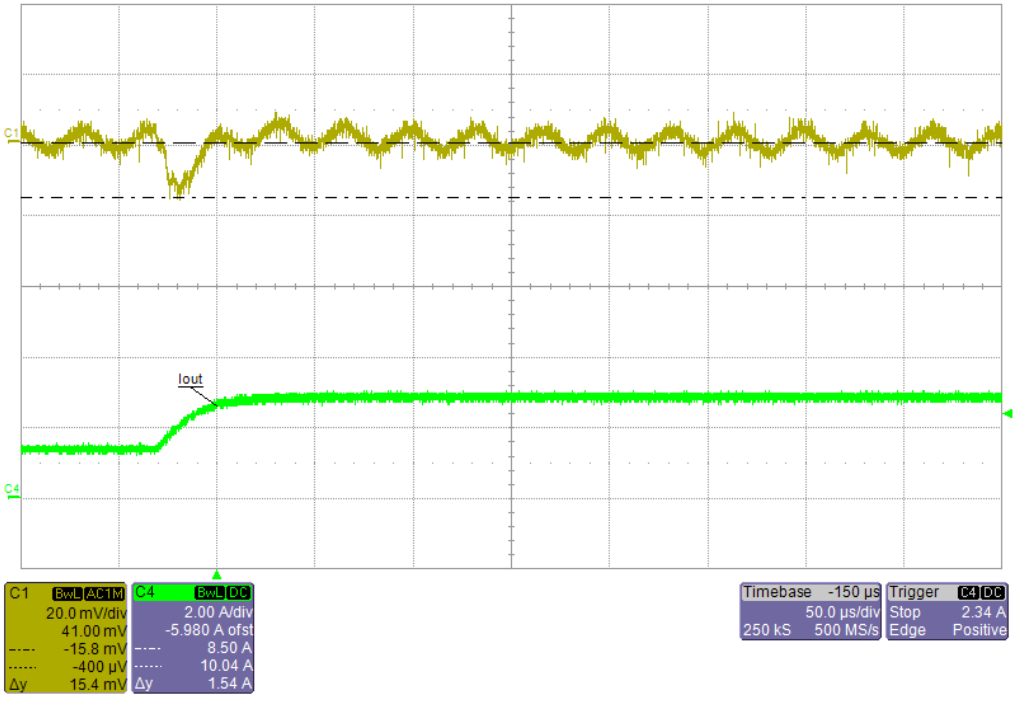
Phase Margin 46.56 @ 72.52 kHz

5.6 Load Transient

V_{in} = 18V, V_{out} = 2.5V, I_{out} = 1.5A to 3A

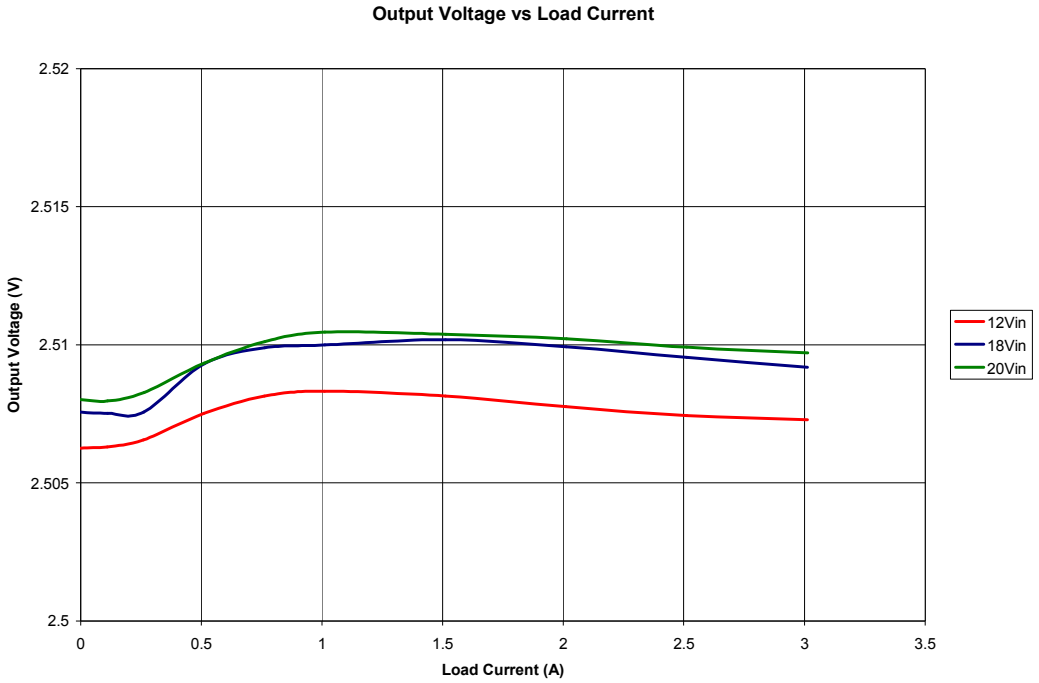


Zoom



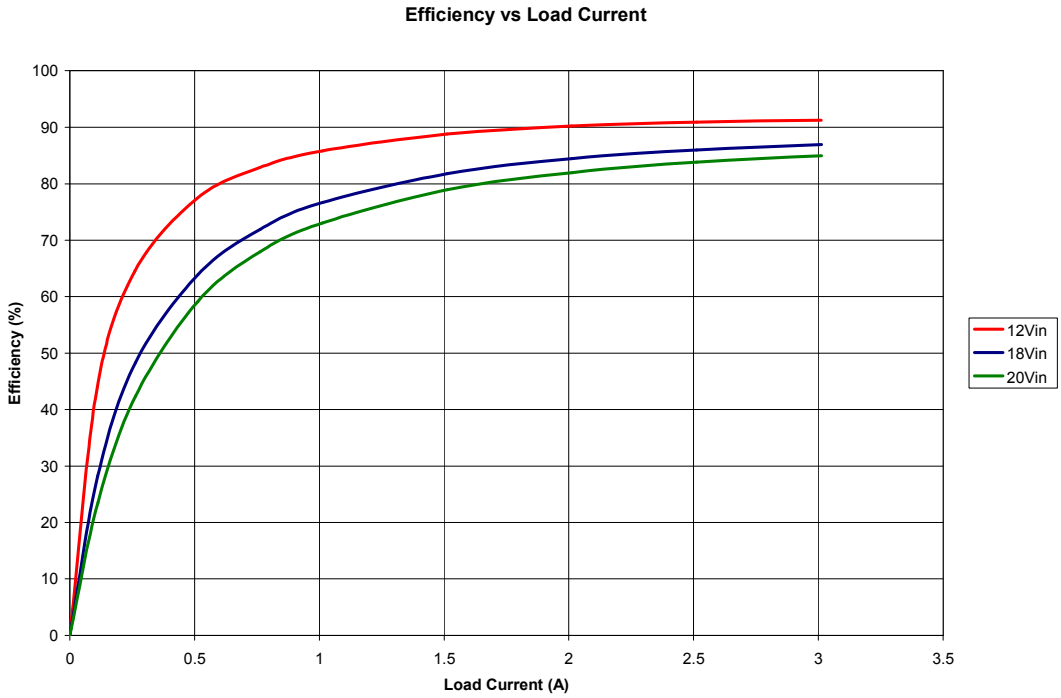
5.7 Load Regulation

V_{in} = 2.5V



5.8 Efficiency

V_{in} = 2.5V



6 TPS40303 – 0.9V @ 6A

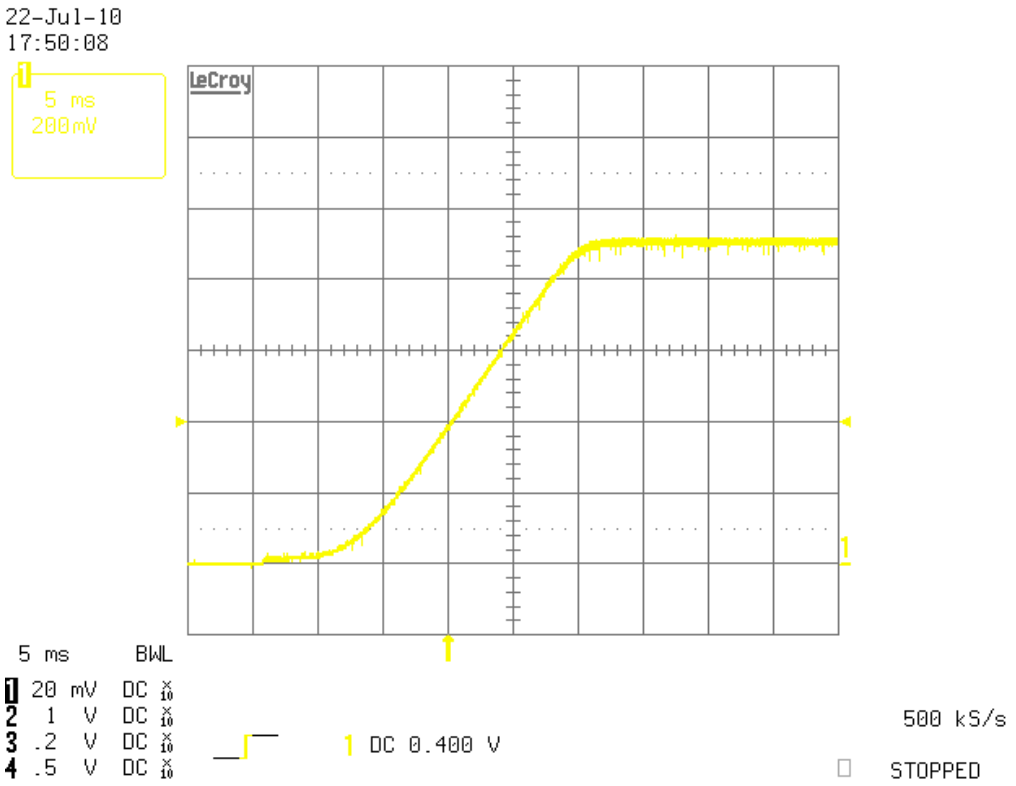
6.1 Performance Summary

Performance parameters below represent data obtained from the PMP5754 design; changes to the design, component selection or layout may result in varied performance.

Parameter	Test Conditions	Min	Typ	Max	Unit
Loop Bandwidth	V_{in}= 18V, I_{out}= 6A		62.73		kHz
Phase Margin	V_{in}= 18V, I_{out}= 6A		49.73		º
Output Voltage Ripple	I_{out}= 6A		9		mV
Maximum Efficiency			90.14		%
Load Regulation	V_{in} = 18V, I_{out}= 0A to 6A		0.3		%
Switching Frequency	I_{out}= 6A		306		kHz

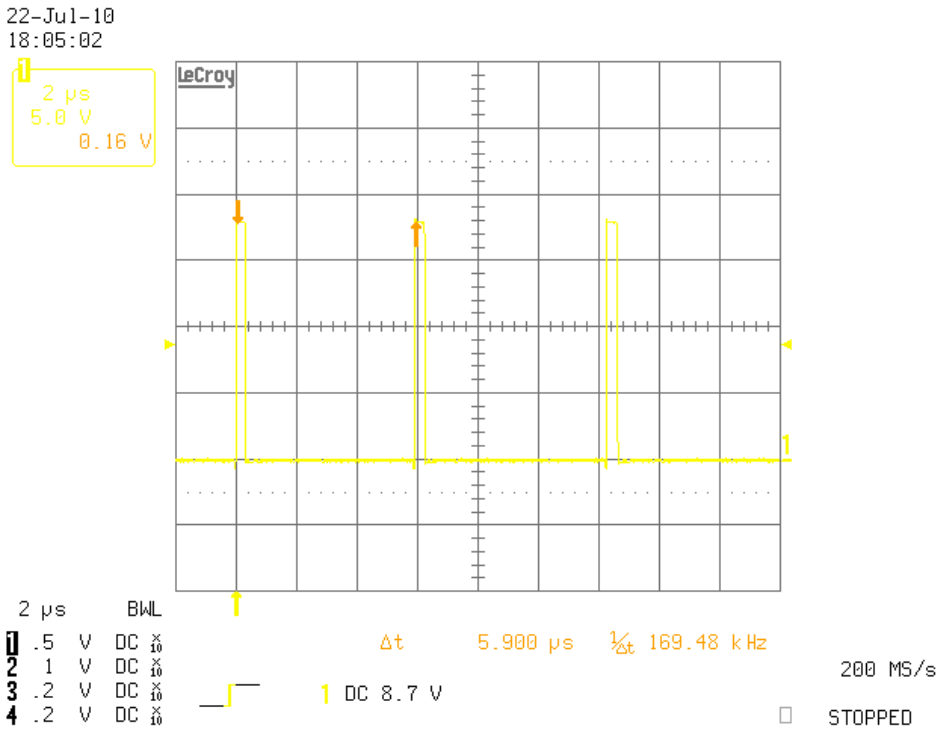
6.2 Start-up Waveform

V_{in} = 18V, V_{out} = 0.9V, I_{out} = 500mA

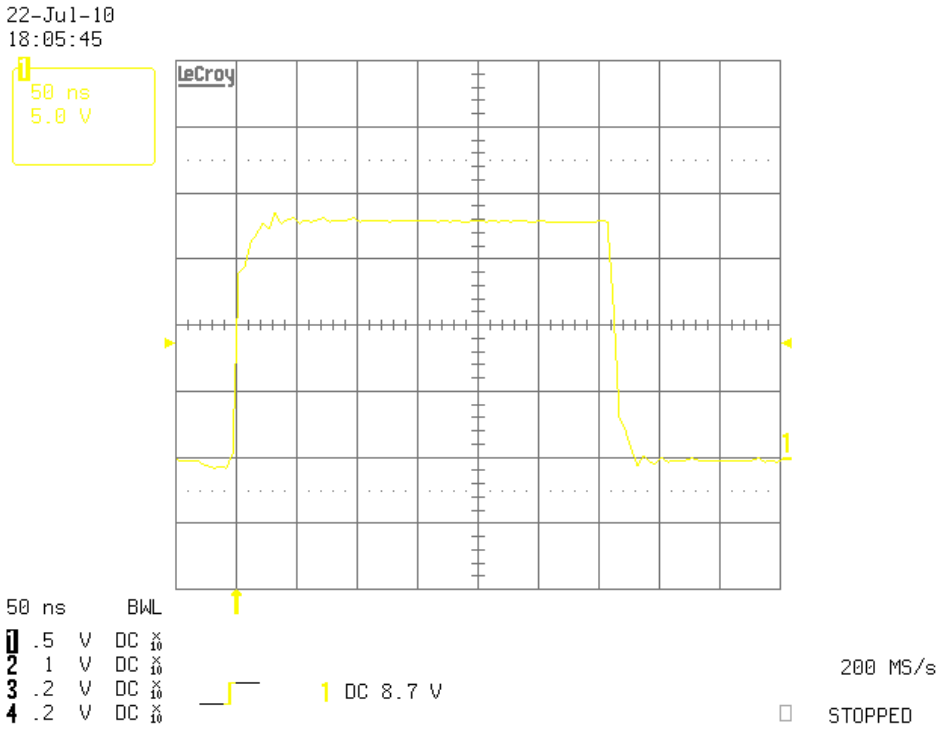


6.3 Switch Node

V_{in} = 18V, V_{out} = 0.9V, I_{out} = 6A

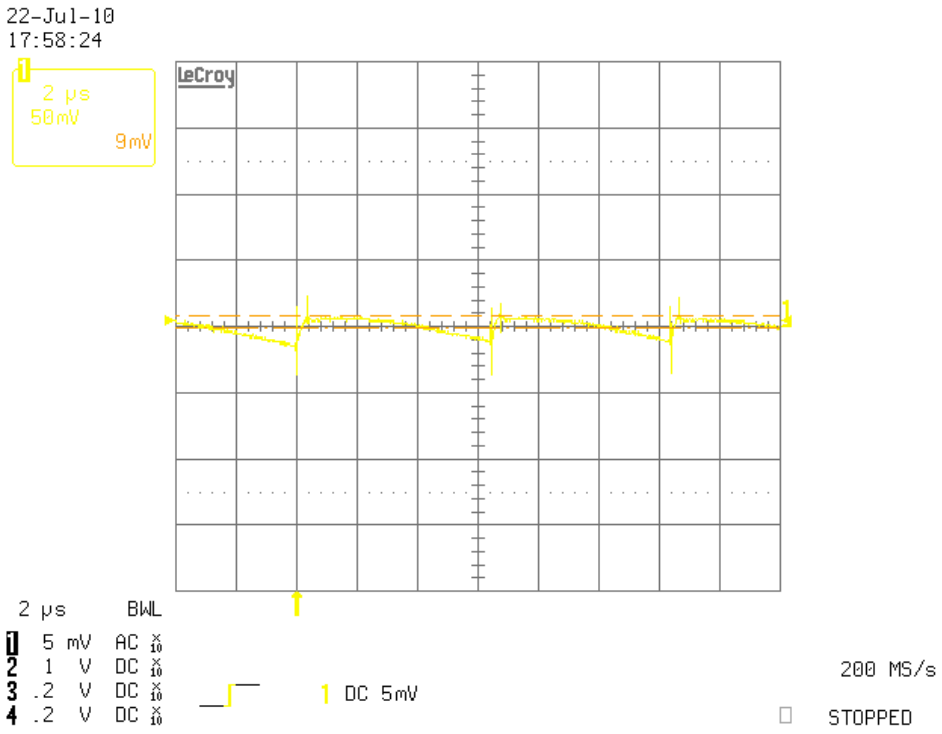


Zoom



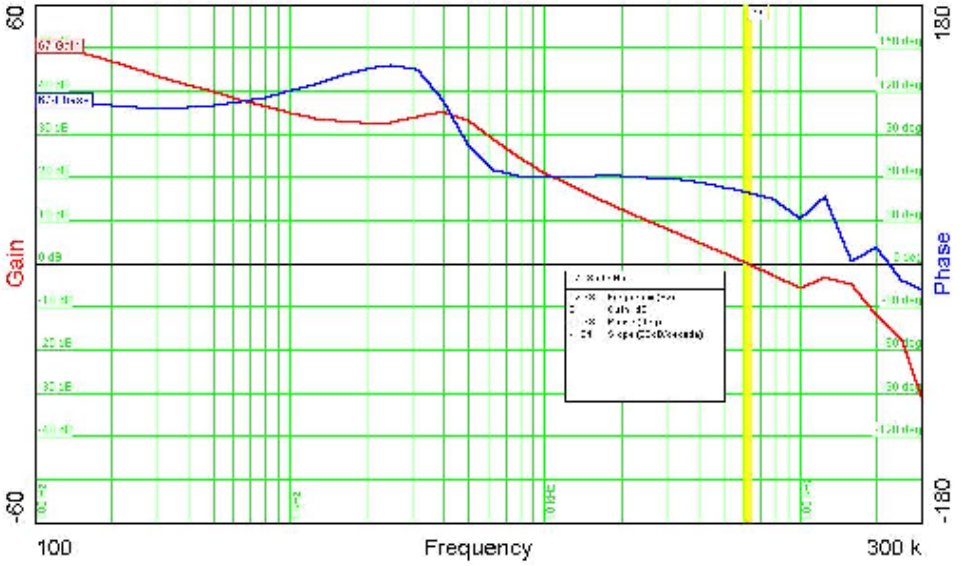
6.4 Output Voltage Ripple

V_{in} = 18V, V_{out} = 0.9V, I_{out} = 6A



6.5 Loop Response

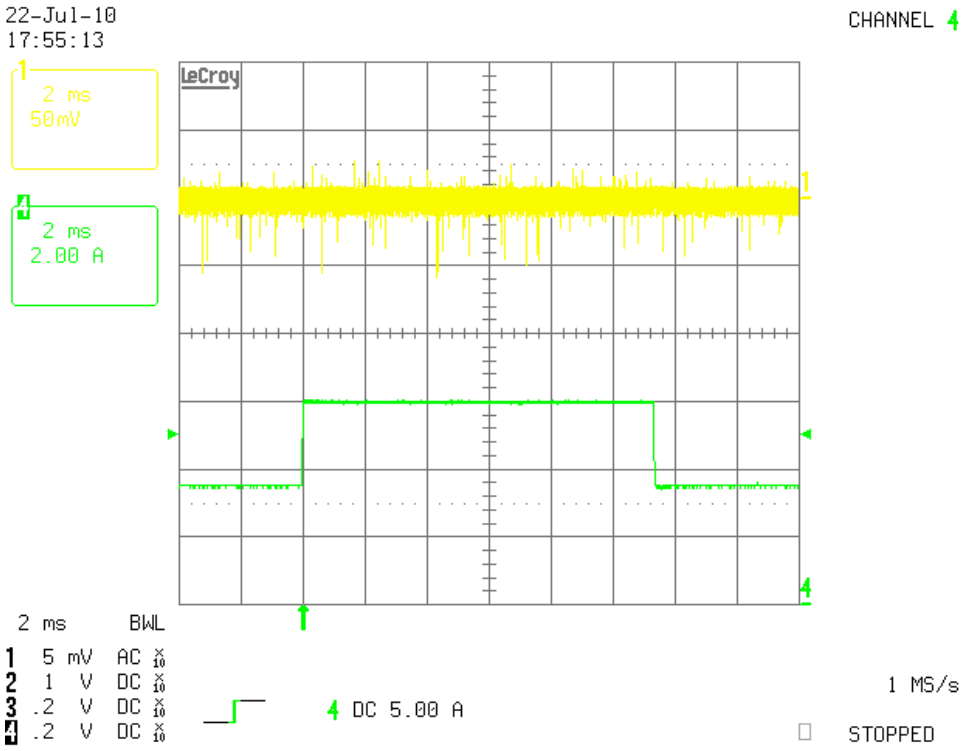
V_{in} = 18V, V_{out} = 0.9V, I_{out} = 6A



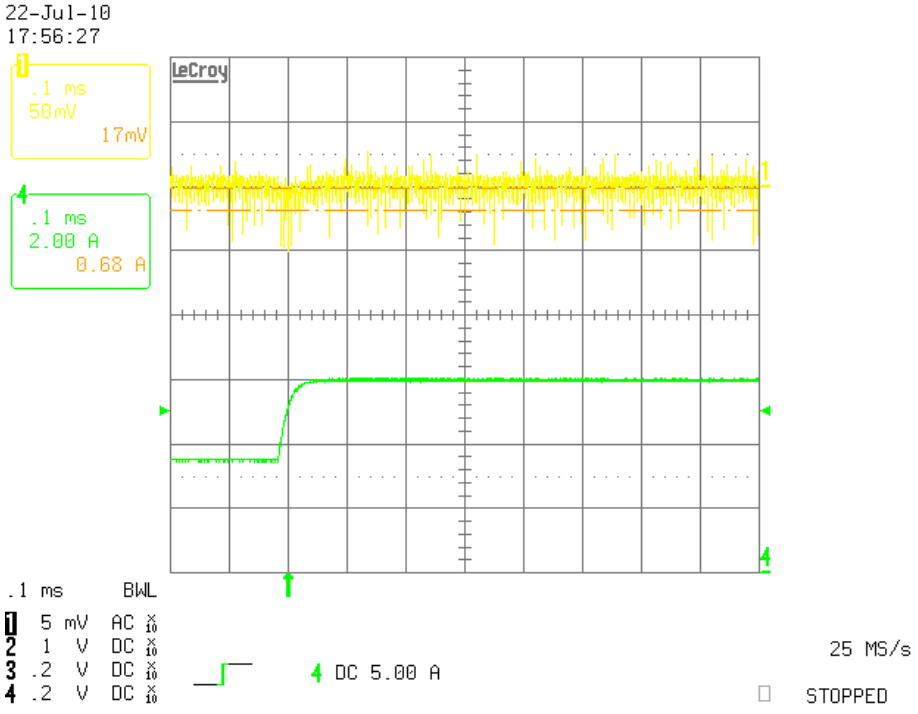
Phase Margin 49.73 @ 62.73 kHz

6.6 Load Transient

V_{in} = 18V, V_{out} = 0.9V, I_{out} = 3A to 6A

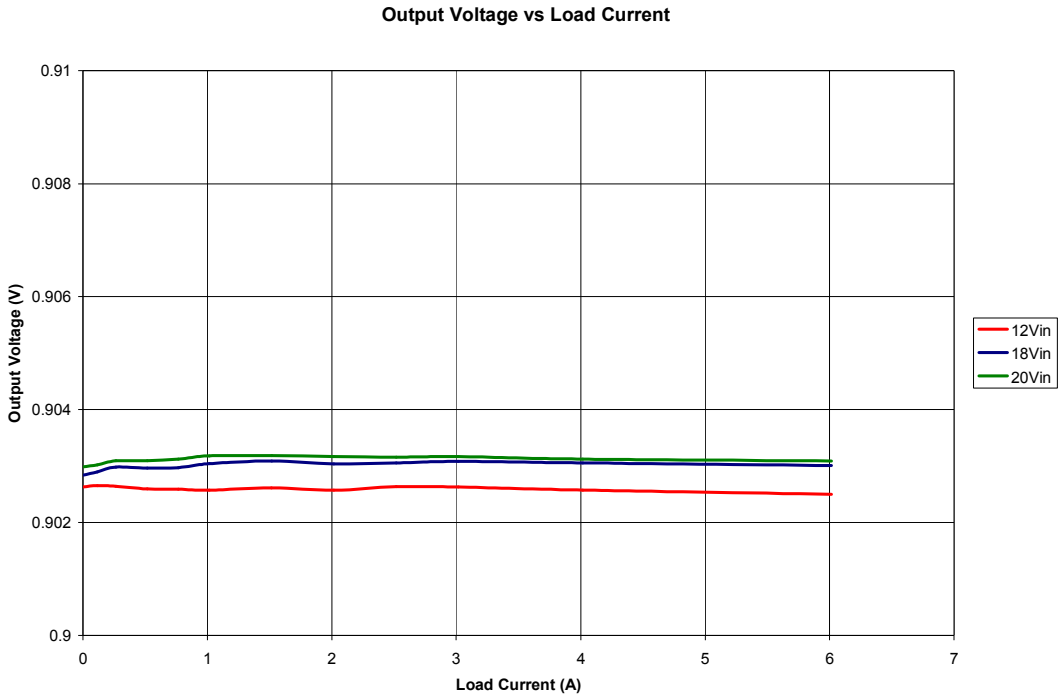


Zoom



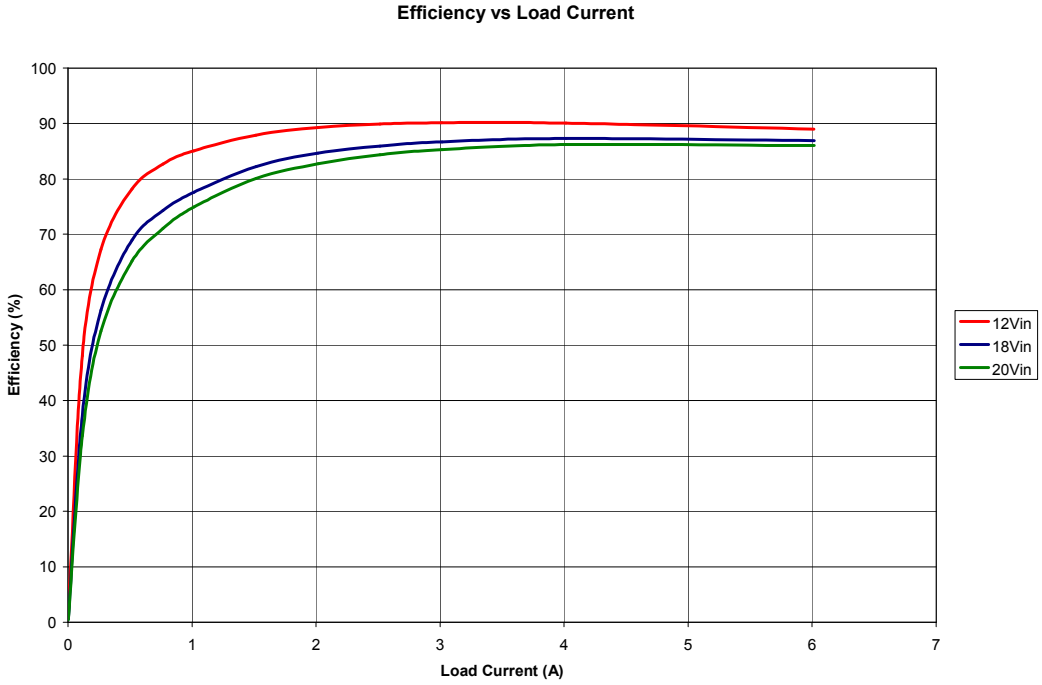
6.7 Load Regulation

V_{out} = 0.9V



6.8 Efficiency

V_{out} = 0.9V



7 TPS40304 – -4V @ 6A

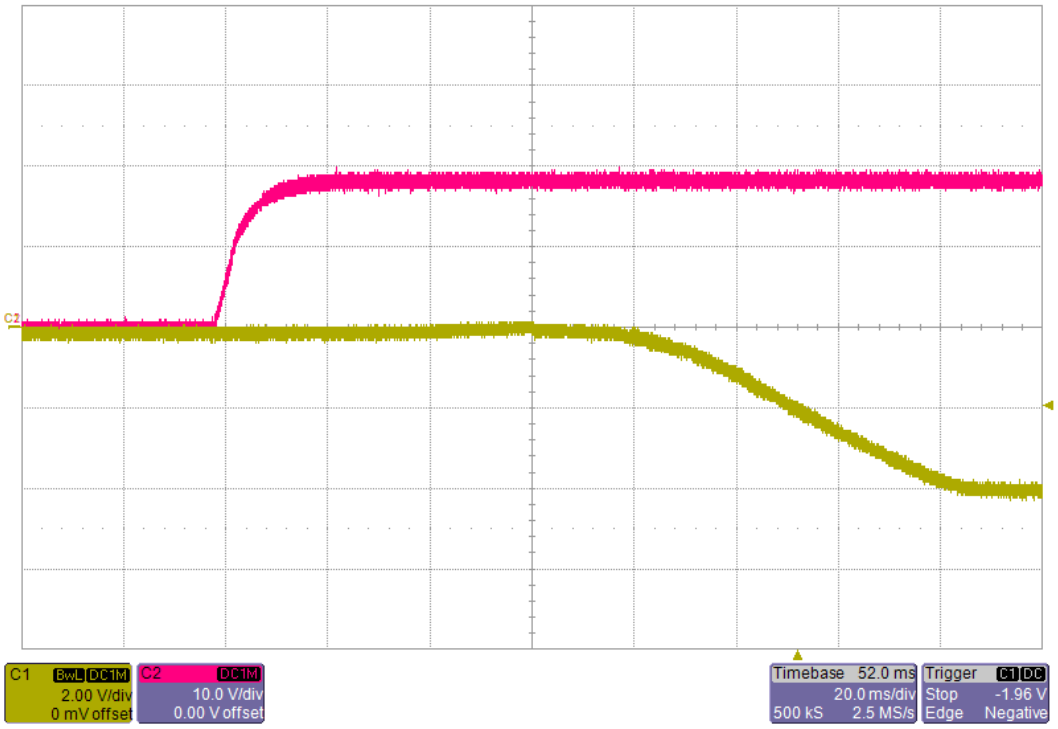
7.1 Performance Summary

Performance parameters below represent data obtained from the PMP5754 design; changes to the design, component selection or layout may result in varied performance.

Parameter	Test Conditions	Min	Typ	Max	Unit
Loop Bandwidth	V_{in}= 18V, I_{out}= 6A		9.545		kHz
Phase Margin	V_{in}= 18V, I_{out}= 6A		55.82		º
Output Voltage Ripple	I_{out}= 6A		40.8		mV
Maximum Efficiency			89.2		%
Load Regulation	V_{in} = 18V, I_{out}= 0A to 6A		2.1		%
Switching Frequency	I_{out}= 6A		623		kHz

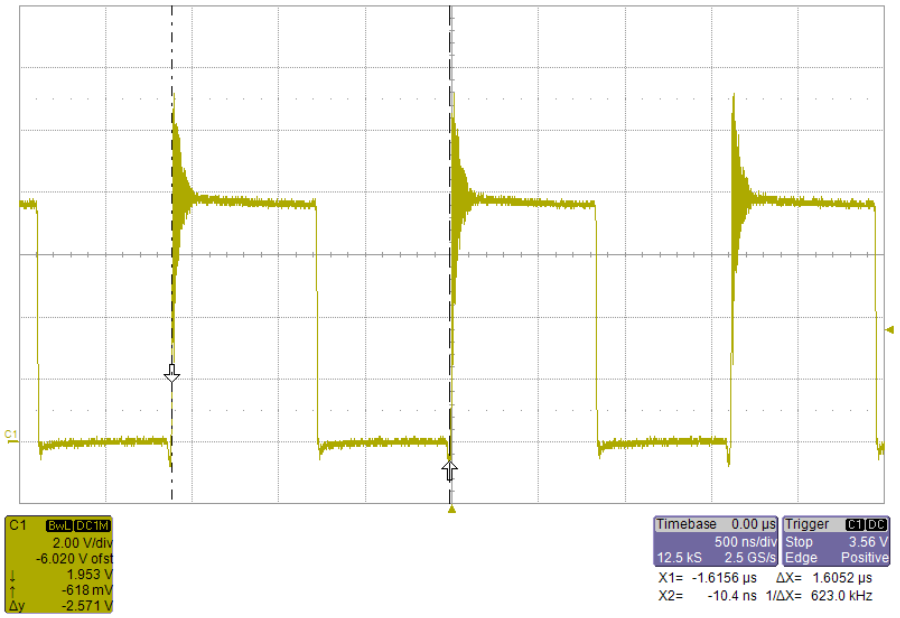
7.2 Start-up Waveform

V_{in} = 18V, V_{out} = -4V, I_{out} = 500mA

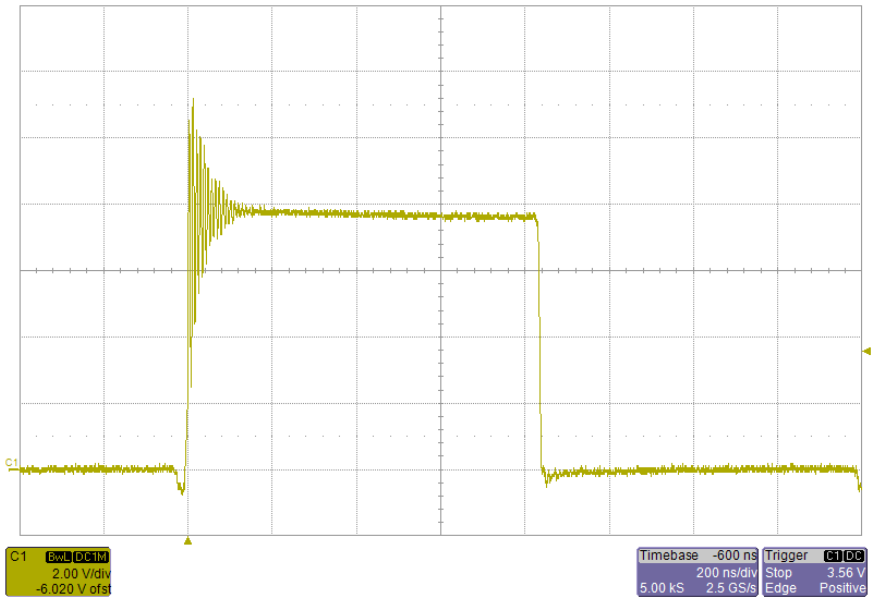


7.3 Switch Node

V_{in} = 18V, V_{out} = -4V, I_{out} = 6A

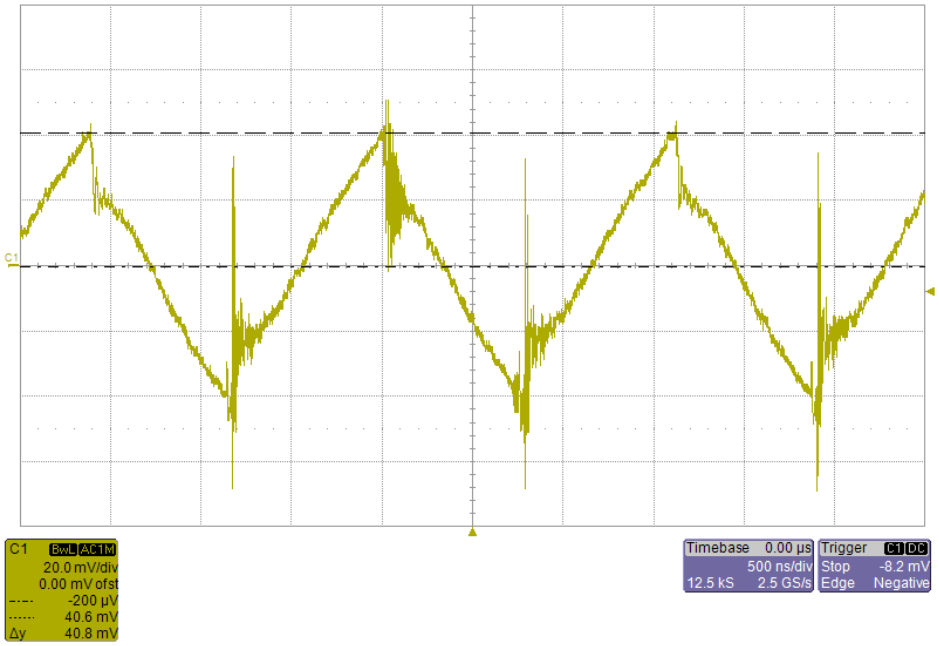


Zoom - V_{in} = 18V, V_{out} = -4V, I_{out} = 6A



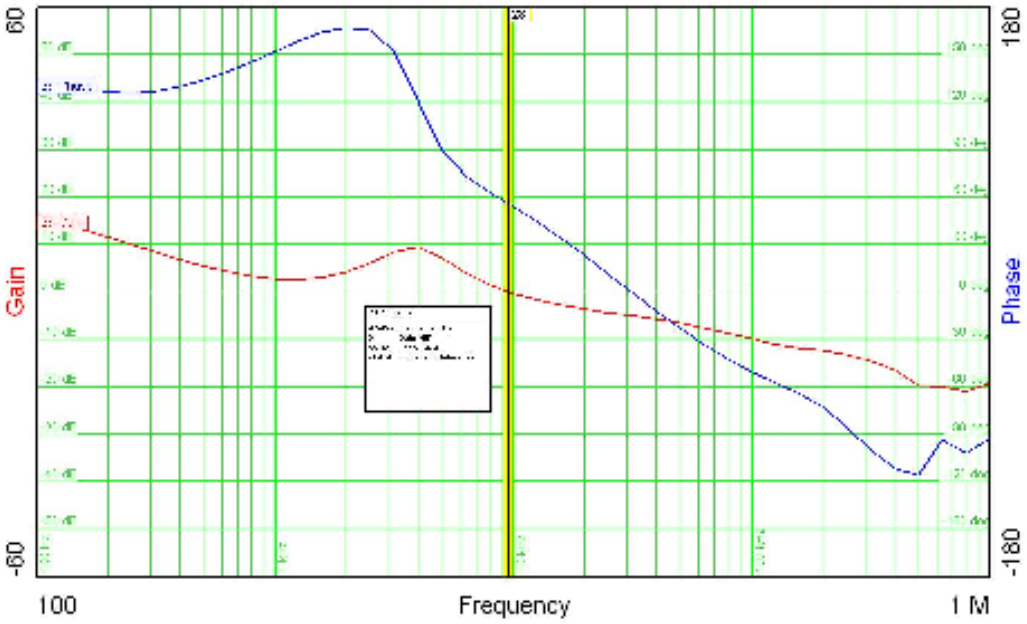
7.4 Output Voltage Ripple

V_{in} = 18V, V_{out} = -4V, I_{out} = 6A



7.5 Loop Response

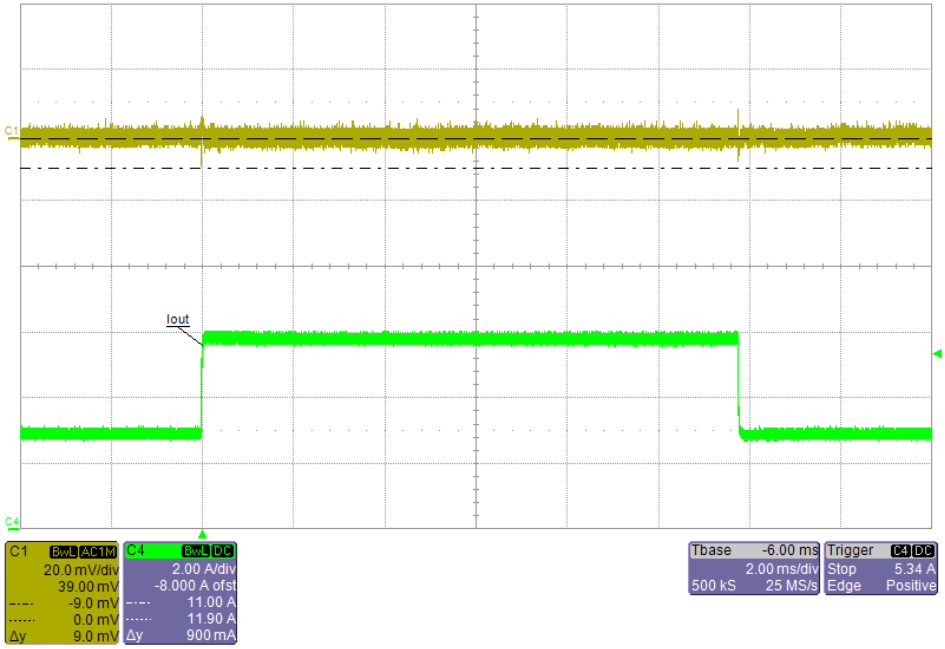
V_{in} = 18V, V_{out} = -4V, I_{out} = 6A



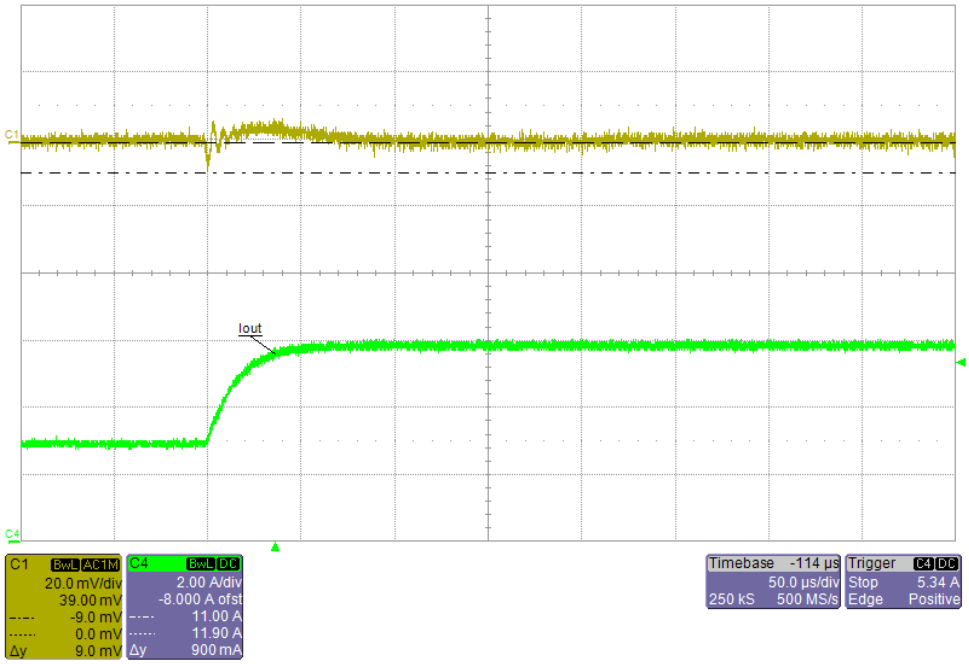
Phase Margin 55.82 @ 9.545 kHz

7.6 Load Transient

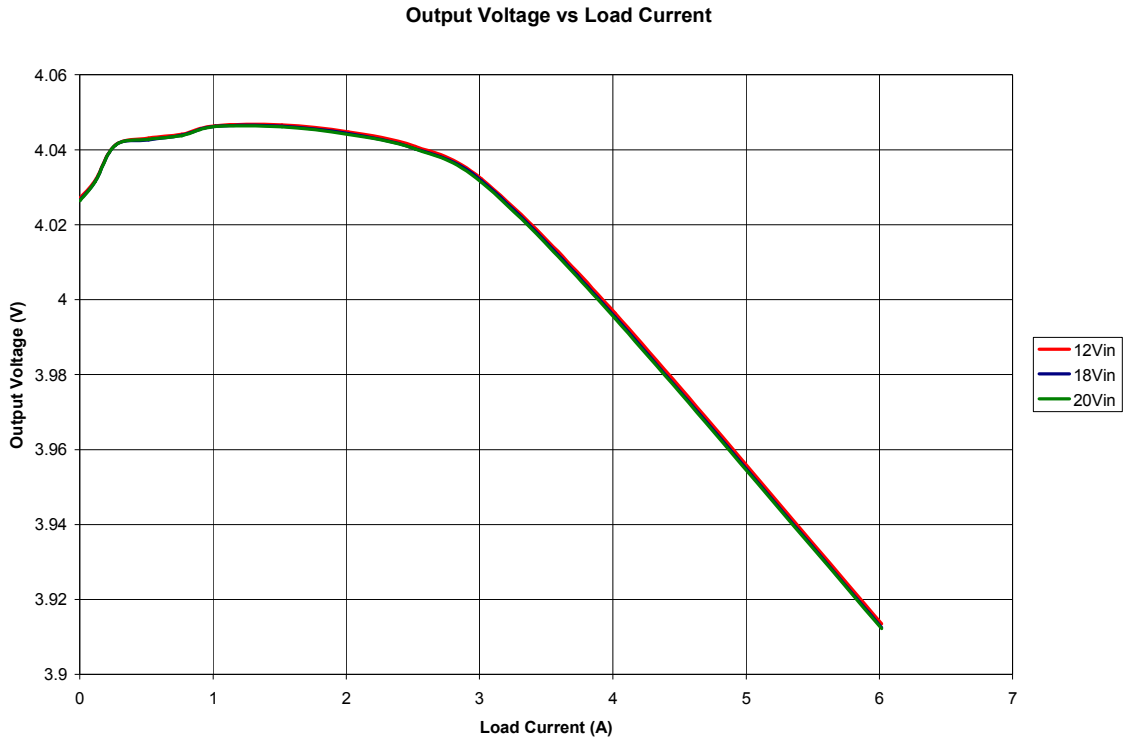
V_{in} = 18V, V_{out} = -4V, I_{out} = 3 to 6A



Zoom

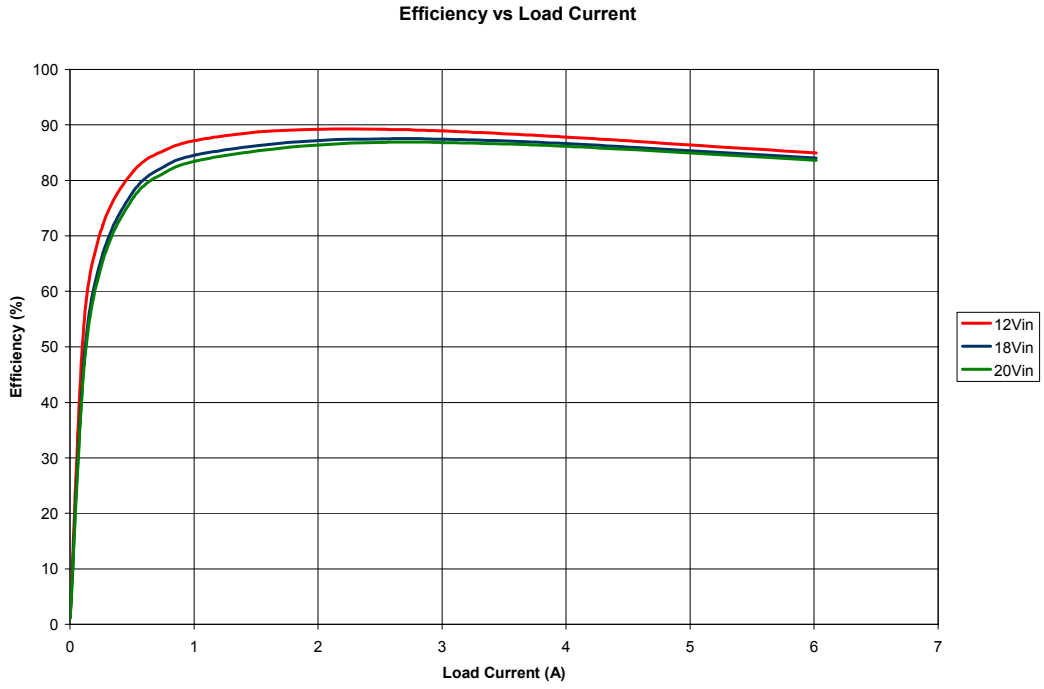


7.7 Load Regulation



7.8 Efficiency

V_{out} = -4V



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