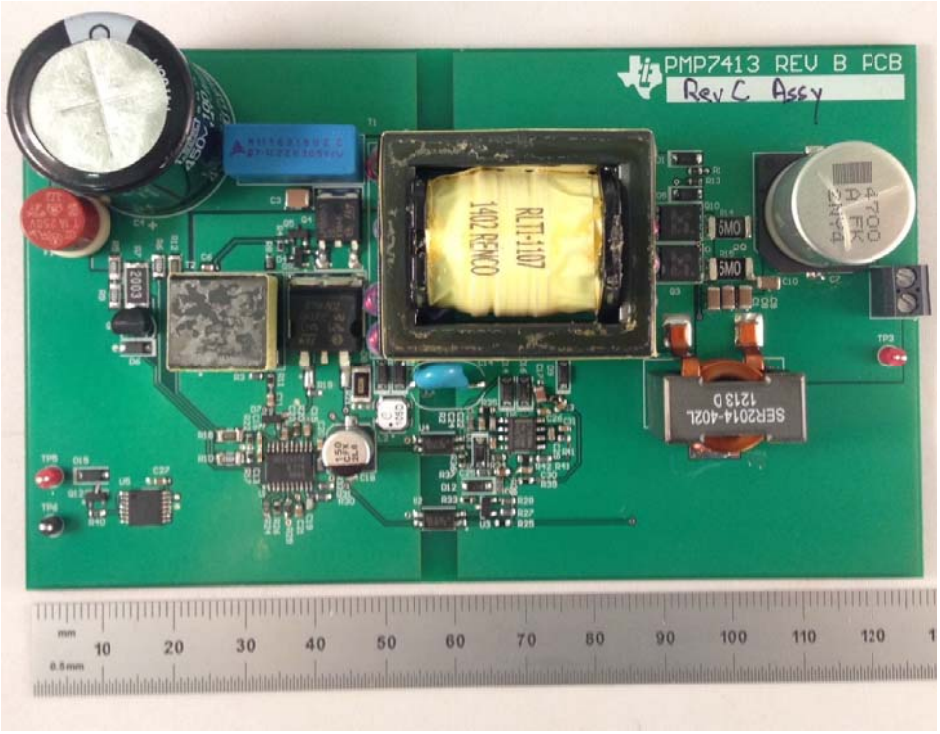
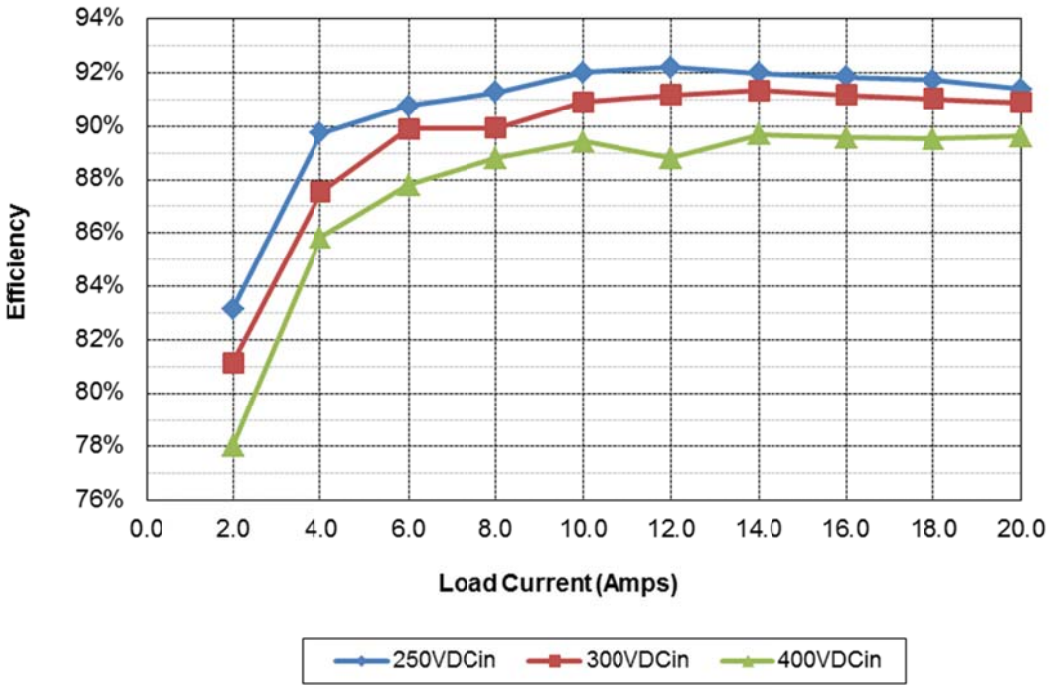
1 Photo

The photograph below shows the PMP7413 Rev C demo board. This circuit was build using a PMP7413 Rev B PCB.



2 Efficiency



PMP7413 Rev B Test Results

250VDCin

Iout	Vout	Vin	Iin	Pin	Pout	Losses	Efficiency
0.00	4.99	250.0	0.007	1.75	0.00	1.75	0.0%
2.00	4.99	250.0	0.048	12.00	9.98	2.02	83.2%
4.00	4.99	249.9	0.089	22.24	19.96	2.28	89.7%
6.00	4.99	249.9	0.132	32.99	29.94	3.05	90.8%
8.00	4.99	249.9	0.175	43.73	39.92	3.81	91.3%
10.00	4.99	249.9	0.217	54.23	49.90	4.33	92.0%
12.00	4.99	249.8	0.260	64.95	59.88	5.07	92.2%
14.0	4.99	249.8	0.304	75.94	69.86	6.08	92.0%
16.0	4.99	249.8	0.348	86.93	79.84	7.09	91.8%
18.0	4.99	249.8	0.392	97.92	89.82	8.10	91.7%
20.0	5.00	249.8	0.438	109.41	100.00	9.41	91.4%

300VDCin

Iout	Vout	Vin	Iin	Pin	Pout	Losses	Efficiency
0.00	4.99	300.0	0.007	2.10	0.00	2.10	0.0%
2.00	4.99	300.0	0.041	12.30	9.98	2.32	81.1%
4.00	4.99	300.0	0.076	22.80	19.96	2.84	87.5%
6.00	4.99	300.0	0.111	33.30	29.94	3.36	89.9%
8.00	4.99	299.9	0.148	44.39	39.92	4.47	89.9%
10.00	4.99	299.9	0.183	54.88	49.90	4.98	90.9%
12.00	4.99	299.9	0.219	65.68	59.88	5.80	91.2%
14.0	4.99	299.9	0.255	76.47	69.86	6.61	91.4%
16.0	4.99	299.9	0.292	87.57	79.84	7.73	91.2%
18.0	4.99	299.9	0.329	98.67	89.82	8.85	91.0%
20.0	5.00	299.8	0.367	110.03	100.00	10.03	90.9%

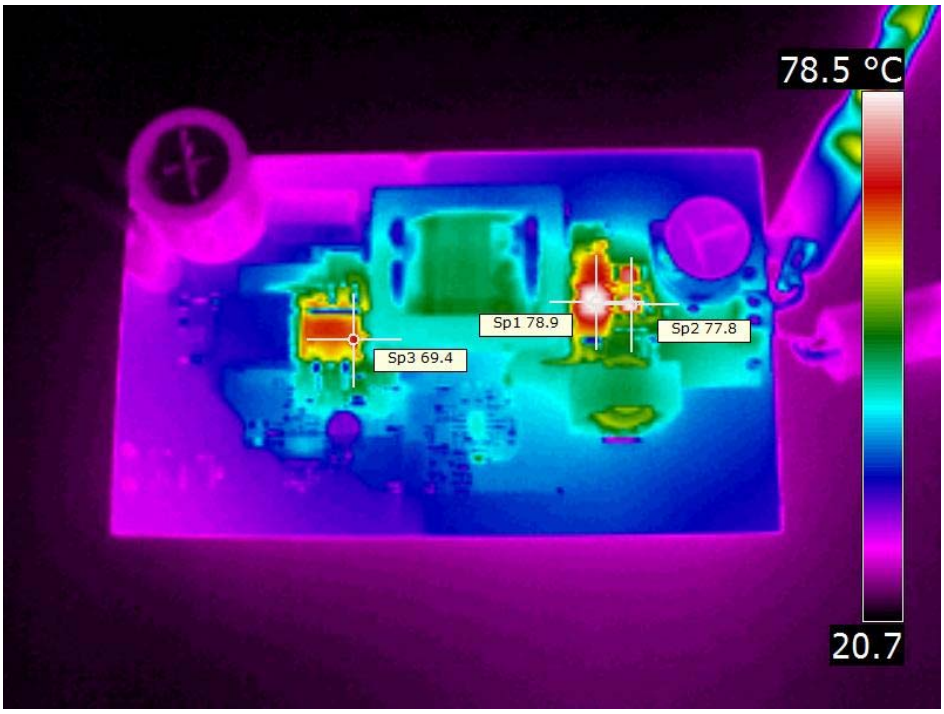
400VDCin

Iout	Vout	Vin	Iin	Pin	Pout	Losses	Efficiency
0.00	4.99	387.6	0.007	2.71	0.00	2.71	0.0%
2.00	4.99	387.6	0.033	12.79	9.98	2.81	78.0%
4.00	4.99	387.5	0.060	23.25	19.96	3.29	85.8%
6.00	4.99	387.5	0.088	34.10	29.94	4.16	87.8%
8.00	4.99	387.5	0.116	44.95	39.92	5.03	88.8%
10.00	4.99	387.5	0.144	55.80	49.90	5.90	89.4%
12.00	4.99	387.5	0.174	67.43	59.88	7.54	88.8%
14.0	4.99	387.5	0.201	77.89	69.86	8.03	89.7%
16.0	4.99	387.5	0.230	89.13	79.84	9.29	89.6%
18.0	4.99	387.4	0.259	100.34	89.82	10.52	89.5%
20.0	5.00	387.4	0.288	111.57	100.00	11.57	89.6%

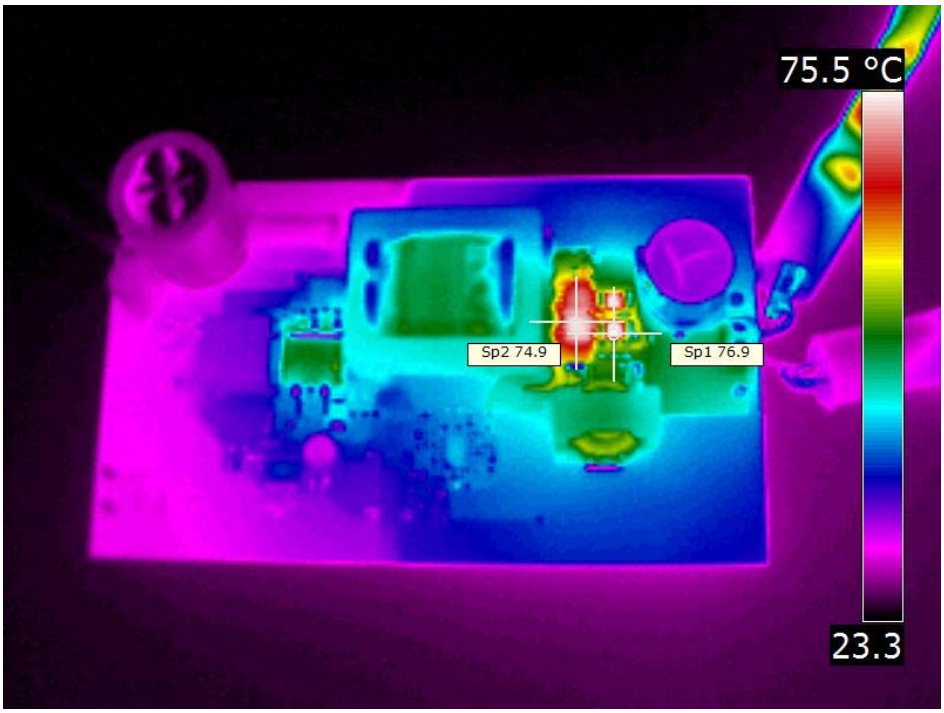
3 Thermal Images

The ambient temperature was 25C with 200LFM of forced air flow. The output was loaded with 20A.

3.1 400VDC Input

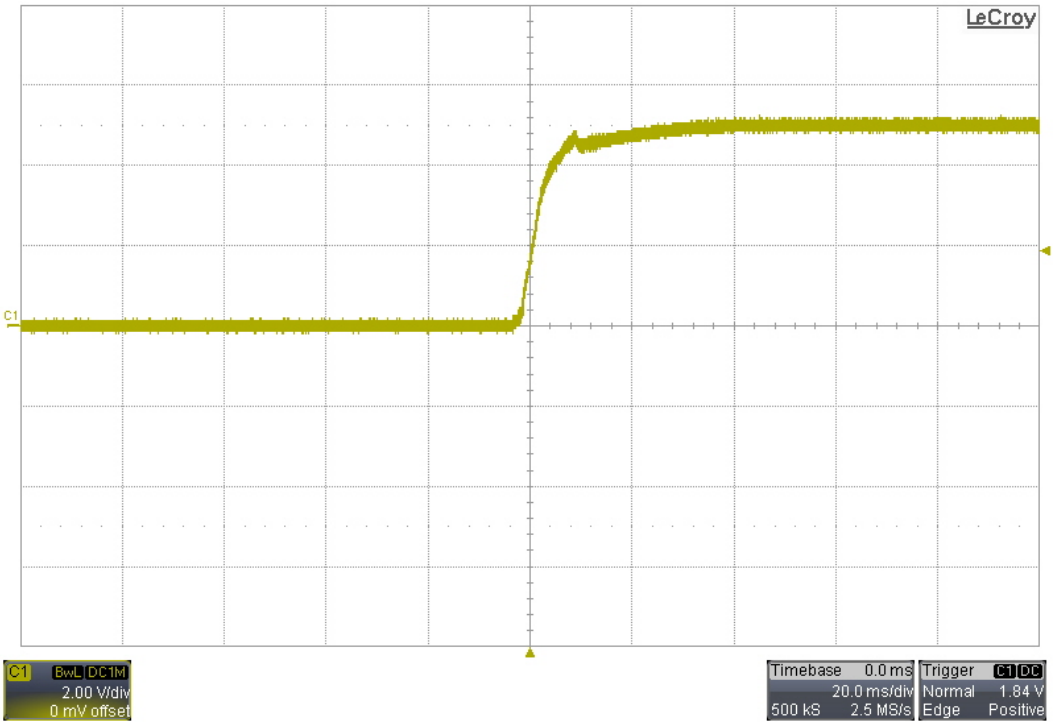


3.2 250VDC Input

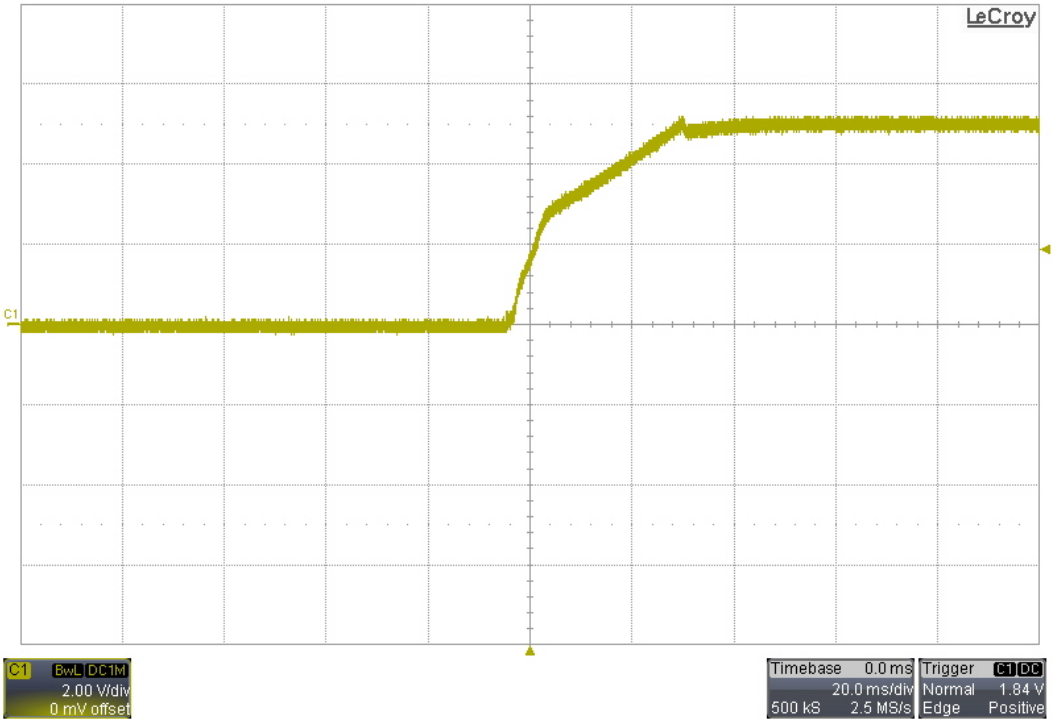


4 Startup

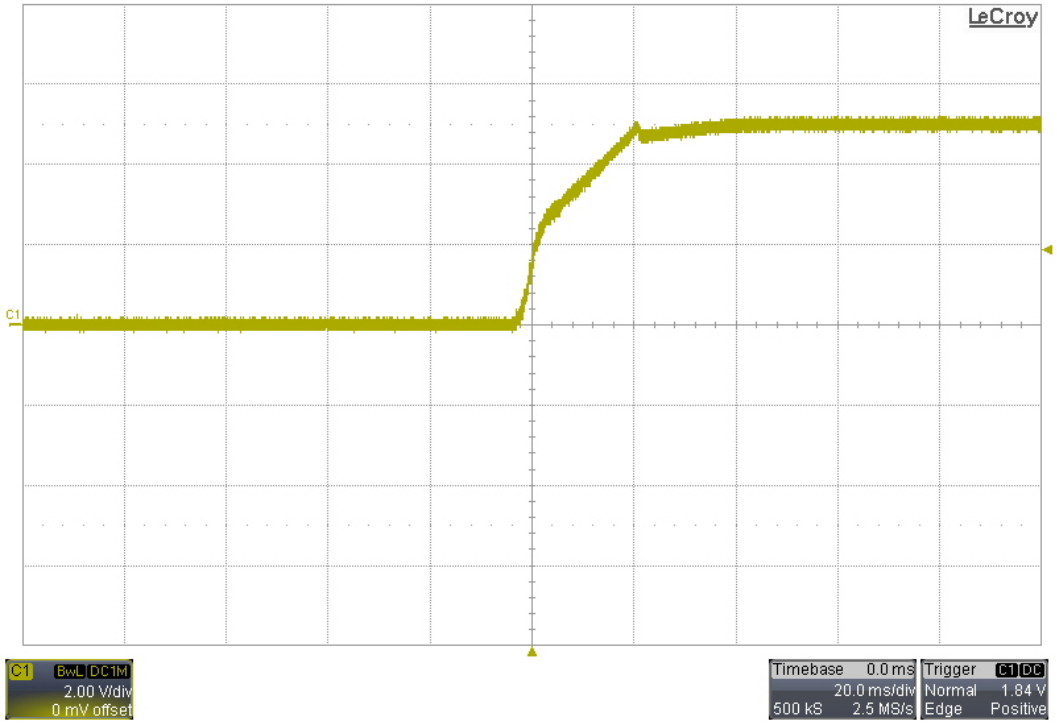
4.1 400VDC Input Startup, No Load



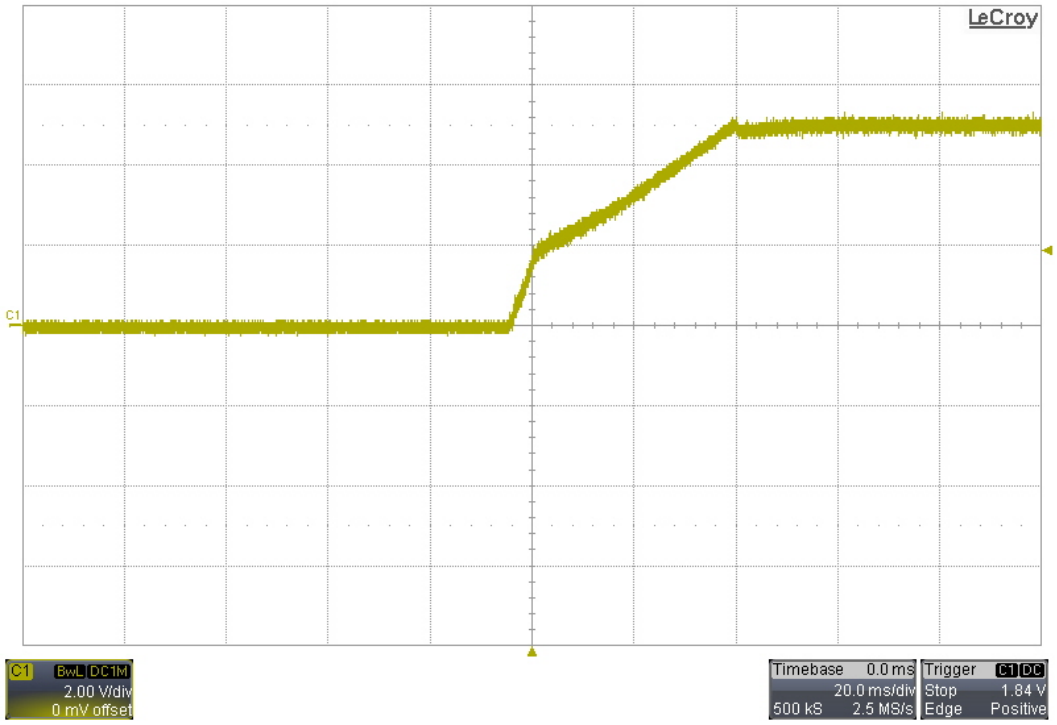
4.2 400VDC Input Startup, 0.5Ω Load



4.3 250VDC Input Startup, No Load

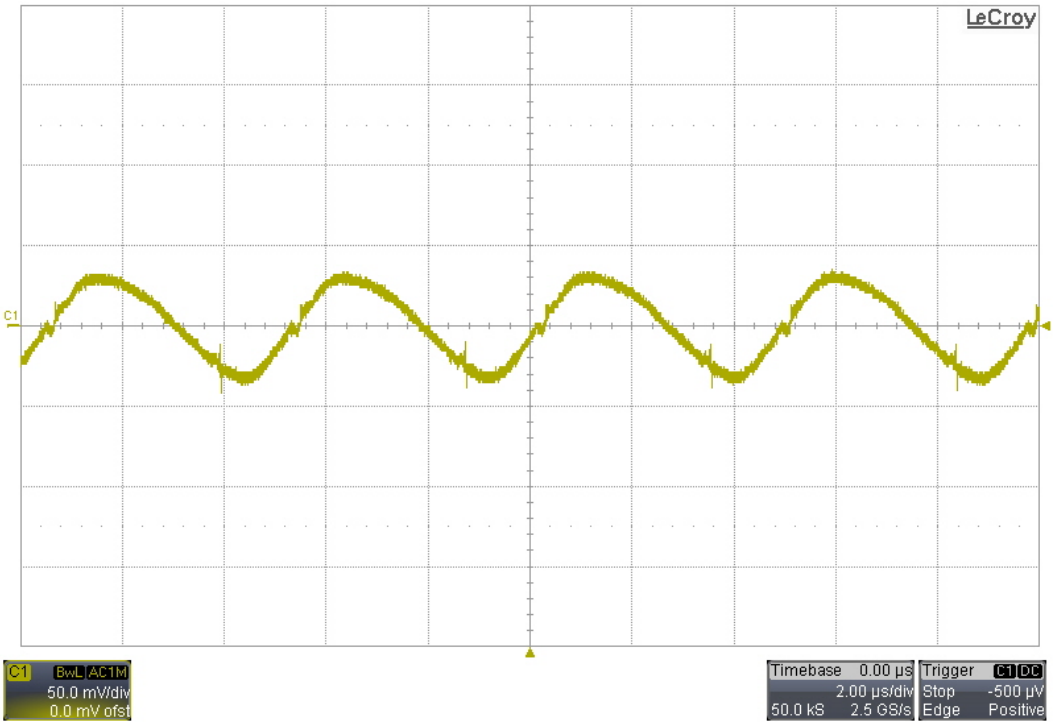


4.4 250VDC Input Startup, 0.5Ω Load

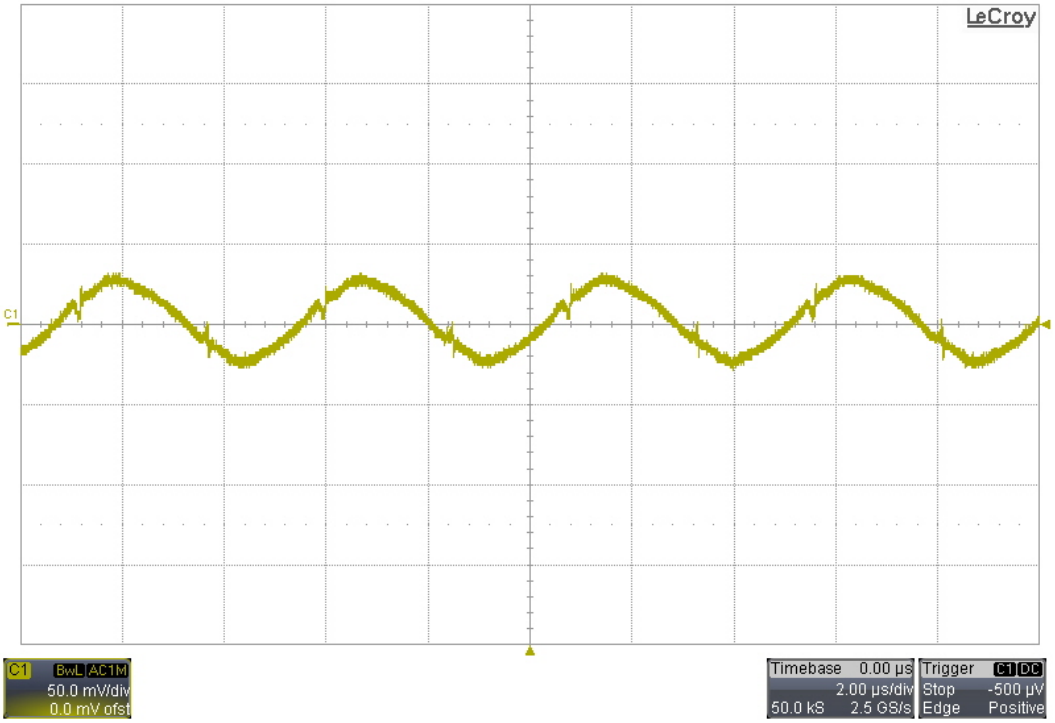


5 Output Ripple Voltage

5.1 400VDC Input, 20A Ripple Voltage

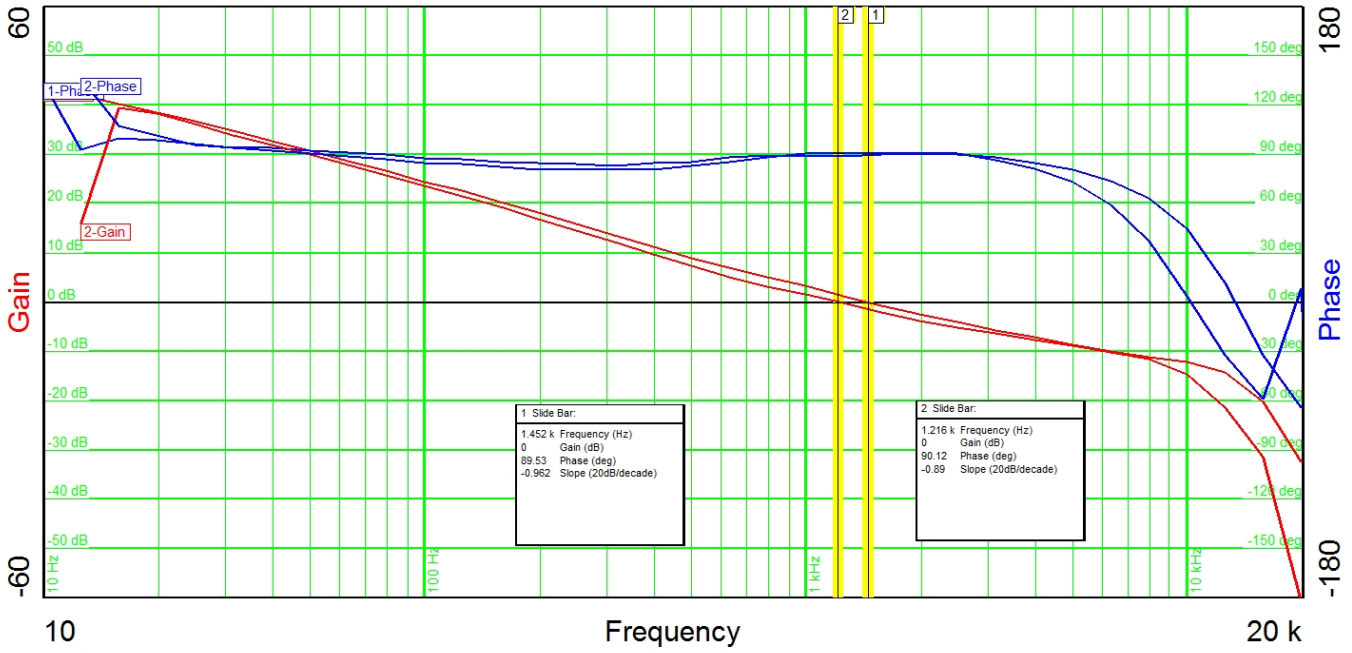


5.2 250VDC Input, 20A Ripple Voltage



6 Voltage Loop Response

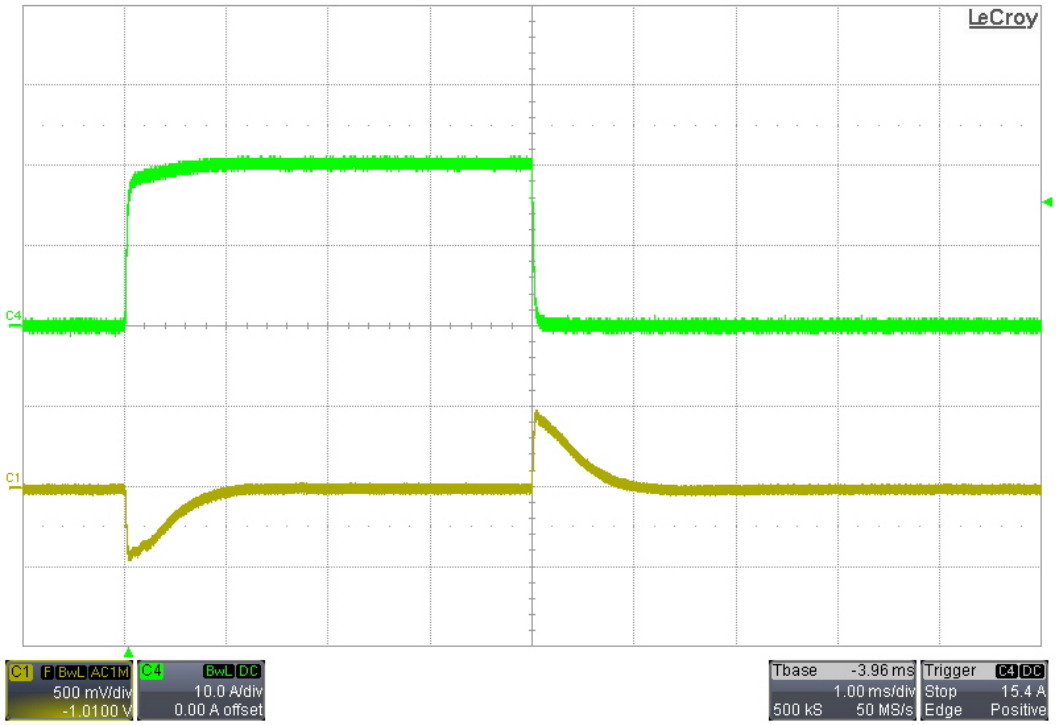
The frequency response of the voltage feedback loop is shown in the image below. The output was loaded with 20A. For gain/phase plot #1, the input was 400VDC and for gain/phase plot #2, the input was 250VDC.



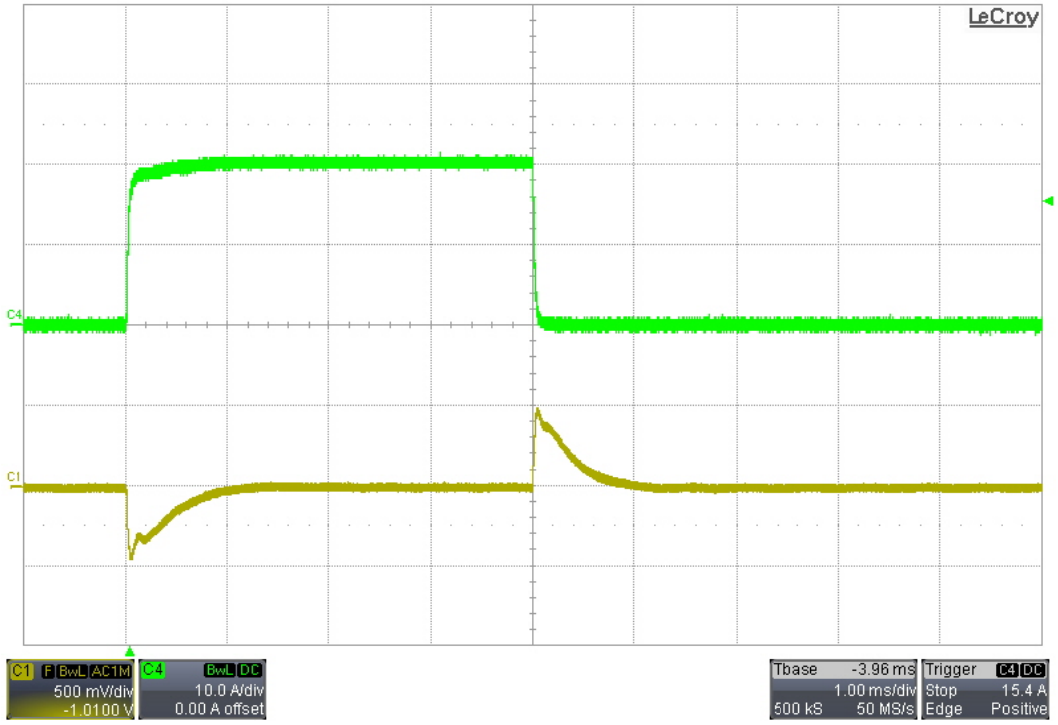
7 Load Transients

The response to a load step from 0A to 20A is shown in the images below. Channel 1: Vout (ac coupled); Channel 4: Iout

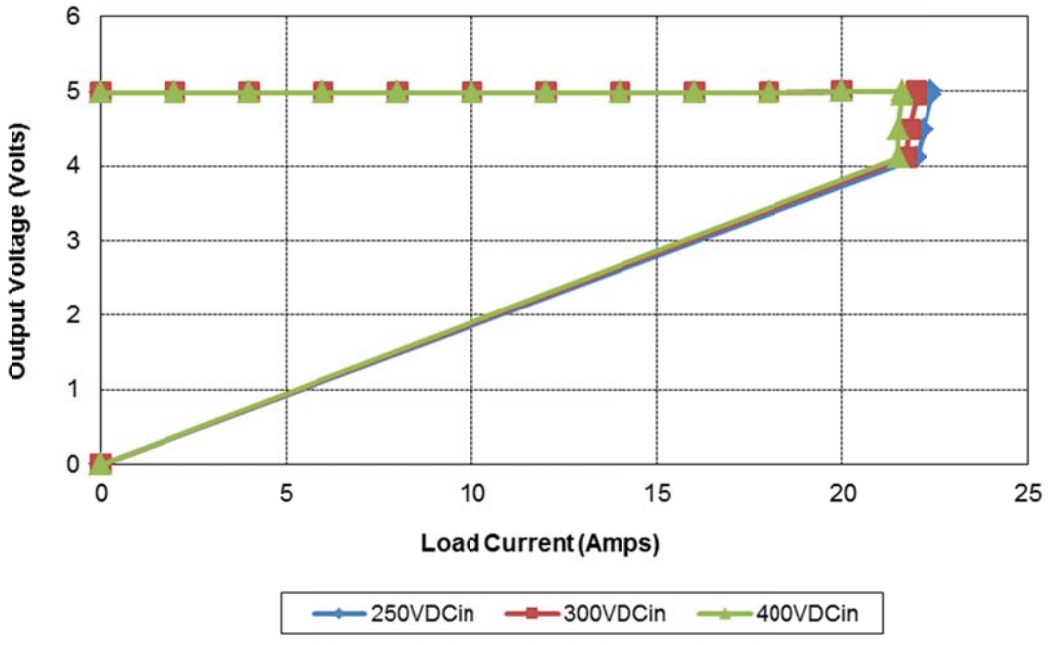
7.1 400VDC Input



7.2 250VDC Input

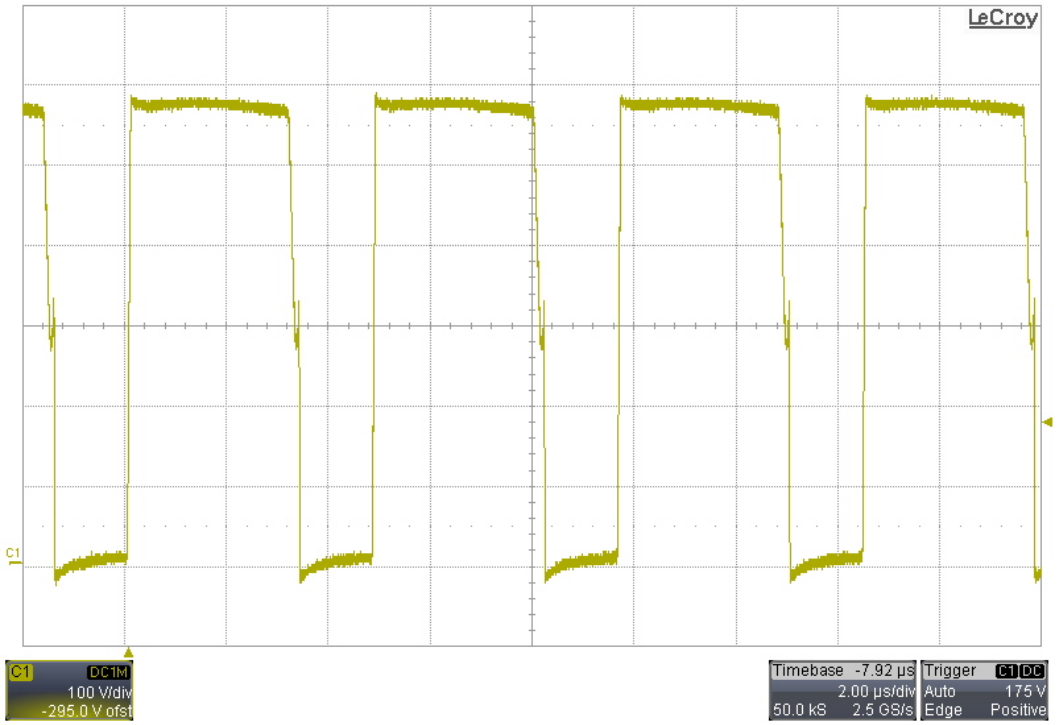


8 Overload V-I Characteristics

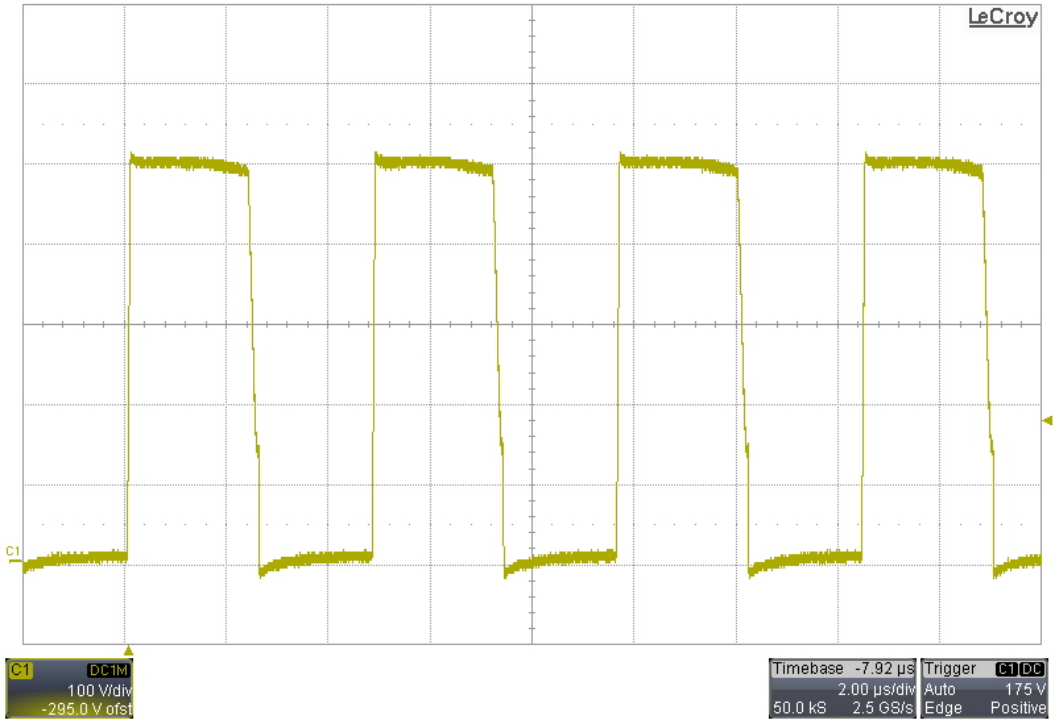


9 Primary Drain Waveforms

9.1 Primary FET (Q9) Vds – 400VDC Input, 20A Load

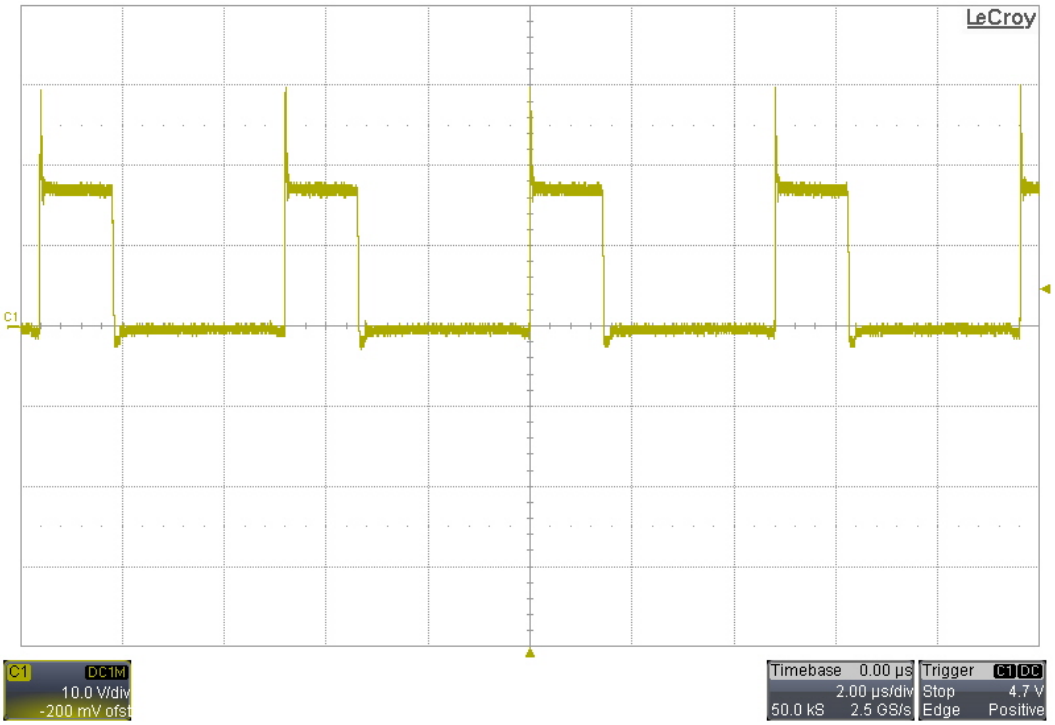


9.2 Primary FET (Q9) Vds – 250VDC Input, 20A Load

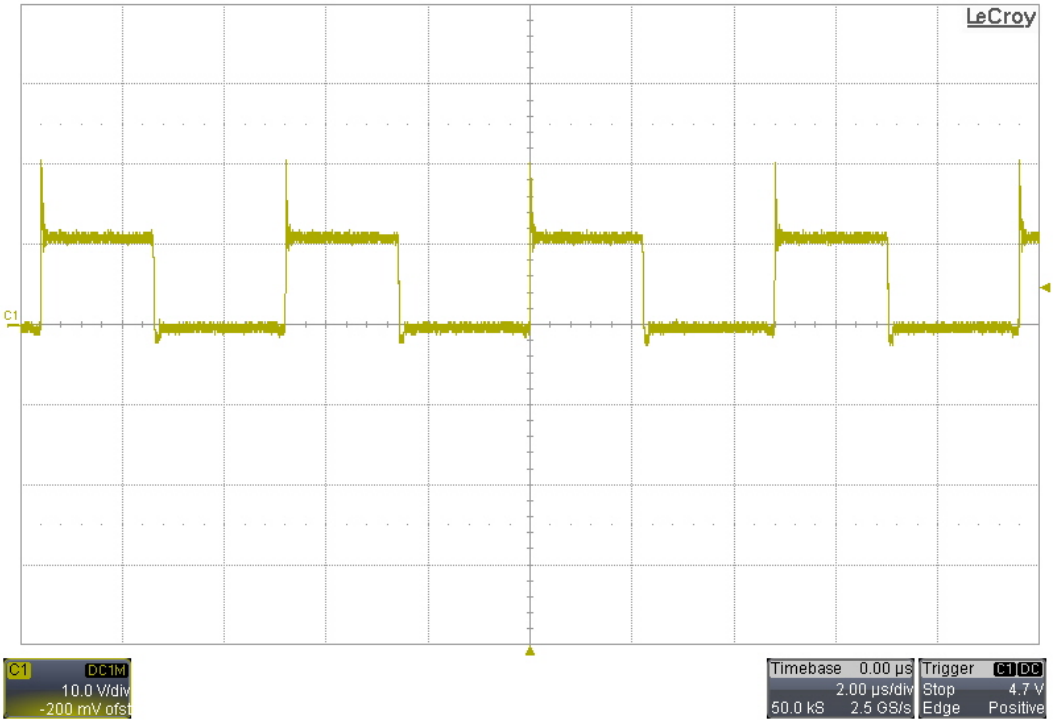


10 Synchronous FET Drain Waveforms

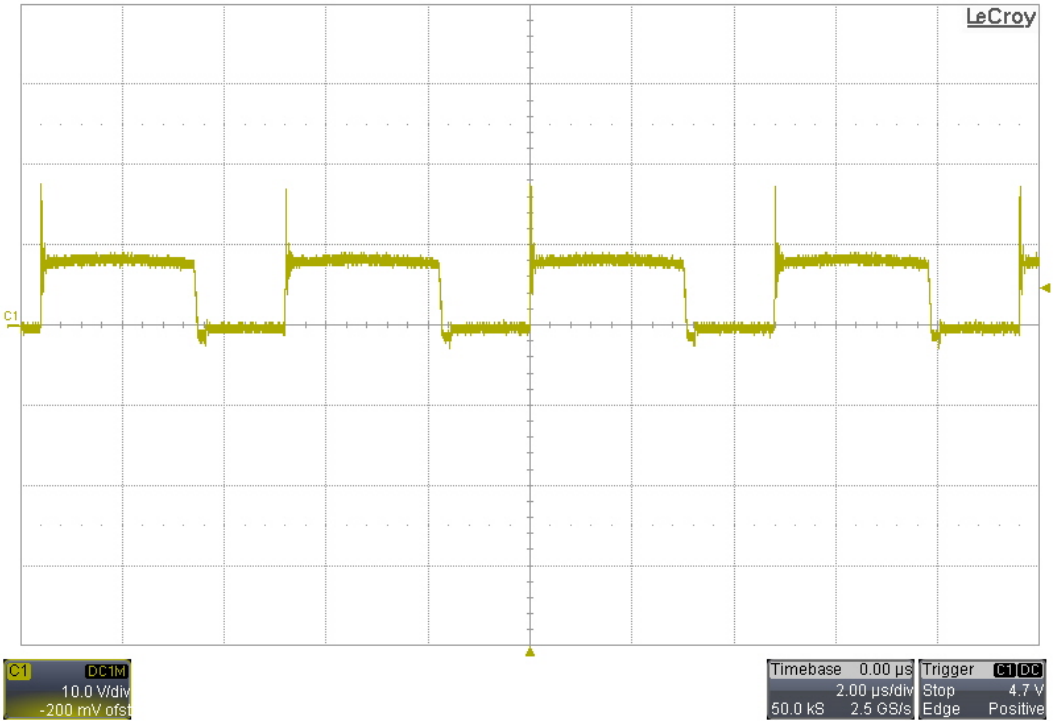
10.1 Q3 Synchronous FET Vds – 400VDC Input, 20A Load



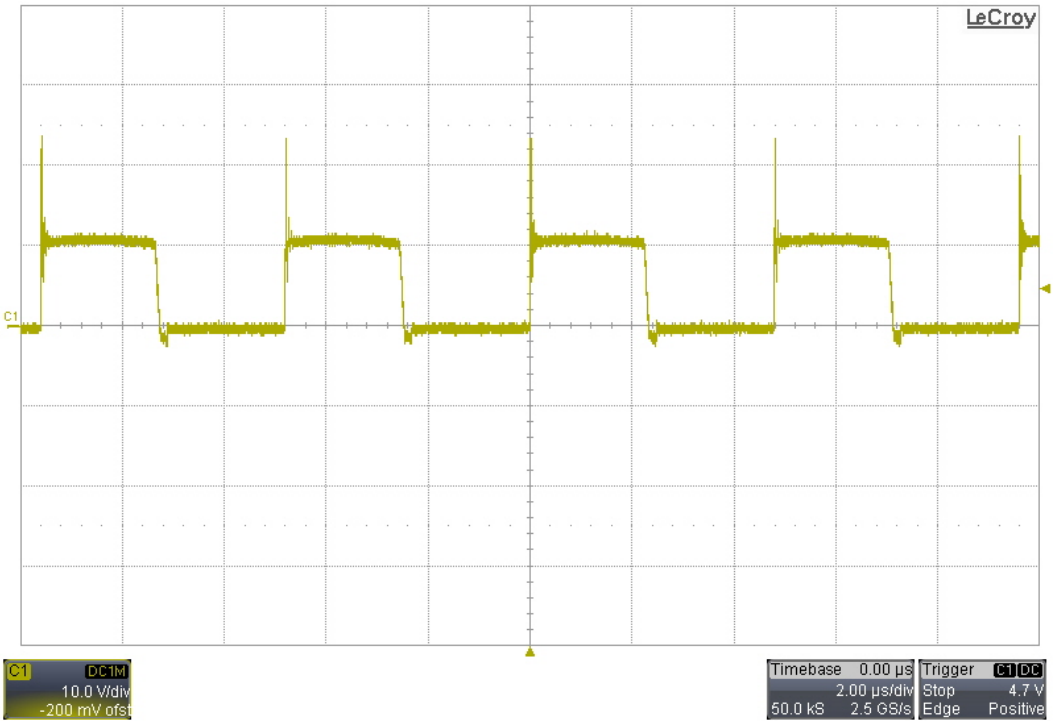
10.2 Q3 Synchronous FET Vds – 250VDC Input, 20A Load



10.3 Q10 Synchronous FET Vds – 400VDC Input, 20A Load

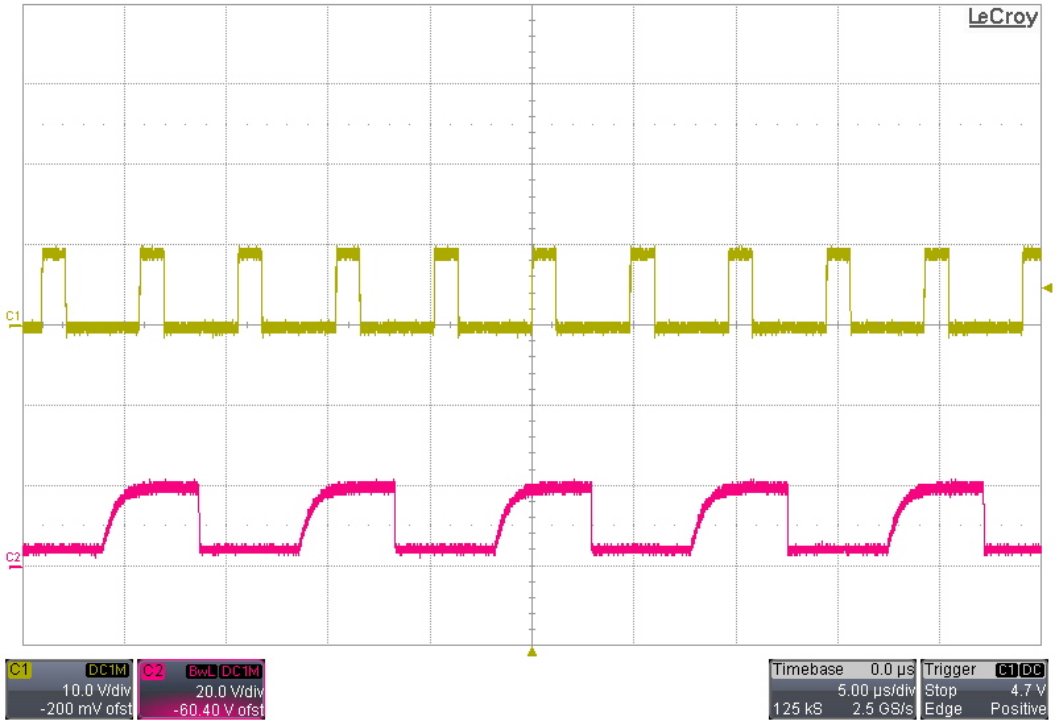


10.4 Q10 Synchronous FET Vds – 250VDC Input, 20A Load



11 Synchronization Output

Channel 1 shows the voltage on the gate of the primary FET (Q9). Channel 2 shows the sync output (TP5). The sync output signal was pulled up to an external 20V source through a 30k resistor.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265