PMP8824 REV.B Test Report

Table of Contents

Table of Figures

Requirements

1.1 Test Setup

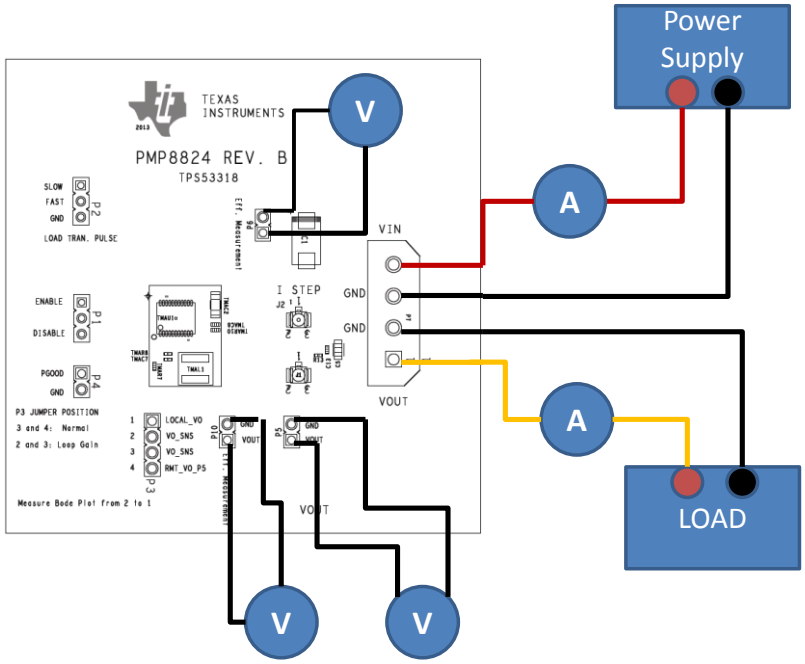


Figure 1 Test Setup of the TPS53318, 6A Tiny Macro, PMP8824 REV. B.

2.0 Test Results

2.1 Startup and Shutdown Behavior

2.1.1 Turn-on and Turn-off from VIN

- Enable line is connected so supply turns on and off with the rise and fall of Vin
- Vin rise time should be between 2V/msec and 3V/msec
- For this test, an external VCC supply will NOT be used. The IC's internal regulator will derive the gate drive voltage from Vin
- Vin should turn off by becoming high impedance (not actively driven low)
- Load applied to output to draw 10% of rated current when output voltage is at nominal
- Method employed to measure inductor current
- Scope waveform will show:
  - **ENABLE, 5V/DIV**
  - **Input voltage, 2V/DIV**
  - **Output voltage, 500mV/DIV**
  - **Phase Node, 10V/DIV**

Embed scope waveforms in tables below:

Table 1 Start-up and Shutdown Waveforms with VIN UVLO

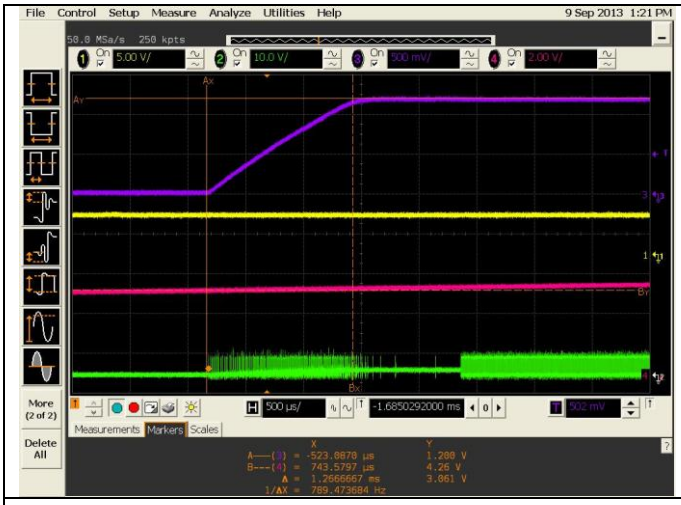
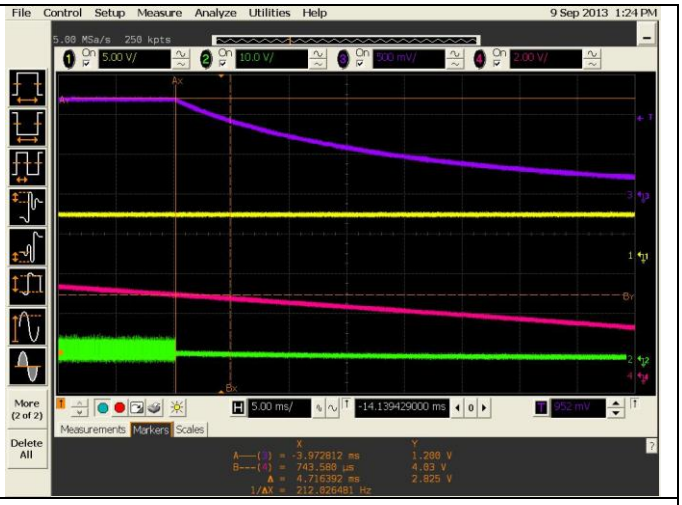
	

Figure 2 Turn-on, 10Vin, 1.2Vout, 10% of Rated Current	**Figure 3 Turn-off, 10Vin, 1.2Vout, 10% of Rated Current**

Figure 4 Turn-on, 10Vin, 0.8Vout, 10% of Rated Current	**Figure 5 Turn-off, 10Vin, 0.8Vout, 10% of Rated Current**

+

Comments:

- Start-up and shut-down are gated by VREG UVLO threshold. Measured VIN_UVLO_Threshold matches the datasheet spec.
- Measured soft-start ramp time is 1.2msec. Datasheet spec is 1.4msec.
- Converter operates in Discontinuous Current Mode during start up to prevent any reverse current.

2.1.2 Turn-on and Turn-off from Enable

- Enable line is toggled so supply turns on and off by enable control
- Resistive load applied to output to draw 10% of max current when output voltage is at nominal
- Method employed to measure inductor current of each phase
- Scope waveform will show:
  - **Output voltage, 500mV/DIV**
  - **Input voltage, 10V/DIV**
  - **Enable signal, 2V/DIV**
  - **Phase Node, 10V/DIV**

Embed scope waveforms in tables below:

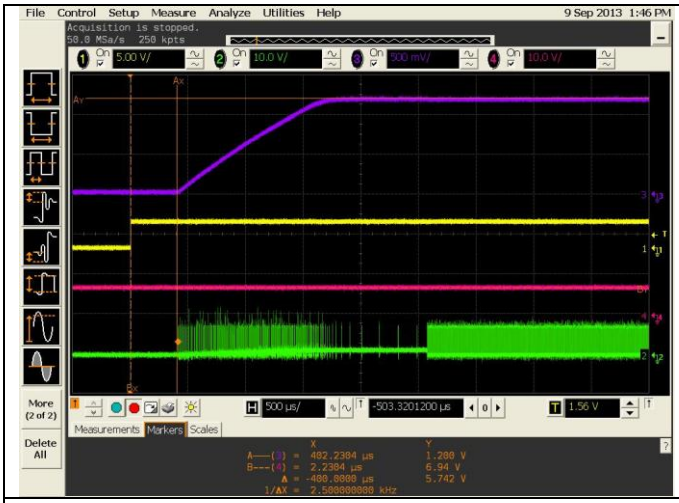


Figure 6 Turn-on, 7Vin, 1.2Vout, 10% of Rated Current

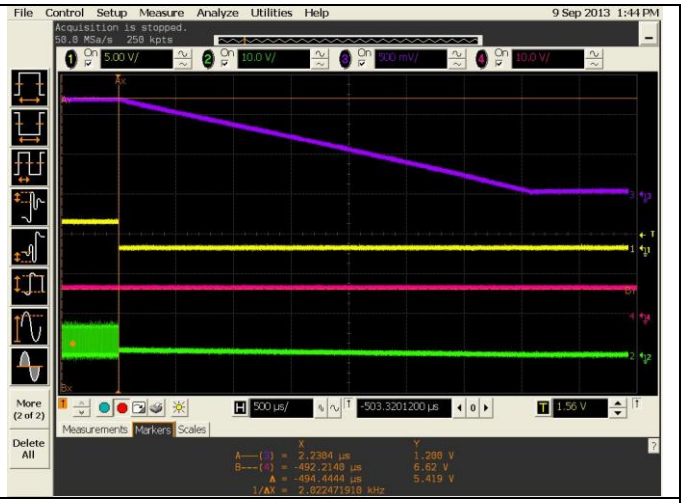


Figure 7 Turn-off, 7Vin, 1.2Vout, 10% of Rated Current

Figure 8 Turn-on, 10Vin, 1.2Vout, 10% of Rated Current

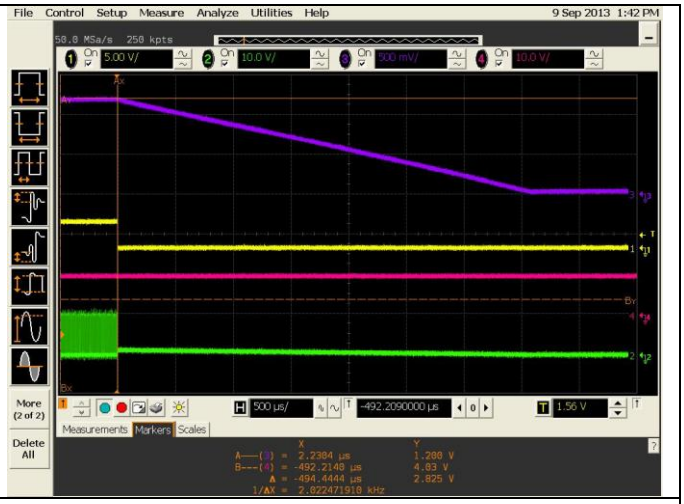


Figure 9 Turn-off, 10Vin, 1.2Vout, 10% of Rated Current

Figure 10 Turn-on, 12Vin, 1.2Vout, 10% of Rated Current

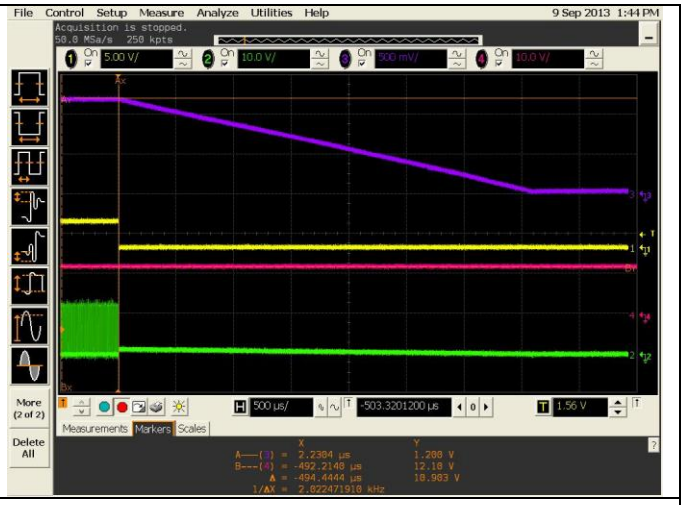


Figure 11 Turn-off, 12Vin, 1.2Vout, 10% of Rated Current

Comments:

- Measured soft-start ramp time is 1.2msec. Datasheet spec is 1.4msec
- Measured delay from ENABLE rising edge to first PWM is 377usec
- Measured delay from ENABLE falling edge to last PWM is minimum.
- Converter operates in Discontinuous Current Mode during start up.

2.1.3 PGOOD Signal

VIN = 10V

- **Output voltage, 500mV/DIV**
- **PGOOD, 5V/DIV**
- **Enable signal, 5V/DIV**
- **Phase Node, 10V/DIV**

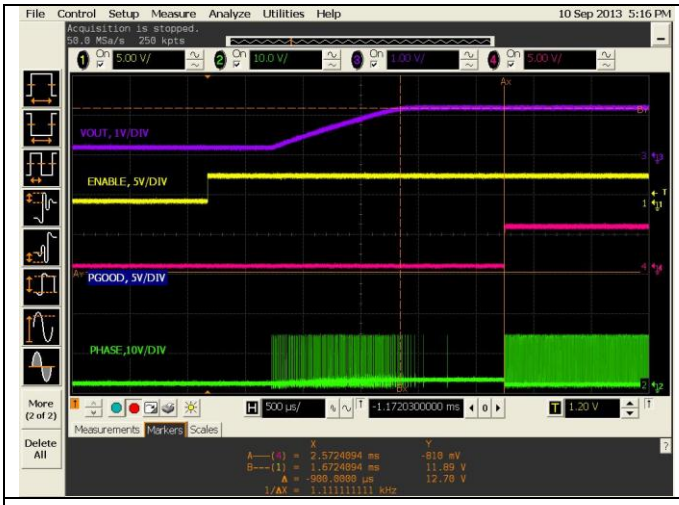


Figure 12 PG Turn-on, 12Vin, 10% of Rated Current

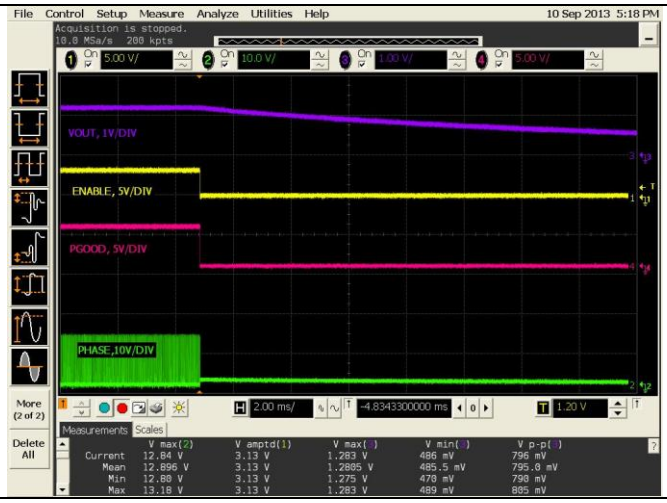
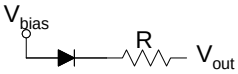


Figure 13 PG Turn-off, 12Vin, 10% of Rated Current

Comment: measured PGOOD delay matches datasheet specification.

2.1.4 Turn-on and Turn-off in presence of pre-bias on output



An external supply, Vbias, along with diode and series resistor is connected to the output to pre-bias the output voltage.

- Output voltage is pre-biased to > 60% of the nominal output voltage
- Supply is turned on and off via. enable control
- OK to capture behavior at 10Vin only
- Scope waveform will show:
  - **Output voltage, 100mV/DIV**
  - **Phase node voltage, 10V/DIV**

Prebiased output at 940mV.

Table 2 Prebiased Start-Up Waveforms.

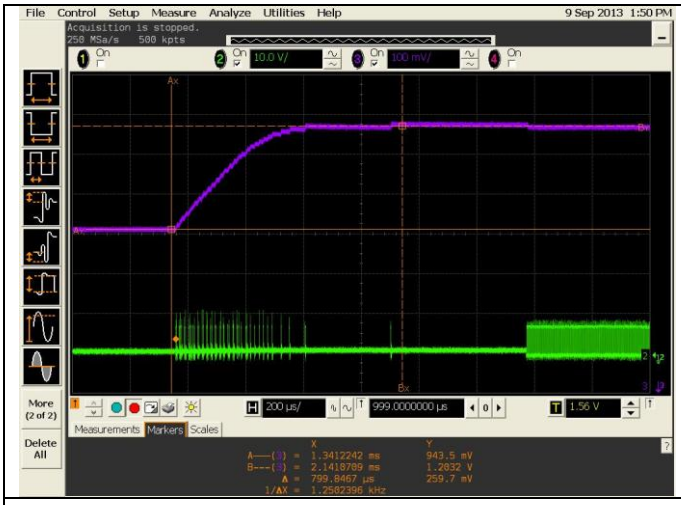


Figure 14 Prebias Turn-on, 7Vin, 1.2Vout

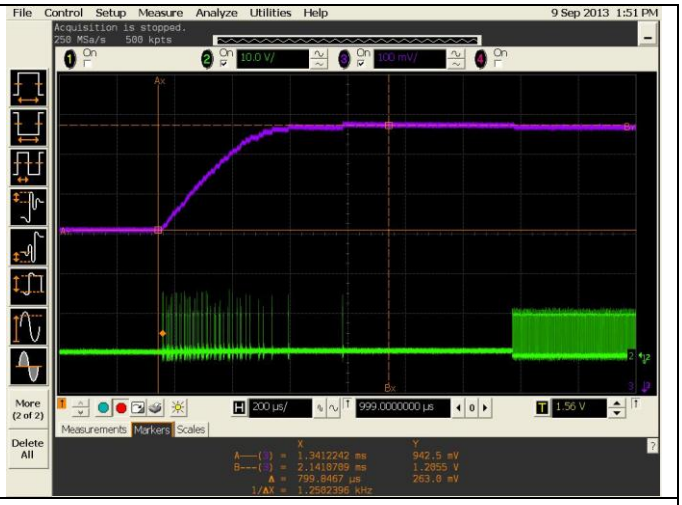


Figure 15 Prebias Turn-on, 10Vin, 1.2Vout

Figure 16 Prebias Turn-on, 12Vin, 1.2Vout

2.2 Voltage ripple and switch-node waveforms

2.2.1 Nominal input voltage conditions

- Use low-noise measurement technique to measure voltage ripple near output of converter
- Recommend switch-node measurement be made directly across low-side FET
- Use external load to measure waveforms at 10% and 100% of rated current
- Use full bandwidth mode on scope for phase node.
- Trigger off of first switch-node and use infinite persistence of scope to show duty-cycle “jitter”
- Scope waveform will show:
    - **Output voltage, 10mV/DIV**
    - **Phase node voltage, 5V/DIV**
    - **Time scale, 1usec/DIV**

- Oscilloscope
- Embed scope waveforms in tables below:

2.2.1.1 Voltage Ripple and Switch-node waveforms at VOUT = 1.2V

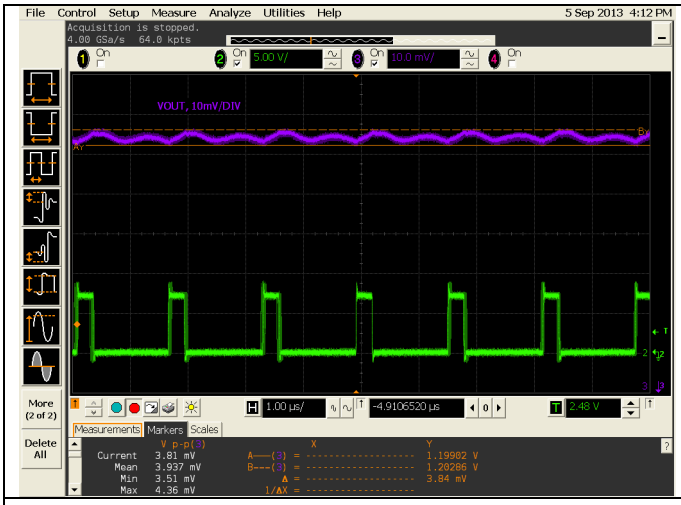


Figure 17 7Vin, 1.2Vout, No Load, Phase and Vout

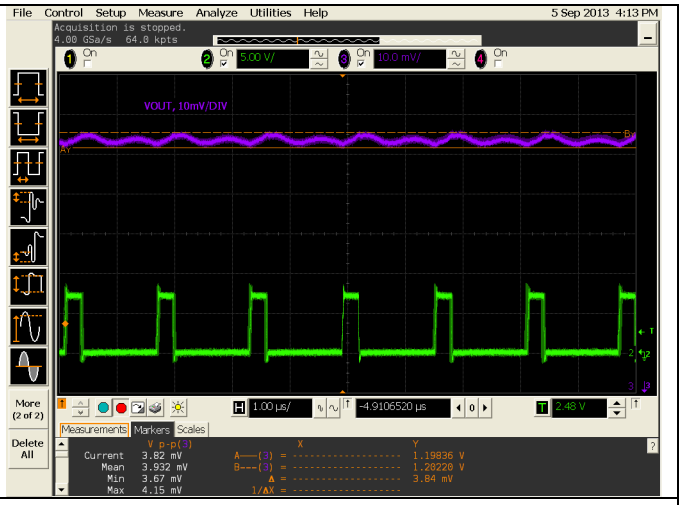


Figure 18 7Vin, 1.2Vout,10% Load, Phase and Vout

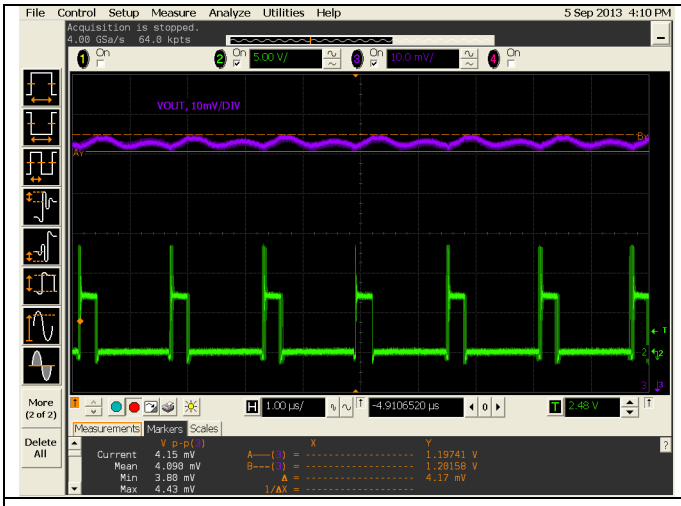


Figure 19 7Vin, 1.2Vout, 50%, Phase and Vout

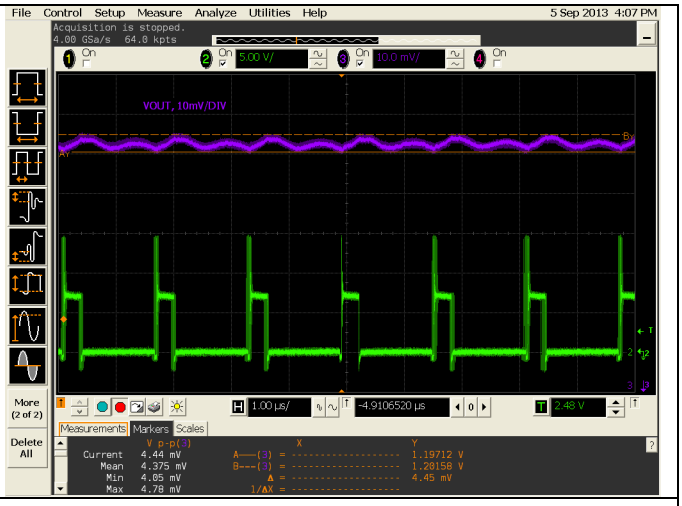


Figure 20 7Vin, 1.2Vout, 100%, Phase and Vout

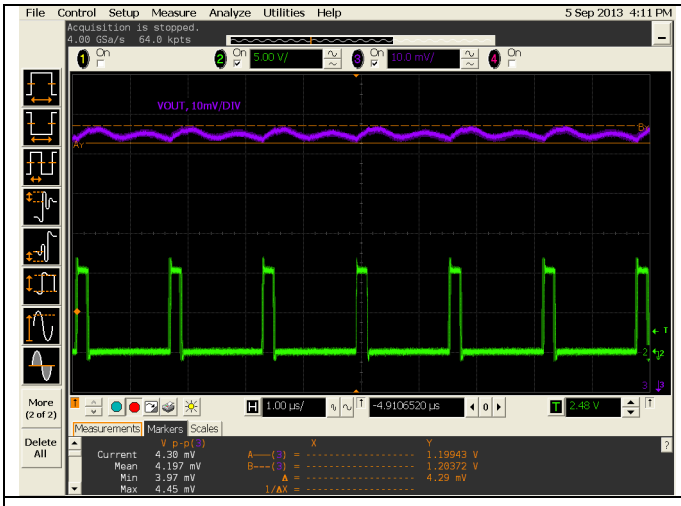


Figure 21 10Vin, 1.2Vout, No Load, Phase and Vout

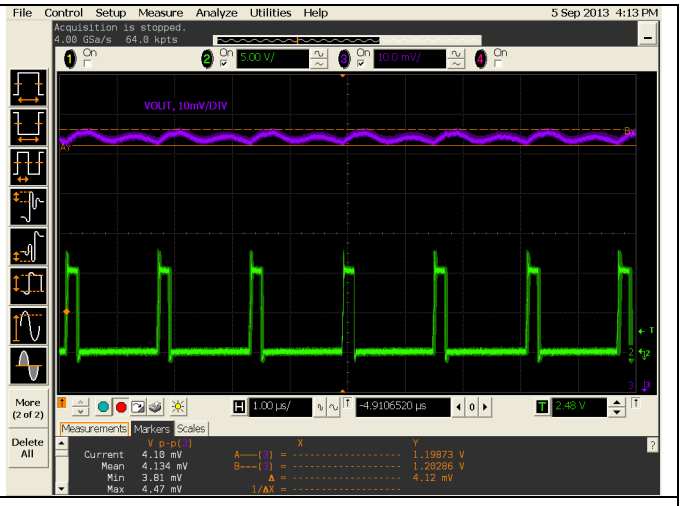


Figure 22 10Vin, 1.2Vout,10% Load, Phase and Vout

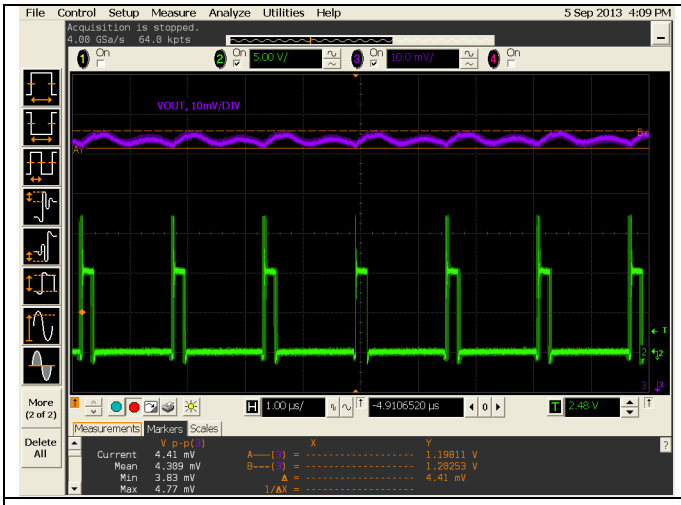


Figure 23 10Vin, 1.2Vout, 50%, Phase and Vout

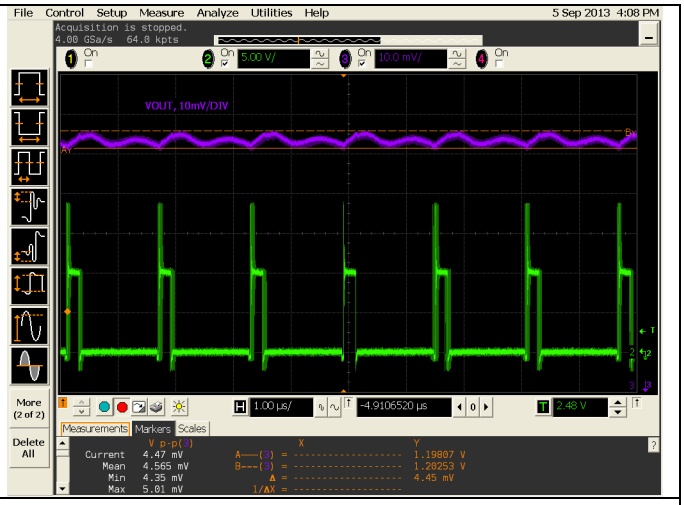


Figure 24 10Vin, 1.2Vout, 100%, Phase and Vout

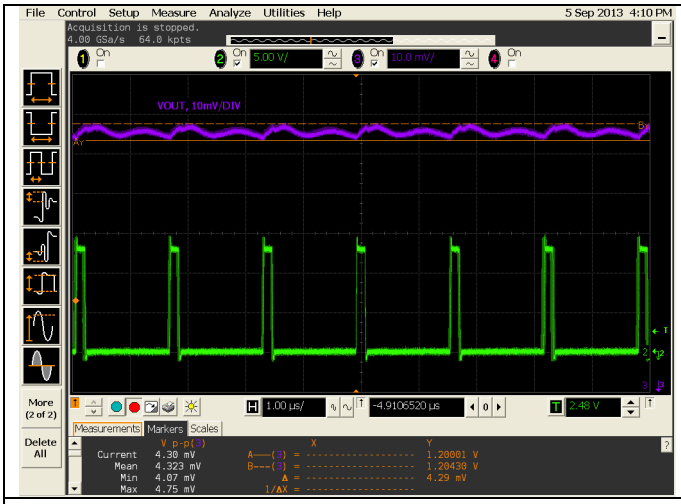


Figure 25 12.6Vin, 1.2Vout, No Load, Phase and Vout

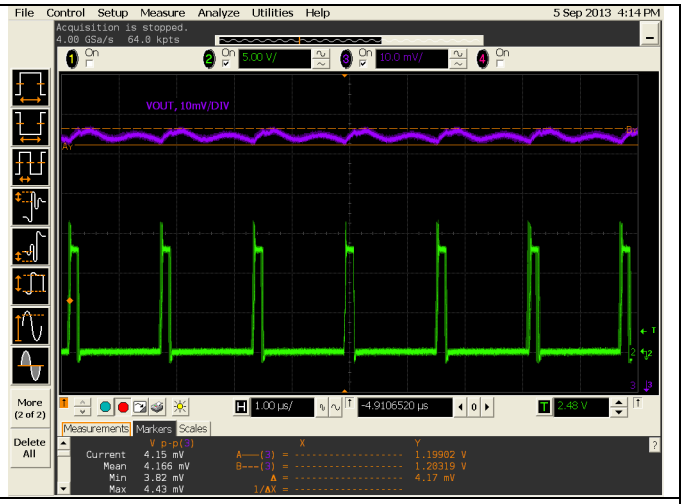


Figure 26 12.6Vin, 1.2Vout,10% Load, Phase and Vout

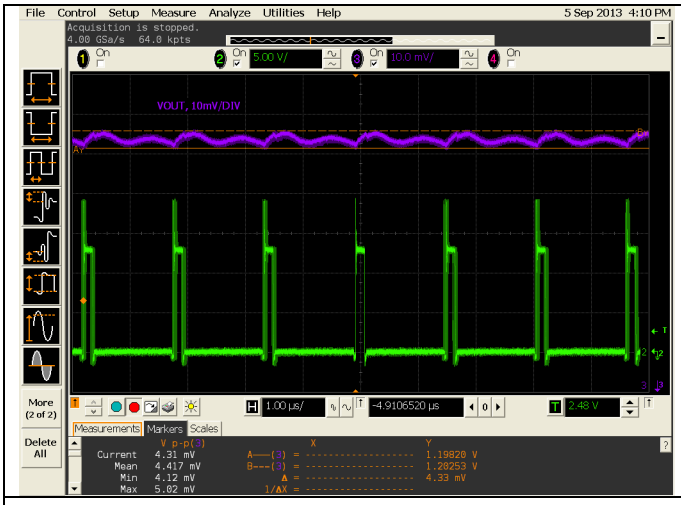


Figure 27 12.6Vin, 1.2Vout, 50%, Phase and Vout

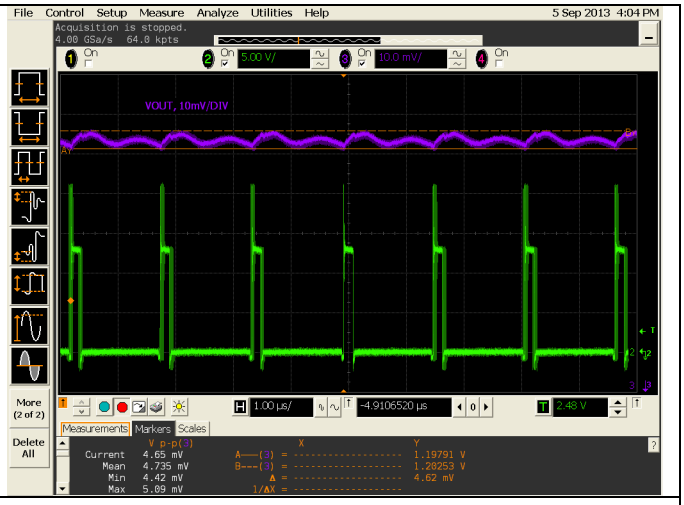


Figure 28 12.6Vin, 1.2Vout, 100%, Phase and Vout

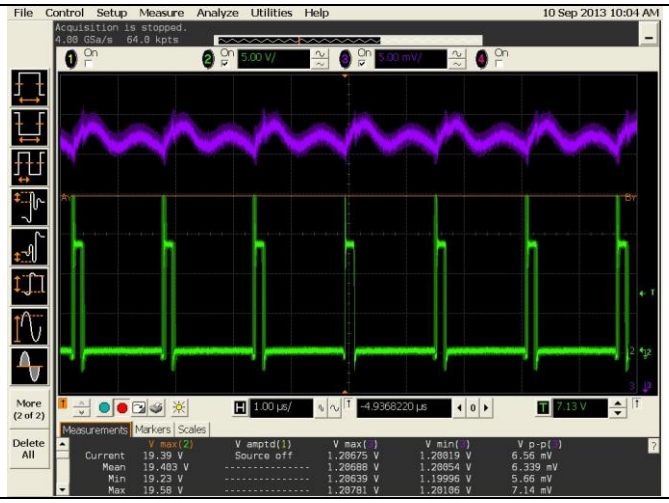


Figure 29 13.2Vin, 1.2Vout, 50%, Vout,5mV/DIV, Full BW

Comments:

- Output peak to peak ripple voltage worst case happens at VIN = 12.6V and 100% load.
- The maximum ripple voltage measured was **5.09mV**, ±0.212%.

2.2.1.2 Voltage Ripple with Broadband Noise at VOUT = 1.2V

- 20MHz Bandwidth, unless otherwise specified
- **Output voltage, 10mV/DIV**
- **Phase node voltage, 5V/DIV**
- Time scale, 20usec/div

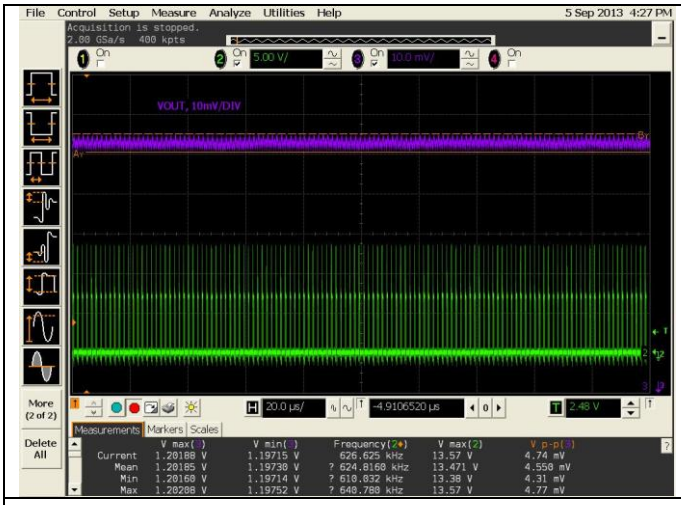


Figure 30 7Vin, 1.2Vout, 50% Load, Phase and Vout

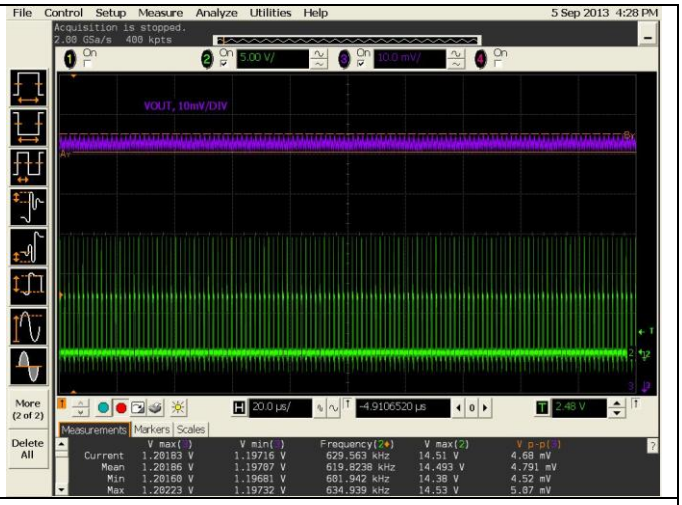


Figure 31 7Vin, 1.2Vout,100% Load, Phase and Vout

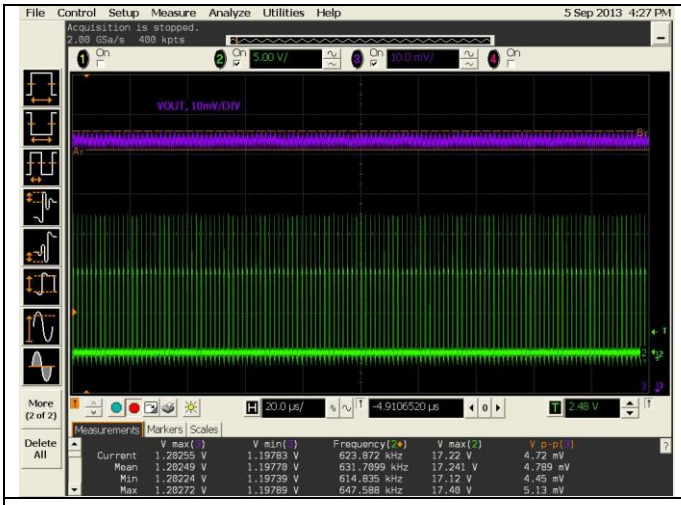


Figure 32 10Vin, 1.2Vout, 50%, Phase and Vout

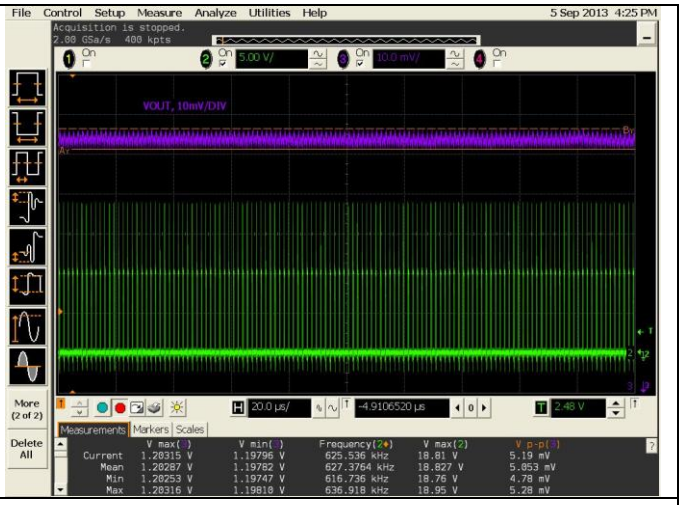


Figure 33 10Vin, 1.2Vout, 100%, Phase and Vout

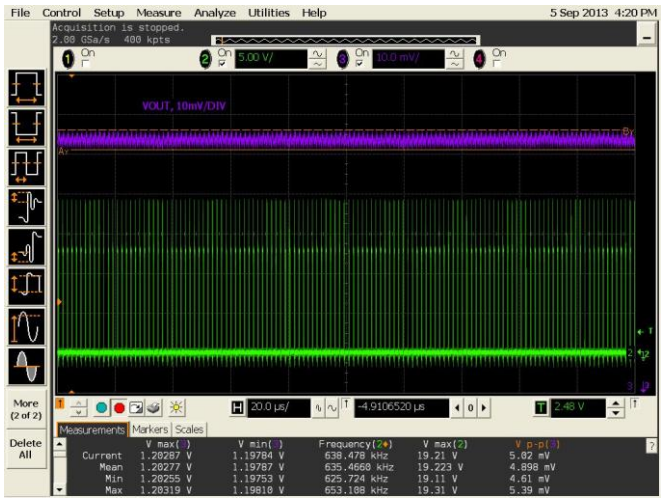


Figure 34 12.6Vin, 1.2Vout, 50%, Phase and Vout

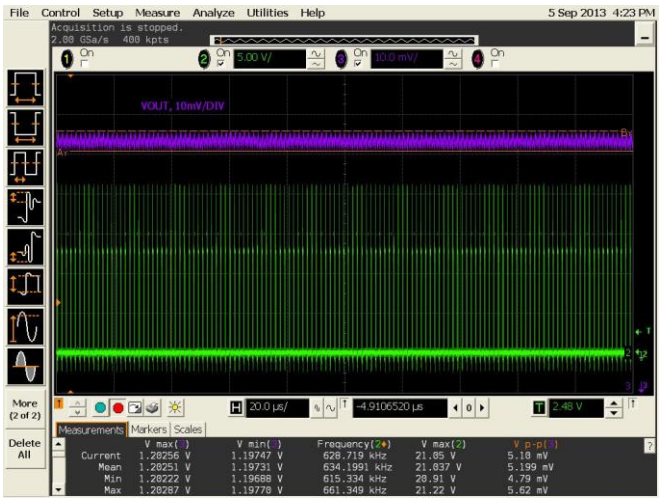


Figure 35 12.6in, 1.2Vout, 100%, Phase and Vout

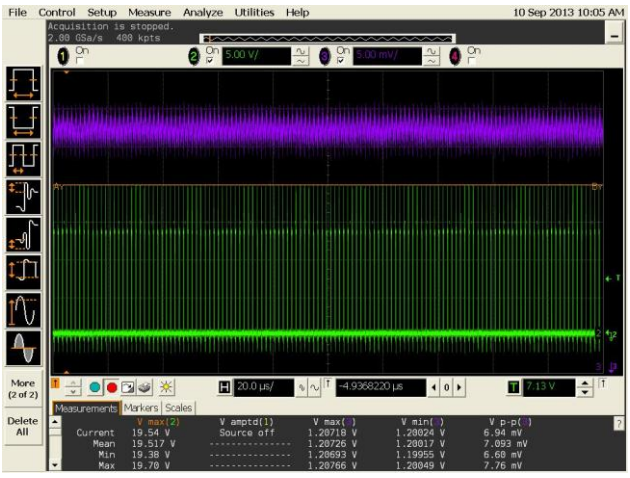


Figure 36 13.2in, 1.2Vout, 100%, Phase and Vout, 5mV/DIV, Full BW

Comments:

- Output peak to peak ripple voltage worst case happens at VIN = 12.6V and 100% load.
- The maximum ripple voltage including white noise measured was **5.62mV**. White noise contributes to output ripple by 0.53mV, 10% of the switching ripple.

2.2.2 Maximum jitter over input voltage range

In some instances (such as low or high duty cycle), switch-node jitter can increase. For this test, the input voltage will be swept between 7V and 12.6V and the condition that has the highest switch-node jitter will be captured

- Use low-noise measurement technique to measure voltage ripple near output of converter
- Recommend switch-node measurement be made directly across low-side FET
- Use external load to measure waveforms at 50% of rated current
- Use full bandwidth mode on scope
- Trigger off of first switch-node and use infinite persistence of scope to show duty-cycle “jitter”

R12 and C11 are for remote sensing and loop gain measurement.
For normal operation without remote sensing, it is recommended to set: R12 = 0Ω and C11 = 0.22uF

Compensation components Used for 1.2V output:
R11 = 6.19KΩ, C10 = 22nF, C9 = 470pF
R1 = 15KΩ, R2 = 14.7KΩ and R3 = OPEN.

Compensation components used for 0.8V output:
R11 = 5.11KΩ, C10 = 22nF, C9 = 680pF
R1 = 10KΩ, R2 = 9.76KΩ and R3 = 866KΩ,
Vsen is connected to remote VOUT through 5.1Ω resistor.

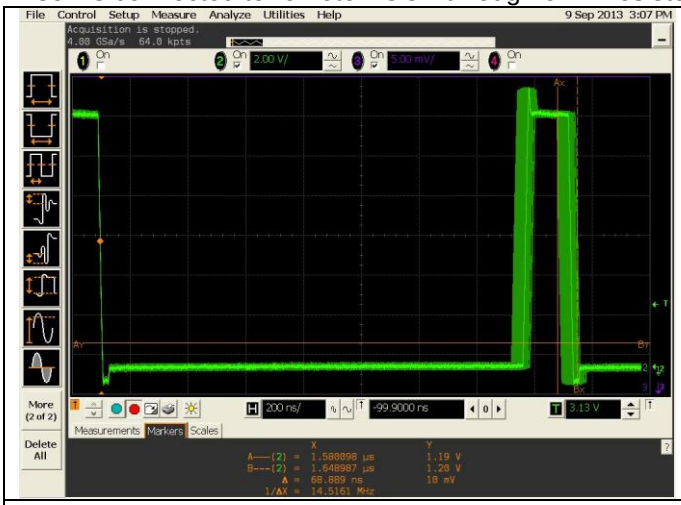


Figure 37 Vin swept 7-12.6V, 1.2Vout, No Load
Input voltage captured: 12.6V. 69nsec

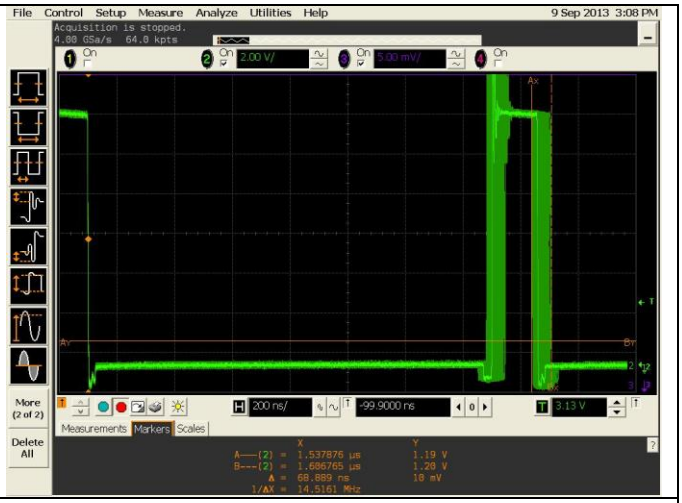


Figure 38 Vin swept 7-12.6V, 1.2Vout, 50% Load
Input voltage captured: 12.6V. 69nsec

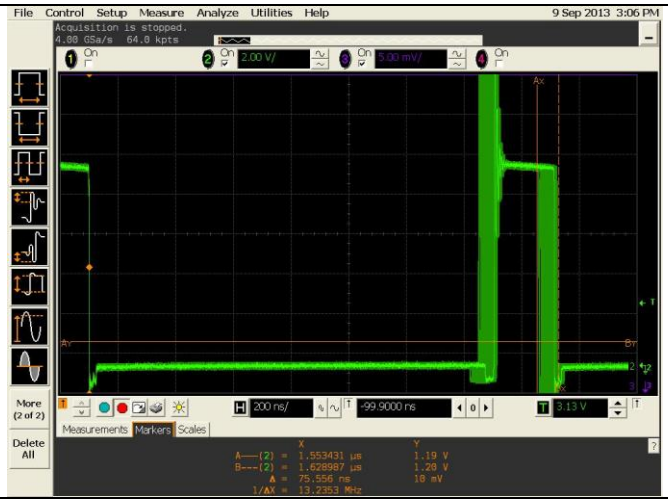


Figure 39 Vin swept 7-12.6V, 1.2Vout, 100% Load, Input voltage captured:10V, 75.5nsec

2.2.3 Maximum Phase Node Voltage Stress

Test Conditions:

- **Inductor: XAL5030 0.8uH**
- **Fsw = 600KHz**
- **Snubber = 220pF + 1.3Ω**
- **Bootstrap circuit: Rboot = 2.2Ω, Cboot = 0.1uF, 0402, X5R**

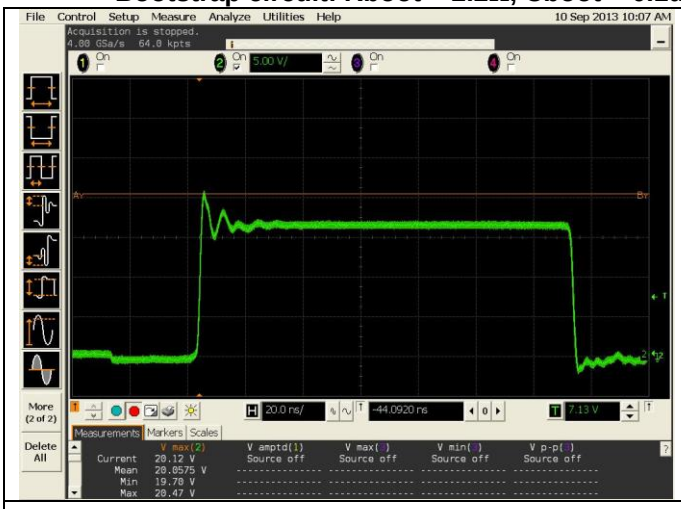


Figure 40 16Vin, 1.2Vout, 6A, Phase

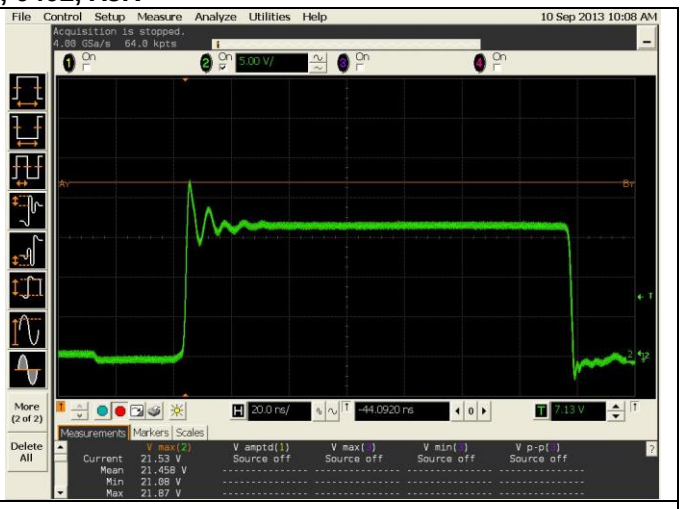


Figure 41 16Vin, 1.2Vout, 8A, Phase

Figure 42 18Vin, 1.2Vout, 6A, Phase

Figure 43 18Vin, 1.2Vout, 8A, Phase

Comments:

- TPS53318 Phase Pin Absolute Maximum Rating 31V @ 10nsec
- Measured Maximum Phase Pin Voltage Stress at VIN = 18V is 21V, which is below 24.8V, 80% of the Absolute Maximum Rating.

2.3 Efficiency

Provide charts and tables of DC/DC conversion efficiency from 10% to 100% of rated load for each condition:

2.3.1 Efficiency at VOUT = 1.2V

Efficiency of Alternative inductors is also measured. The alternative inductor meets the thermal stress requirement. Thermal data were taken with ambient temperature = 23.7 deg C, VIN = 12V and Io = 6A.
Comments:

- Inductor XAL5030-801M
- Measure surface temperature of the TPS53318 is 41 deg C. Temperature rise is 17.3 deg C.
- Measured surface temperature of the XAL5030 is 43.6 deg C. Temperature rise is 19.9 deg C.

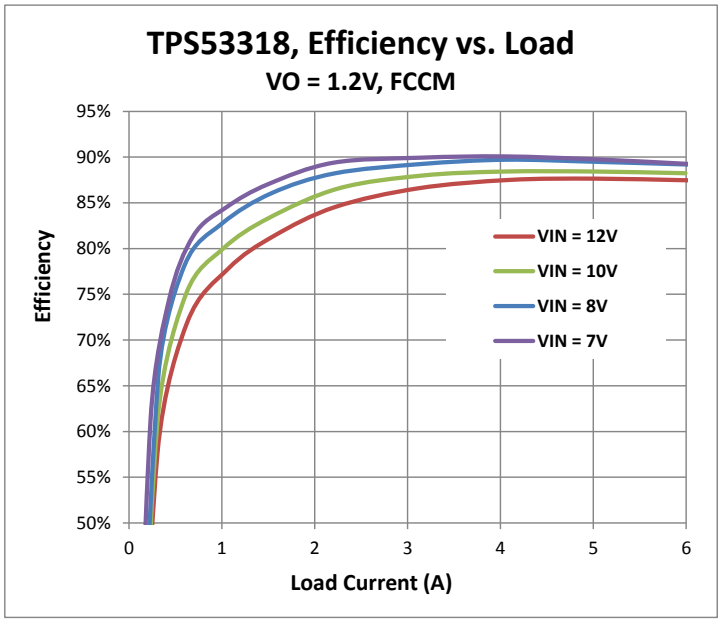


Figure 44 Efficiency vs. Load at different VIN, VO= 1.2V.

2.4 Loop Stability

Using appropriate analyzer, capture loop response of each test condition at 10% and 100% load. It is expected that loop will be tuned for good bandwidth with minimum 10dB gain margin and 45° phase margin.
In each case below, please determine and note:

- Cross-over frequency
- Phase margin
- Gain margin

2.4.1 Loop Stability at VOUT = 1.2V

Compensation components Used for 1.2V output:
R14 = 6.19KΩ, C10 = 22nF, C9 = 470pF
R1 = 15KΩ, R2 = 14.7KΩ and R3 is NOT stuffed.

2.4.1.1 Bode plots at VIN = 10V and VOUT = 1.2V

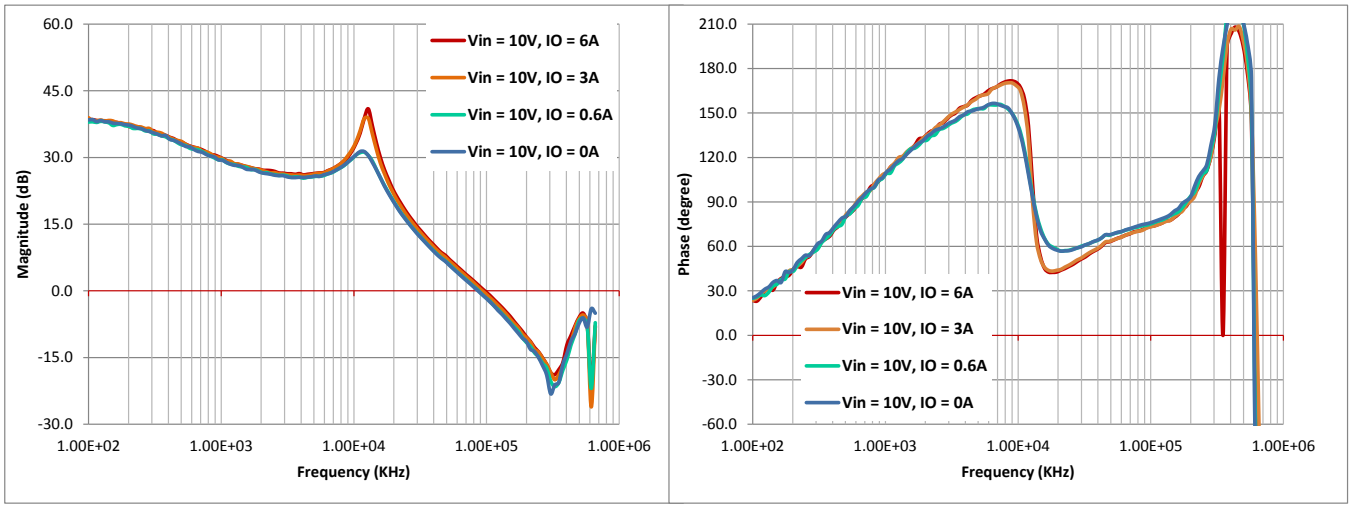


Figure 45 Bode plots of Voltage Loop at VIN = 10V.

Comments:

- Control Bandwidth is from 85 KHz to 96 KHz.
- Phase margin is greater than 73 deg.

2.4.1.2 Bode plots at VIN = 12.6V and VOUT = 1.2V

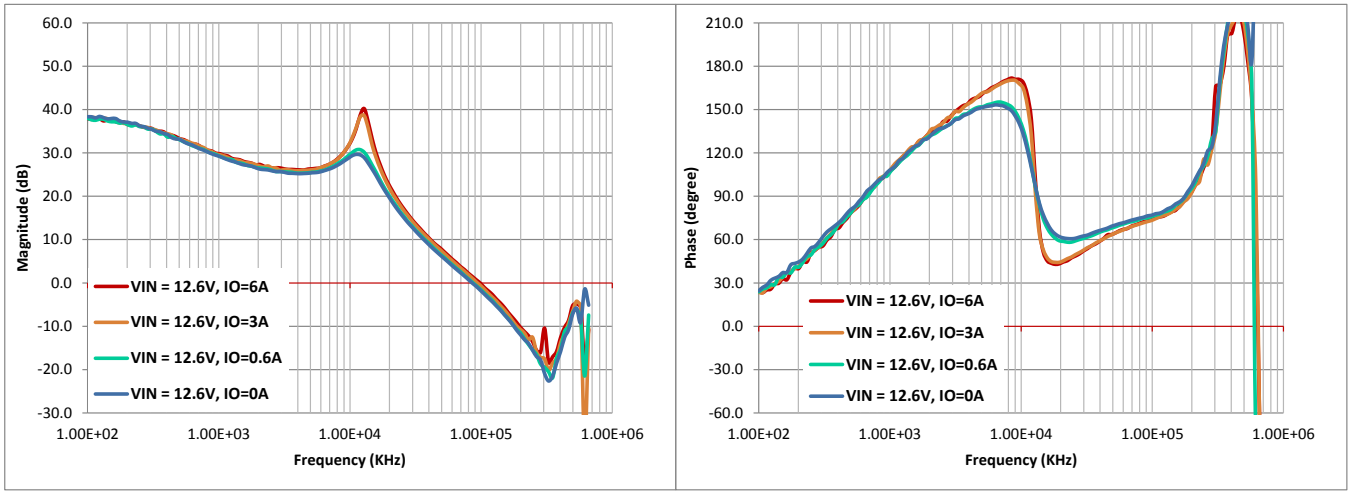


Figure 46 Bode plots of Voltage Loop at VIN = 12.6V.

Comments:

- Control Bandwidth is from 86 KHz to 96 KHz.
- Phase margin is greater than 74 deg.

2.5 Load transient response

- Scope waveform will show:
  - **Output voltage (20mV/DIV, DC coupling)**
  - **Transient current (1/DIV, 1A/100mV)**

Table 3 Load Transient Response for 1.2V output with 50% Load Step (50% to 100% and 100% to 50%)

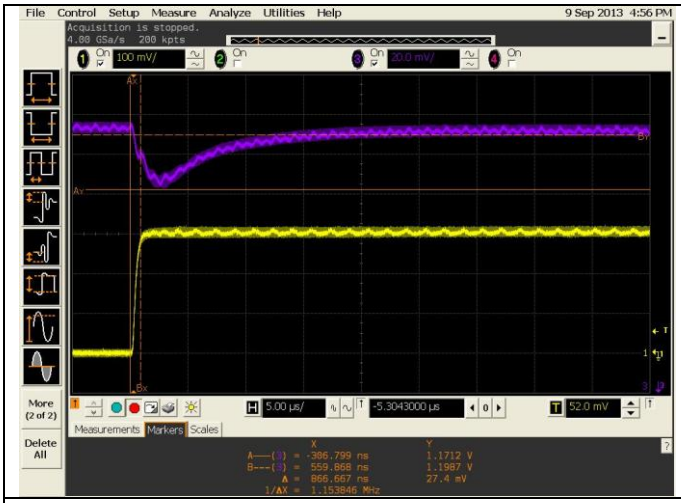


Figure 47 7Vin, 1.2Vout, 50% to 100% Load Step

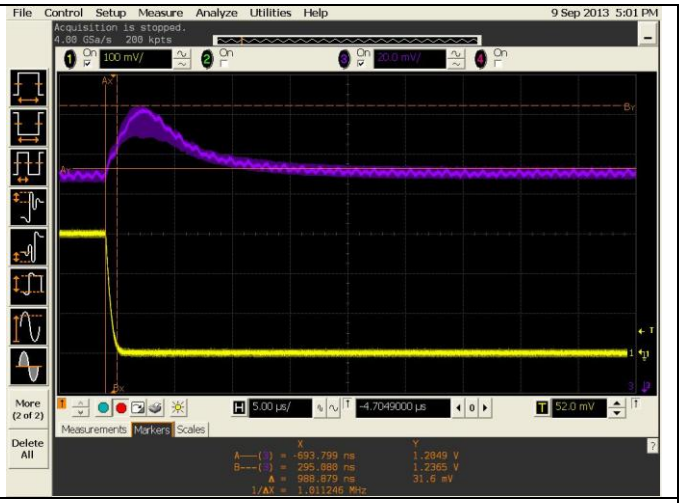


Figure 48 7Vin, 1.2Vout, 100% to 50% Load Step

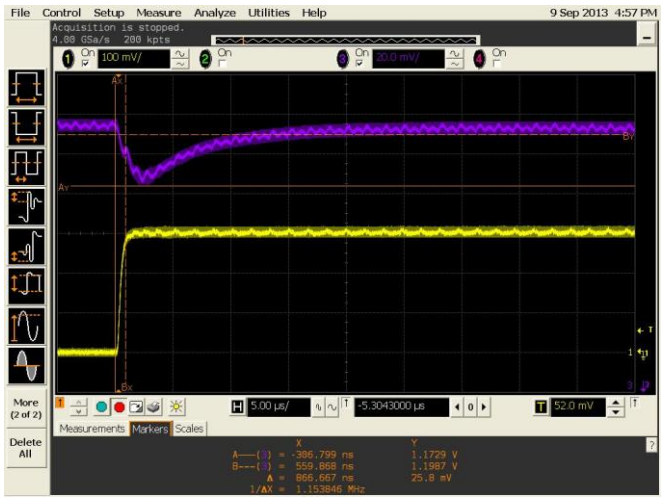


Figure 49 10Vin, 1.2Vout, 50% to 100% Load Step

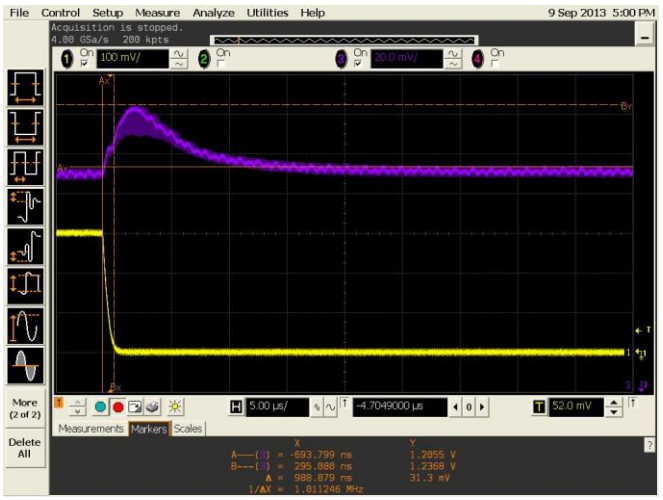


Figure 50 10Vin, 1.2Vout, 100% to 50% Load Step

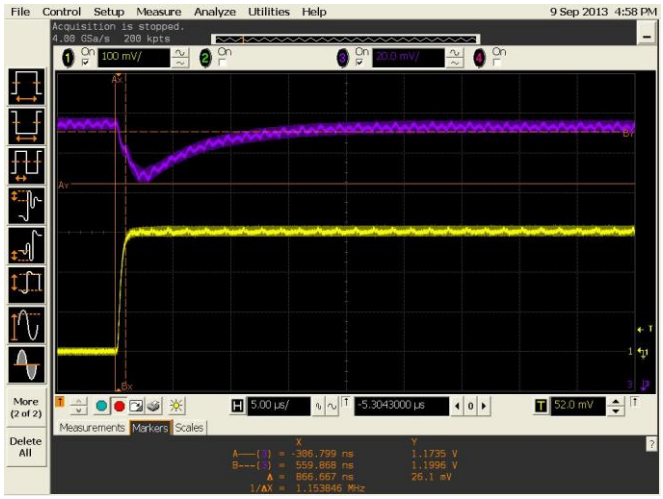


Figure 51 12.6Vin, 1.2Vout, 50% to 100% Load Step

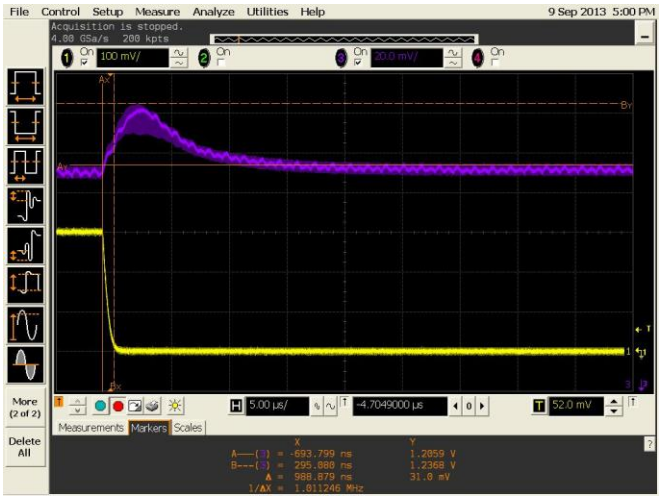


Figure 52 12.6Vin, 1.2Vout, 100% to 50% Load Step

Comments:

- Worst case 50% step up undershoot is 27.4mV, 2.28%
- Worst case 50% step down overshoot is 31.9mV, 2.66%

2.6 Load and Line Regulation

2.6.1 Load and line regulation for VOUT = 1.2V

R12 and C11 are for remote sensing and loop gain measurement.
If remote sensing is not necessary, it is recommended to set : R12 = 0Ω and C11 = 0.22uF
When remote sensing is in place, it is recommended to set R12 = 49.9Ω and C11 = 0.22uF. **Connect Vsen to remote sensing point through a 5.1Ω resistor.**

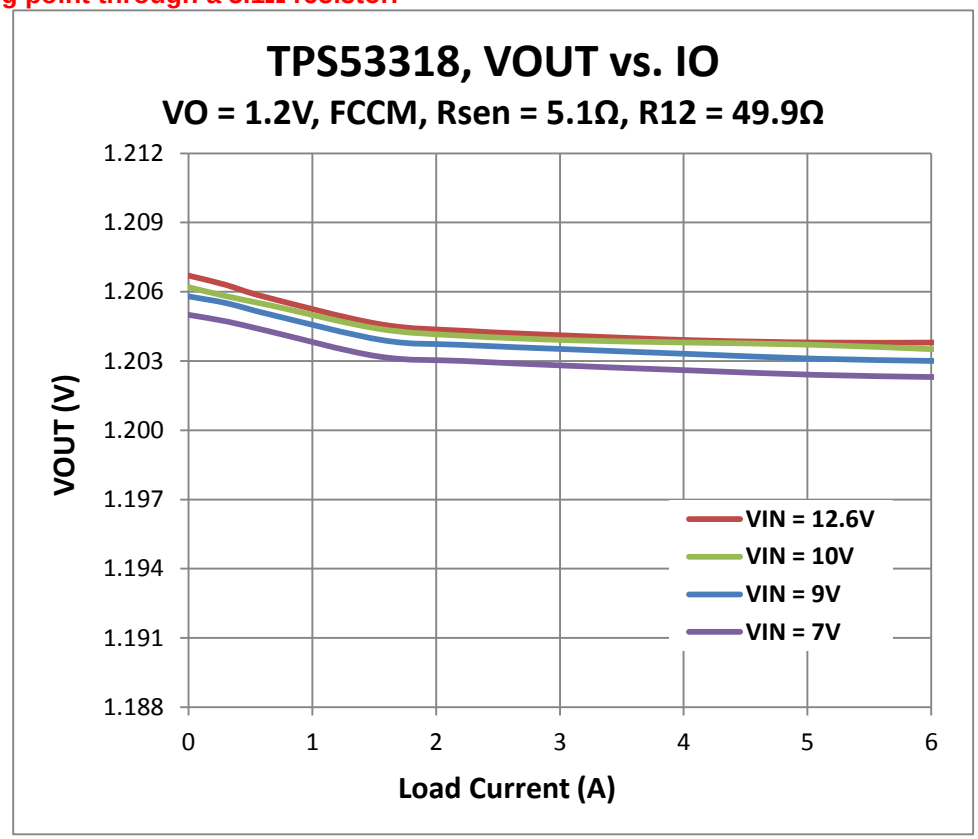


Figure 53 Output Regulation with Rsen = 5.1Ω for VOUT = 1.2V

2.7 Over-current response

2.7.1 Over-current response behavior

- Use external electronic load in constant-resistance mode to increase the load until the output falls out of regulation.
- Use current probe to capture load current
- Recommend ramp from no-load to output out of regulation be 20-50msec
- Method employed to measure inductor current

TMACROC = 88.7KΩ
Ioc_trip_Valley_nominal = 7.1A

Ioc_trip_Valley_min = 6.06A

- Scope waveform will show:
  - **Output voltage**
  - **Inductor current**
  - **Phase node**

Table 4 Load Regulation and over-current protection

Figure 54 7Vin, 1.2Vout, Load regulation and over-current protection

Figure 55 8Vin, 1.2Vout, Load regulation and over-current protection

- Converter becomes constant current source when it is over-loaded
- OC_Valley measured is 6.5A.

2.7.2 Over-current thermal stress

Maximum inductor valley current occurs at VIN = 7V and full load condition.

OC_TRIP should be set higher than this max. Inductor valley current.

Max. Inductor valley current = 4.9A.

Set TMACROC = 88.7KΩ. Then minimum valley OC trip point is 6.06A and nominal valley OC trip point is 7.12A at VIN = 7V.

Measured OC Load current = 8.23A.

At VIN = 12.6V, ambient temp. = 22.6 deg C, and IOUT = 8.21A.

Measured FET case temperature = 51.6 deg C. Temperature rise is 29 deg C.
Measured inductor surface temperature = 53.9 deg C. Temperature rise is 31.3 deg C

2.8 Short circuit protection and recovery

- Use reliable method to apply hard short circuit to the output
- Have method to capture current through short circuit so it can be displayed on the scope

- Method employed to measure inductor current of each phase
- Capture the inception as well as the release of the short circuit
- Scope waveform will show:
  - **Output voltage, 1V/DIV**
  - **Inductor current, 5A/DIV**
  - **Phase node, 10V/DIV**

Embed scope waveforms in tables below:

Table 5 Short circuit protection entry and recovery, VOUT = 1.2V

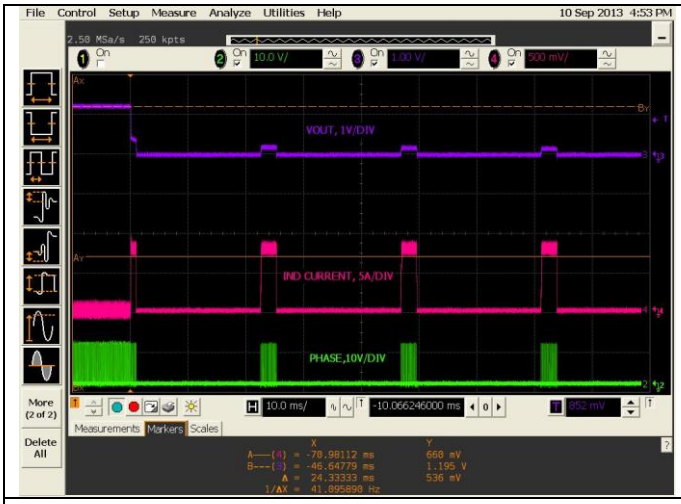
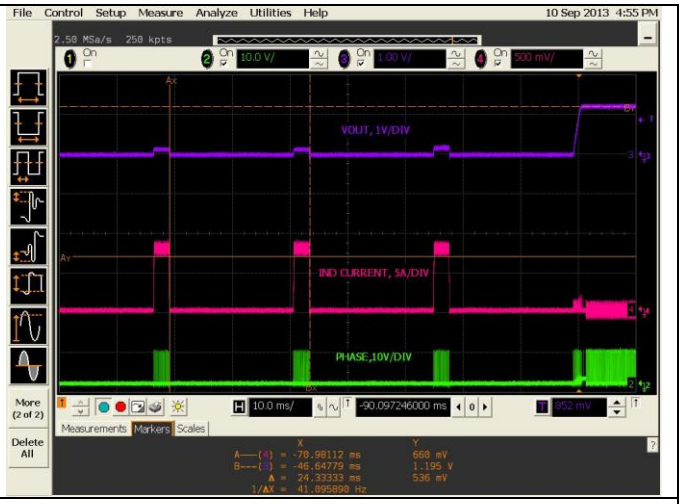
	

Figure 56 8Vin, 1.2Vout, Short circuit applied	**Figure 57 8Vin, 1.2Vout, Short circuit released**

Comments:

- Measured hiccup interval is 24.33msec. Expected hiccup interval is 20.6msec. Measurement matches expectation.
- Current stress during hiccup is reduced to 3.09Arms.

2.9 Power up into a short circuit

- Apply hard short circuit across the output
- Have method to capture current through short circuit to it can be displayed on the scope
- Use enable control to turn on device, and trigger scope on this signal
- Method employed to measure inductor current of each phase
- Scope waveform will show:
  - **Output voltage, 1V/DIV**
  - **Input voltage, 10V/DIV**
  - **Inductor current, 5A/DIV**
  - **Phase node, 10V/DIV**

Embed scope waveforms in tables below:

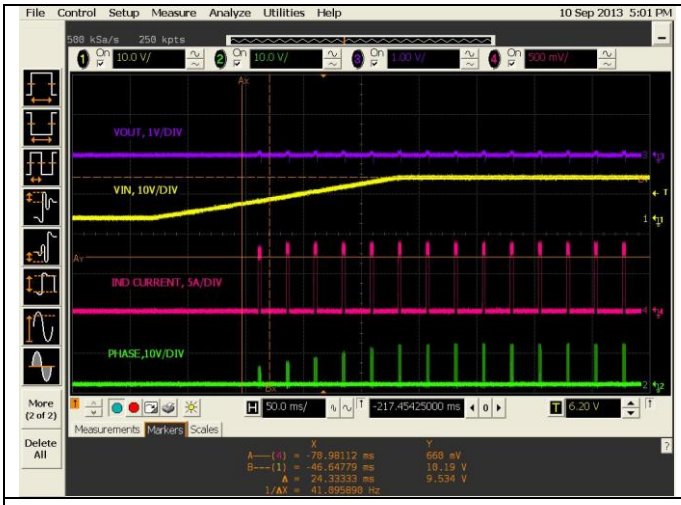


Figure 58 10Vin, 1.2Vout, Startup into short circuit

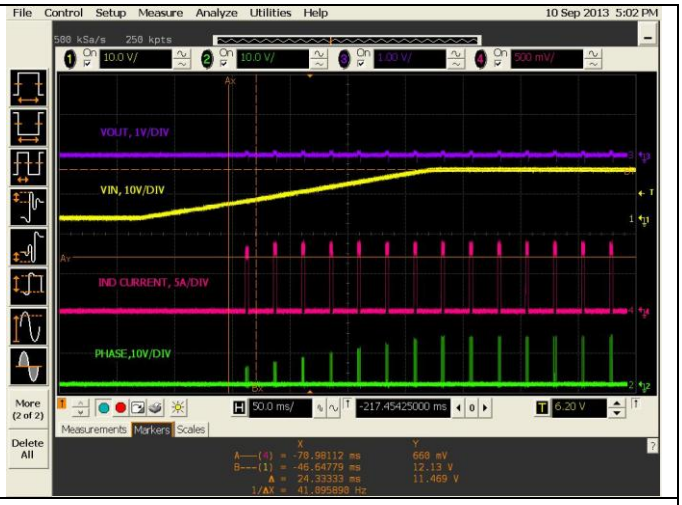


Figure 59 12Vin, 1.2Vout, Startup into short circuit

2.10 Enabling into a short circuit

- Apply hard short circuit across the output
- Have method to capture current through short circuit to it can be displayed on the scope
- Use enable control to turn on device, and trigger scope on this signal
- Method employed to measure inductor current of each phase
- Scope waveform will show:
  - **Output voltage, 1V/DIV**
  - **ENABLE, 5V/DIV**
  - **Inductor current, 5A/DIV**
  - **Phase node, 10V/DIV**

Figure 60 12Vin, 1.2Vout, Enable into short circuit

2.11 Output Over-Voltage by Transient

Perform test that demonstrates controller's response to output over-voltage condition. Vendor may suggest method, but recommended approach is to apply an external source to the output. Note care must be taken to prevent the input supply from being boosted up by the synchronous action of the controller.

- Have method to capture current through external source to it can be displayed on the scope
- Method employed to measure inductor current of each phase
- Scope waveform will show:

- **RVOP, 200mV/DIV**
- **FB pin Voltage, 200mV/DIV**
- **Inductor current, 10A/DIV**
- **Phase Node, 10V/DIV**

Embed scope waveforms in tables below:

Table 6 Over-Voltage-Protection

Figure 61 7Vin, 1.2Vout, Over-Voltage-Protection, Latch Off

Figure 62 7Vin, 1.2Vout, Extreme transient response, No Latch

Figure 63 12Vin, 1.2Vout, Over-Voltage-Protection, Latch Off

2.12 Feedback Shorted to GND

FB pin is pulled down to GND.

- Scope waveform will show:
  - **RVOP, 200mV/DIV**
  - **FB pin Voltage, 200mV/DIV**
  - **Inductor current, 10A/DIV**
  - **Phase, 10V/DIV**

Embed scope waveforms in tables below:

Figure 64 **12Vin, 1.2Vout, FB shorted to GND**

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265