UCC24624EVM-015 LLC Synchronous Rectifier (SR) Gate Driver Evaluation Module

User's Guide

Literature Number: SLUUBW4A
July 2018–Revised December 2018

1 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and nonconductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. After EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

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3. Personal Safety
   a. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

UCC24624EVM-015 LLC Gate Driver Evaluation Module

2 Introduction

The UCC24624EVM-015 evaluation module (EVM) is used to replace output rectifier's diodes in an LLC power converter to synchronous rectifiers (SR) MOSFETs. The SR-MOSFETs can achieve very low conduction loss compared to that of rectifier diodes, significantly improving the efficiency of the converter.

This user's guide provides the schematic, component list of materials, and installation instructions necessary to evaluate the UCC24624 in an LLC power converter.

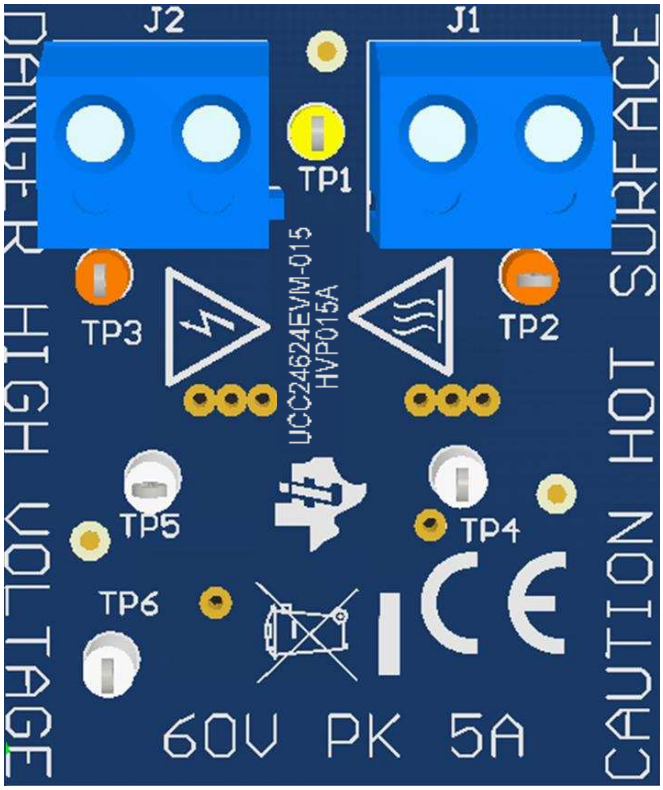

Figure 1. UCC24624EVM-015 (Top View)

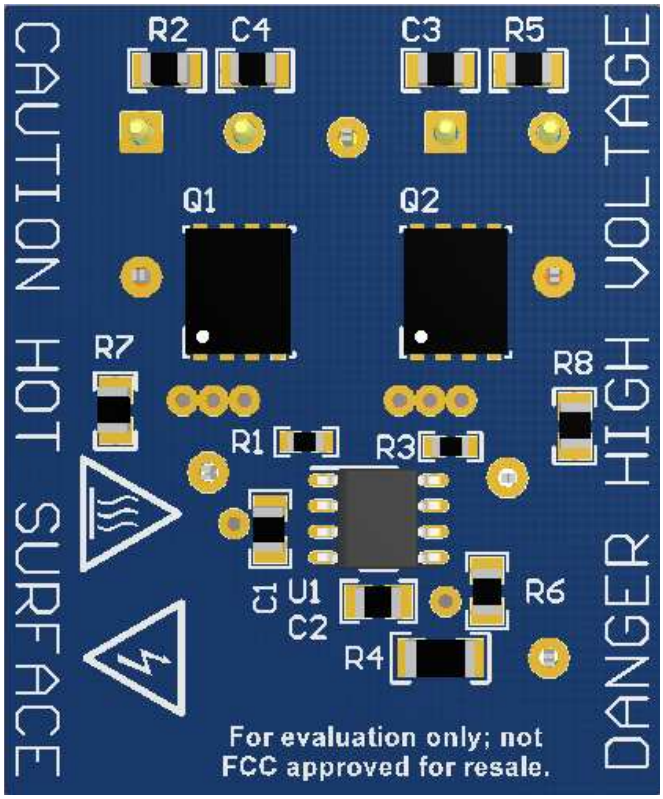

Figure 2. UCC24624EVM-015 (Bottom View)

3 Description

This EVM comes with UCC24624 LLC synchronous driver installed with two **60V**, 158A 2.5 mΩ FETs and all the supporting R, Cs and connectors to replace standard rectifier diodes with SR-MOSFETs in an LLC power converter.

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Please note with convection cooling this EVM can only operate with 5A of average current through each FET for a total of 10A maximum output current.

Six test points and two terminal blocks provide access to several important nodes in the SRs control circuit. Refer to the schematic diagram of the UCC24624EVM-015 in figure 3 for test points and terminal block connections .

The 2-position terminal blocks (J1 and J2) are used to connect the on-board MOSFETs source and drain nodes to the application using wires. Short lengths of bare wire, 20 AWG – 18 AWG (0.75 – 1 mm diameter), are best but other sizes with or without insulation can be used.

4 Schematic

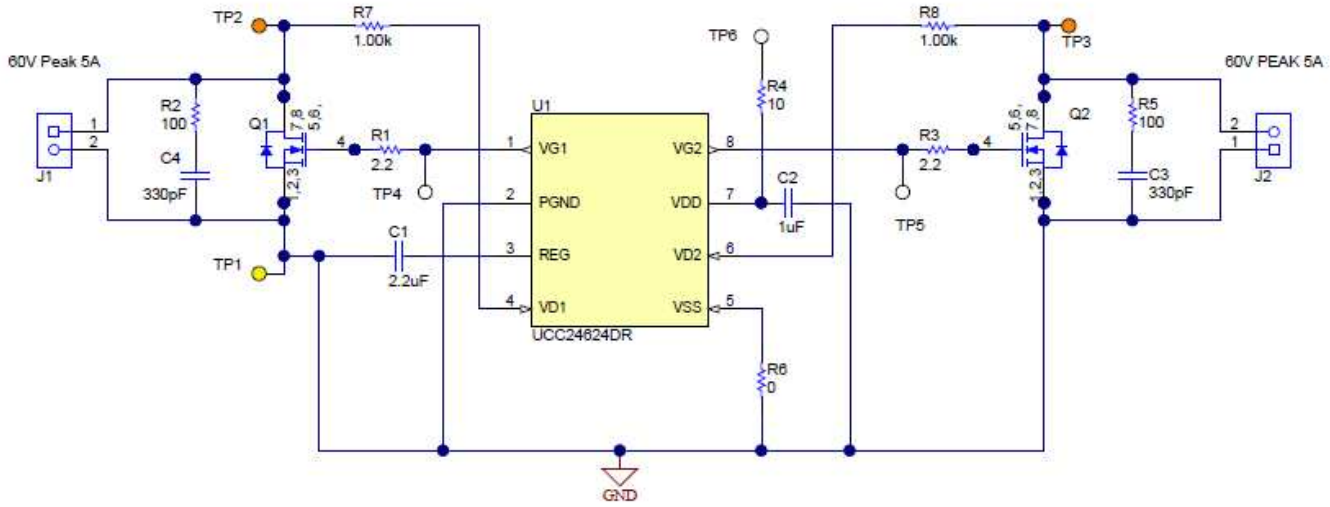

Figure 3. UCC24624EVM-015 Schematic

5 Test Point and Terminal Block

a. Terminal blocks J1 and J2 are used to connect the SR FETs to the LLC rectifier return paths in place of rectifier diodes.
b. Test point 1 (TP1) is used for sensing the evaluation modules ground (GND).
c. Test Point 2 (TP2) is for Q1 drain sensing/probing/connecting.
d. Test Point 3 (TP3) is for Q2 drain sensing/probing/connecting.
e. Test Point 4 (TP4) is for sensing/probing/evaluating Q1's gate drive (VG1).
f. Test Point 5 (TP5) is for sensing/probing/evaluating Q2's gate drive (VG2).
g. Test Point 6 (TP6) is connected to the LLC output to provide power to the EVM.

6 Specifications

Table 1. UCC24624EVM-015 Test Points

CONNECTIONS	MAX
TP2(+) to TP1(-), TP3(+) to TP1(-)	60 V
TP6(+) to TP1(-)	26 V
TP2(+) to TP1(-), TP3(+) to TP1(-)	7.85-A RMS

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7 EVM Used in a Low-Side LLC SR Application

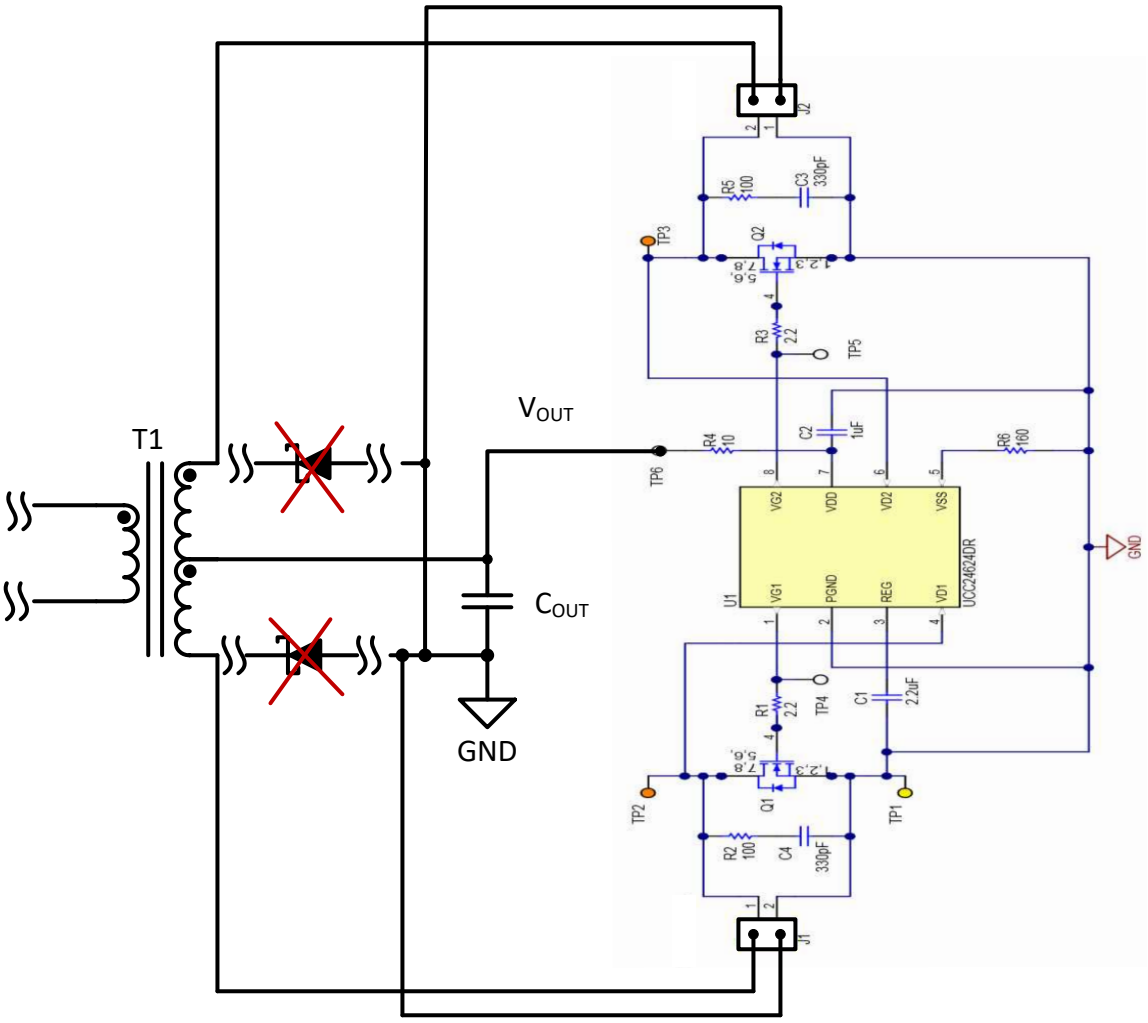

Figure 4. UCC24624EVM-015 Used in LLC Power Converter

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8 RC Snubber Setup for C3, C4, R2, and R5

It may be required to adjust snubbing components C3, C4, R2 and R5 to dampen noise.

To adjust these components will require knowing the LLC transformers secondary leakage inductance (Lslk) and measuring the secondary resonant ring frequency (fr) in circuit at minimal load of 10% or less. It also recommended that the SR is not engaged while doing this and capacitors C3 and C4 are removed from the evaluation module. TP6 should be connected to ground to disable the gate driver.

The secondary winding capacitance (Cs) then needs to be calculated based on the following equation. Please note for a transformer with a secondary winding leakage inductance of 3.8 uH and a ring frequency of 2 MHz, the parasitic capacitance would be 1.7 nF.

$$Cs = \frac{1}{(2 \times \pi \times f_r)^2 \times Lslk} = \frac{1}{(2 \times \pi \times 2MHz)^2 \times 3.8\mu H} = 1.7nF \quad (1)$$

Based on the calculated Cs, Lslk and fr the snubber resistors R2 and R5 can be set to critically dampen the ringing on the secondary, which requires setting the Q of the circuit equal to 1.

$$R2 = R5 = \frac{1}{Q}\sqrt{\frac{Lslk}{Cs}} = \frac{1}{1}\sqrt{\frac{3.8\mu H}{1.7nF}} \approx 47\ \Omega \quad (2)$$

Capacitors C3 and C5 are used to limit the time the snubber resistor is applied to the aux winding during the switching cycle. It is recommended to set the snubber capacitor C3 with the following equation based on the LLC converters minimum switching frequency (f_{SW}). For an LLC converter with a minimum switching at 85 kHz in the example would require a C3 and C4 would be roughly 497 pF.

$$C3 = C4 = \frac{0.01}{5 \times fsw \times R3} = \frac{0.01}{5 \times 85kHz \times 47.3\Omega} \approx 497pF \quad (3)$$

Please note that the calculations for R2, R5, C3 and C4 are just starting points and should be adjusted based on individual preference, performance and efficiency requirements.

9 Application Test Data

The UCC24624EVM-015 was used to replace rectifier diodes in a 120 W LLC power converter using the UCC256302 LLC controller. The power converter had an input voltage (V_{IN}) range of 340-V to 410-V with a typical input of 390-V, with a regulated 12V output.

9.1 Steady State

- CH1 = VG1(TP4), CH3 = Q1 drain (TP2), CH2 = VG2(TP5), CH4 = Q1 drain (TP3)

Figure 5. V_{IN} = 340 V, I_{OUT} = 0 A, No Gate Drive Under Light Load (VG1, VG2)

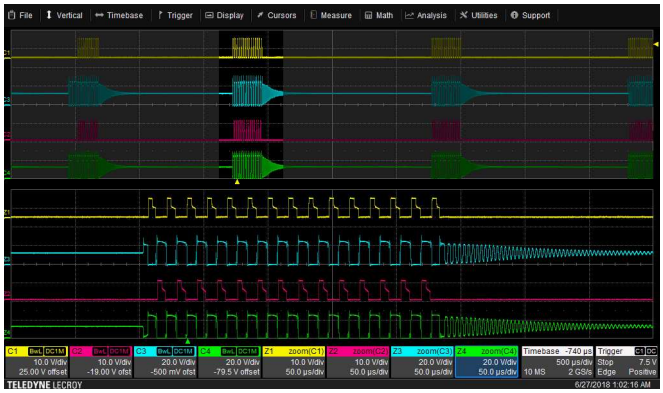

Figure 6. V_{IN} = 340 V, I_{OUT} = 0.3 A, LLC is Operating In Burst Mode

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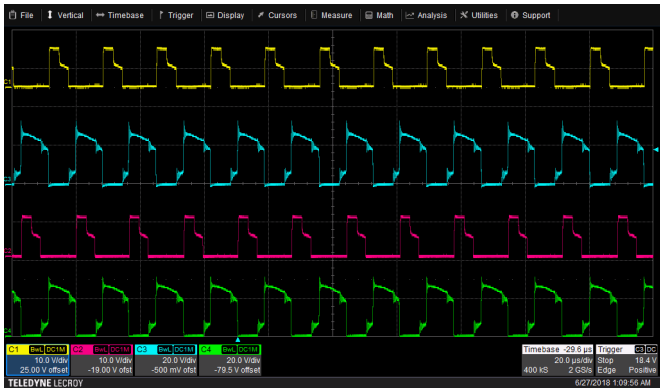

Figure 7. V_{IN} = 340 V, I_{OUT} = 10 A Full Load

Figure 8. V_{IN} = 390 V, I_{OUT} = 0 A, No Gate Drive Under Light Load (VG1, VG2)

Figure 9. V_{IN} = 390 V, I_{OUT} = 0.3 A, LLC is Operating In Burst Mode

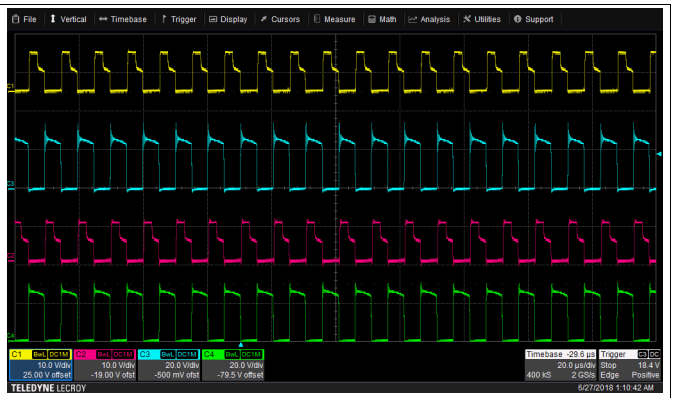

Figure 10. V_{IN} = 390 V, I_{OUT} = 10 A Full Load

Figure 11. V_{IN} = 410 V, I_{OUT} = 0 A, No Gate Drive Under Light Load (VG1, VG2)

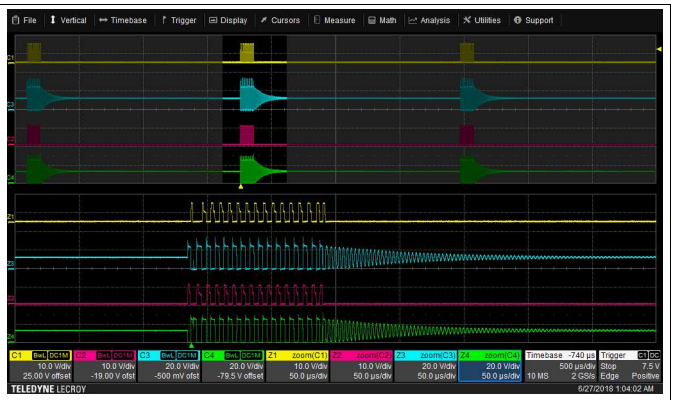

Figure 12. V_{IN} = 410 V, I_{OUT} = 0.3 A, LLC is Operating In Burst Mode

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Figure 13. V_{IN} = 410 V, I_{OUT} = 10 A Full Load

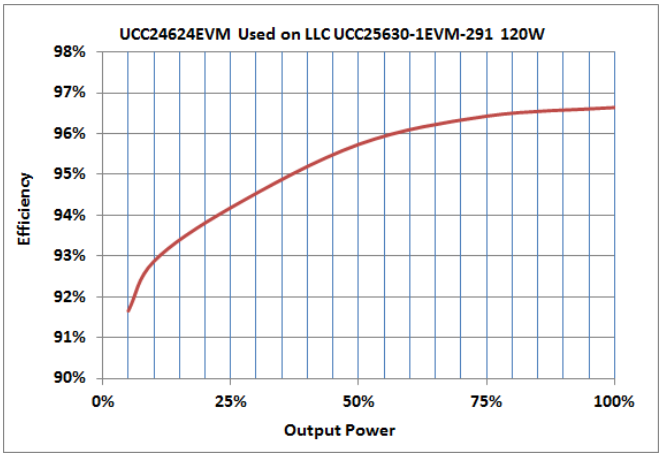

Figure 14. V_{IN} = 390 V, Power Converter System Efficiency Using SR FETs

10 EVM Layout

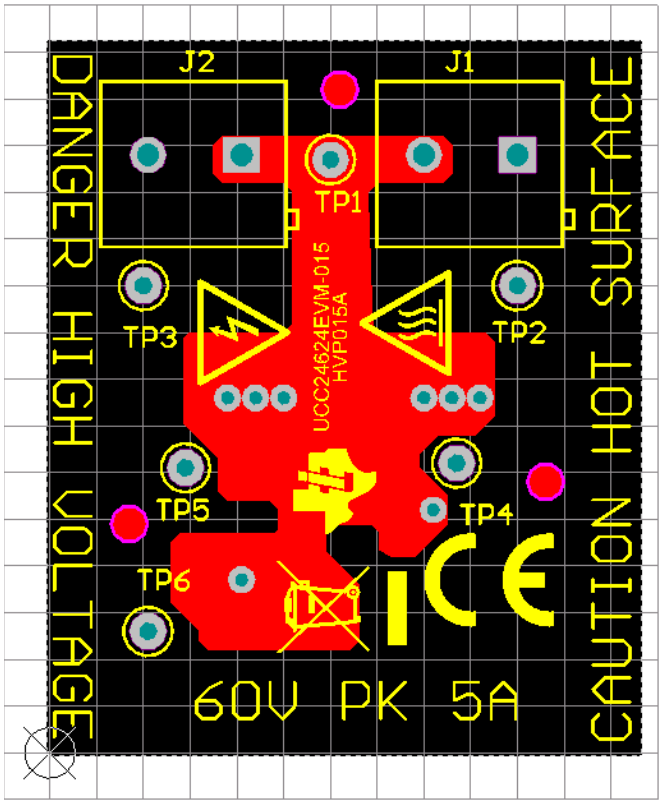

Figure 15. Layout Top

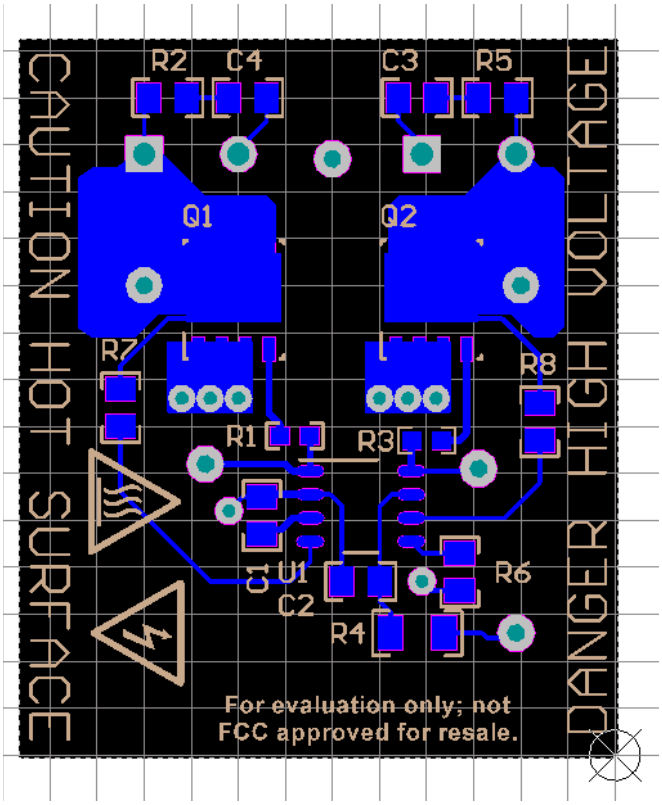

Figure 16. Layout Bottom

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11 List of Materials

UCC24624EVM-015 list of materials as shown in Figure 1.

Table 2. UCC24624EVM-015 List of Materials

QTY	REF	DESCRIPTION	PART NUMBER	Manufacturer
1	C1	Capacitor, ceramic 2.2 µF, 50 V, ±20%, X7R, 0805	C2012X7R1H225M125AC	TDK
1	C2	Capacitor, ceramic, 1 µF, 50 V, +±10%, X7R, 0805	08055C105KAT2A	AVX
2	C3, C4	Capacitor, ceramic, 330 pF, 50 V, ±10%, C0G/NP0, 0805	08055A331KAT2A	AVX
2	J1, J2	Terminal block, 5.08 mm, 2 x 1, brass, TH	ED120/2DS	On-Shore Technology
2	Q1, Q2	MOSFET, N-Channel, 60 V, 158 A, PG-TDSON-8	FDMS86500L	On Semiconductor
2	R1, R3	Resistor, 2.2 Ω, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032R20JNEA	Vishay-Dale
2	R2, R5	Resistor, 100 Ω, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW0805100RJNEA	Vishay-Dale
1	R4	Resistor, 10 Ω, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	CRCW120610R0JNEA	Vishay-Dale
1	R6	Resistor, 0, 5%, 0.125 W, 0805	ERJ-6GEY0R00V	Panasonic
2	R7, R8	Resistor, 1.00 k, 1%, 0.125 W, 0805	CRCW08051K00FKEA	Vishay-Dale
1	TP1	Test point, miniature, yellow, TH	5004	Keystone
2	TP2, TP3	Test point, miniature, orange, TH	5003	Keystone
3	TP4, TP5, TP6	Test point, miniature, white, TH	5002	Keystone
1	U1	High Performance Synchronous Rectifier Driver for LLC Resonant Converter, D0008A (SOIC-8)	UCC24624DR	Texas Instruments

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2018) to A Revision **Page**

- Changed Figure 1 3
- Changed Figure 2 3
- Changed Figure 3 4
- Updated Table 2 9

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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