User's Guide

TPSM843620 SWIFT™ Step-Down Evaluation Module

ABSTRACT

This user's guide contains information for the TPSM843620EVM evaluation module (BSR214) and the TPSM843620 DC/DC Converter. Also included are the performance characteristics, schematic, and bill of materials for the TPSM843620EVM.

Table of Contents

1 Introduction ... 3
- 1.1 Background ... 3
- 1.2 Before You Begin ... 3
- 1.3 Performance Characteristics Summary ... 4

2 Configurations and Modifications ... 5
- 2.1 Output Voltage ... 5
- 2.2 Switching Frequency (SYNC/FSEL Pin) ... 6
- 2.3 Current Limit, Soft-Start Time, and Internal Compensation (MODE Pin) ... 6
- 2.4 Adjustable UVLO ... 6

3 Test Setup and Results ... 7
- 3.1 Input/Output Connections ... 7
- 3.2 BOM Modifications for Spins ... 8
- 3.3 Efficiency ... 9
- 3.4 Output Voltage Regulation ... 11
- 3.5 Load Transient and Loop Response ... 12
- 3.6 Output Voltage Ripple ... 13
- 3.7 Input Voltage Ripple ... 14
- 3.8 Start-up and Shutdown with EN ... 15
- 3.9 Start-up and Shutdown with VIN ... 16
- 3.10 Start-up Into Pre-Bias ... 17
- 3.11 Thermal Performance ... 18

4 Board Layout ... 19
- 4.1 Layout ... 19

5 Schematic and Bill of Materials ... 20
- 5.1 Schematic ... 21
- 5.2 Bill of Materials ... 22

List of Figures

Figure 3-1. U1 Efficiency - Default Configuration ... 9
Figure 3-2. U1 Efficiency – 1000-kHz Switching Frequency with Different Output Voltages ... 9
Figure 3-3. U1 Efficiency – 1-V Output with Different Switching Frequencies ... 9
Figure 3-4. U1 Efficiency – 1-V Output and 1500-kHz Switching Frequency with Different Input Voltages ... 9
Figure 3-5. U1 Efficiency – 1.8-V Output with Different Switching Frequencies ... 10
Figure 3-6. U1 Load Regulation ... 11
Figure 3-7. U1 Line Regulation ... 11
Figure 3-8. U1 Transient Response ... 12
Figure 3-9. U1 Bode Plot ... 12
Figure 3-10. U1 Loop Gain with Different Ramp Settings ... 12
Figure 3-11. U1 Loop Phase with Different Ramp Settings ... 12
Figure 3-12. U1 Output Ripple – No Load ... 13
Figure 3-13. U1 Output Ripple – 6-A Load ... 13
Figure 3-14. U1 Input Ripple – No Load ... 14
Figure 3-15. U1 Input Ripple – 6-A Load ... 14

Figure 3-16. U1 Start-Up with EN – No Load 15
Figure 3-17. U1 Shutdown with EN – No Load 15
Figure 3-18. U1 Start-up with EN - 6-A Load 15
Figure 3-19. U1 Start-up with VIN – No Load 16
Figure 3-20. U1 Shutdown with VIN – 6-A Load 16
Figure 3-21. U1 Start-up Into 0.5-V Pre-Bias 17
Figure 3-22. U1 Thermal Performance – 6-A Load 18
Figure 4-1. Top-Side Composite View 19
Figure 4-2. Bottom-Side Composite View (Viewed From Bottom) 19
Figure 4-3. Top Layer Layout 20
Figure 4-4. Mid Layer 1 Layout 20
Figure 4-5. Mid Layer 2 Layout 20
Figure 4-6. Bottom Layer Layout 20
Figure 5-1. U1 Schematic 21

List of Tables

Table 1-1. Input Voltage and Output Current Summary 3
Table 1-2. TPSM843620EVM Performance Characteristics Summary 4
Table 2-1. VOUT Selection 5
Table 2-2. SYNC/FSEL Selection 6
Table 2-3. MODE Selection 6
Table 3-1. Connectors and Jumpers 7
Table 3-2. Test Points 8
Table 3-3. BOM Modifications 8
Table 3-4. Efficiency Measurement Test Points 9
Table 5-1. TPSM843620EVM Bill of Materials 22

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1 Introduction

1.1 Background

The TPSM843620 DC/DC converter is a synchronous buck module designed to provide up to a 6-A output. The input (VIN) is rated for 4 V to 18 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1.

The high-side and low-side MOSFETs are incorporated inside the TPSM843620 package along with the gate-drive circuitry, inductor and basic passives which achieves better power density with this integration. The low drain-to-source on-resistance of the MOSFET allows the TPSM843620 to achieve high efficiencies and helps keep the junction temperature low at the rated output current. Fixed frequency advanced current mode control allows you to synchronize the regulators to an external clock source. An external divider allows for an adjustable output voltage. The TPSM843620 FSEL and MODE pins provide selectable switching frequency, soft start time, current limit, and internal compensation. Lastly, the TPSM843620 includes an enable pin and a power good output which can be used for sequencing multiple regulators.

This evaluation module is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPSM843620 module. The small area design fits within 115 mm^2. The design also includes jumpers that can be used to easily evaluate the features of the TPSM843620.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPSM843620EVM	V_{IN} = 4 V to 18 V	0 A to 6 A

1.2 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPSM843620EVM. Observe all safety precautions.

Warning The TPSM843620EVM can become hot during operation due to dissipation of power in some operating conditions. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This can result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

1.3 Performance Characteristics Summary

A summary of the TPSM843620EVM performance characteristics is provided in Table 1-2. The TPSM843620EVM is designed and tested for V_{IN} = 4 V to 18 V. Characteristics are given for an input voltage of V_{IN} = 12 V and an output voltage of 1 V, unless otherwise specified. The ambient temperature is room temperature (20°C to 25°C) for all measurements, unless otherwise noted.

Table 1-2. TPSM843620EVM Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} voltage range		4	12	18	V
Input current	V_{IN} = 12 V, I_O = 0 A		15		mA
	V_{IN} = 5 V, I_O = 6 A		1.46		A
V_{IN} start voltage	Set by EN pin resistor divider		4.53		V
V_{IN} stop voltage	Set by EN pin resistor divider		3.98		V
Output voltage setpoint			1.00		V
Output current range	V_{IN} = 4 V to 18 V	0		6	A
Line and load regulation	V_{IN} = 4 V to 18 V, I_O = 0 A to 6 A		±0.1%		
Loop bandwidth	I_O = 6 A, J4 short pins 3 and 4		140		kHz
Phase margin			53		degrees
Input ripple voltage	I_O = 6 A		75		mVPP
Output ripple voltage	I_O = 6 A		10		mVPP
Output rise time	Set by MODE pin resistor, All default J4 options		1		ms
Current limit	Set by MODE pin resistor, J4 short pins 1 and 2, 3 and 4, or 5 and 6		High		
Switching frequency (f_{SW})	Set by FSEL pin resistor, J5 short pins 5 and 6		1000		kHz
Peak efficiency	V_{IN} = 5 V, I_O = 2 A		89.4%		
	V_{IN} = 12 V, I_O = 2.75 A		85.2%		
IC case temperature	V_{IN} = 12 V, I_O = 6 A, 10-minute soak		70.2		°C

2 Configurations and Modifications

These evaluation modules are designed to provide access to the features of the TPSM843620. The design provides jumpers for testing different configurations. Jumper selections must be made prior to enabling the TPSM843620.

If a desired configuration is not available, then some modifications can be made to this module. When modifications are made to the components on the EVM, there is a possibility that the internal compensation option selected with the MODE pin resistor needs to be changed. Changes to the f_{SW}, output voltage, and output capacitors can require a change in the compensation. TPSM843620 data sheet equations or WEBENCH can be used to calculate the output capacitor value, compensation, and f_{SW}. Make sure all components have sufficient voltage and current ratings.

2.1 Output Voltage

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

The TPSM843620EVM comes with fixed 10 kΩ R_{FBT} and R_{FBB} for an output voltage of 1 V. However, the output voltage can still be changed by changing the feedback resistor values. The resistor values can be changed according to this table for certain output voltage options in Table 2-1. If the desired output voltage is not available, a resistor must be changed and the required value for can be calculated with Equation 2.

$$R_{FBB} = R_{FBT} \times \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad (2)$$

Table 2-1. VOUT Selection

TOP FB RESISTOR (R_{FBT})	BOTTOM FB RESISTOR (R_{FBB})	NOMINAL OUTPUT VOLTAGE
R3 = 10 kΩ	R9 = 16.66 kΩ	0.800 V
R3= 10 kΩ (1)	R9 = 10.00 kΩ	1.000 V
R3 = 10 kΩ	R9 = 7.14 kΩ	1.200 V
R3 = 10 kΩ	R9 = 5.00 kΩ	1.500 V
R3 = 10 kΩ	R9 = 3.84 kΩ	1.802 V
R3 = 10 kΩ	R9 = 1.78 kΩ	3.309V

(1) Default Setting

2.2 Switching Frequency (SYNC/FSEL Pin)

Jumper J5 can be used to select between the switching frequency options shown in Table 2-2.

Table 2-2. SYNC/FSEL Selection

JUMPER SETTING	SYNC/FSEL RESISTOR	SWITCHING FREQUENCY
1 to 2 pin shorted	24.3 kΩ	500 kHz
3 to 4 pin shorted	17.4 kΩ	750 kHz
5 to 6 pin shorted(1)	11.8 kΩ	1000 kHz
7 to 8 pin shorted	8.06 kΩ	1500 kHz
9 to 10 pin shorted	4.99 kΩ	2200 kHz

(1) Default Setting

2.3 Current Limit, Soft-Start Time, and Internal Compensation (MODE Pin)

Jumper J4 can be used to select between the current limit, soft-start time, and internal compensation options shown in Table 2-3. If the desired option is not available, change one of the resistors to the value which sets the desired option.

Table 2-3. MODE Selection

JUMPER SETTING	MODE RESISTOR	CURRENT LIMIT	SOFT-START TIME	RAMP
1 to 2 pin shorted	2.21 kΩ	High	1 ms	1 pF
3 to 4 pin shorted(1)	4.87 kΩ	High	1 ms	2 pF
5 to 6 pin shorted	11.3 kΩ	High	1 ms	4 pF
7 to 8 pin shorted	60.4 kΩ	Low	1 ms	2 pF

(1) Default Setting

2.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R7 (R_{ENT}) and R11 (R_{ENB}). See the TPSM843620 data sheet for detailed instructions for setting the external UVLO.

3 Test Setup and Results

This section describes how to properly connect, set up, and use the TPSM843620EVM. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start-up, and current limit modes. Measurements are taken with the following conditions unless otherwise noted.

- 12-V input
- Room temperature (20°C to 25°C)
- The default setting output voltage of 1 V, switching frequency of 1000 kHz, and maximum current limit setting

3.1 Input/Output Connections

The TPSM843620EVM is provided with input connectors, output connectors, and test points as shown in Table 3-1 and Table 3-2.

To support the minimum input voltage with the full rated load on both outputs with the default EVM, a power supply capable of supplying greater than 5 A must be connected to J2 through a pair of 20-AWG wires or better.

For U1 the load must be connected to J1. A pair of 20-AWG wires or better must be used for each connection. With the maximum current limit setting, the maximum load current capability is near 8 A before the TPSM843620 goes into current limit. Wire lengths must be minimized to reduce losses in the wires.

TP3 provides a place to monitor the V_{IN} input voltage with TP4 providing a convenient ground reference. TP9 is used to monitor the output voltage of U1 with TP10 as the ground reference.

If modifications are made to the TPSM843620EVM, then the input current can change. The input power supply and wires connecting the EVM to the power supply must be rated for the input current.

Note

For the FSEL pin of the TPSM843x20 to correctly detect the resistor value connected to ground, the buffers on the EVM need to be provided a VCC voltage of 2 V to 5.5 V to go high impedance. Populating the shunt on J3 enables the output of the buffer.

Table 3-1. Connectors and Jumpers

REFERENCE DESIGNATOR	NAME	FUNCTION
J1	VOUT	VOUT screw terminal to connect load to output.
J2	VIN	VIN screw terminal to connect power to input.
J3	EXT SYNC	2-pin header to connect U2 buffer output enable to ground. Populate shunt to enable output of buffer. Remove shunt to make buffer output high impedance.
J4	MODE	MODE selection header. Use shunt to select MODE resistor. See Table 2-3.
J5	SYNC/FSEL	FSEL selection header. Use shunt to select FSEL resistor. See Table 2-2.

Table 3-2. Test Points

REFERENCE DESIGNATOR	NAME	FUNCTION
TP1	VIN	VIN test point. Use this for input ripple measurements.
TP2	PGND	PGND test point. Use this for input ripple measurements.
TP3	VIN_EFF	VIN test point near input terminals. Use this for efficiency measurements.
TP4	PGND_EFF	PGND test point near input terminals. Use this for efficiency measurements.
TP5	PGOOD	PGOOD test point.
TP6	AGND	AGND test point.
TP7	VOUT	VOUT test point. Use this for output ripple measurements.
TP8	PGND	PGND test point. Use this for output ripple measurements.
TP9	VOUT_EFF	VOUT test point near output terminals. Use this for efficiency measurements.
TP10	PGND_EFF	PGND test point near output terminals. Use this for efficiency measurements.
TP11	EN	EN test point. If applying an external voltage, then EN must be kept below the absolute maximum voltage of the EN pin of 6 V.
TP12	VOUT	meSMB connector to measure output voltage. When using this test point, make sure the scope is set for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP13	EXT_SYNC	SYNC test point. Supply an external clock to this test point if using one.
TP14	SYNC/FSEL	FSEL test point.
TP15	MODE	MODE test point.
TP16	BODE	Test point between voltage divider network and output voltage. Used for Bode plot measurements.

3.2 BOM Modifications for Spins

The TPSM843620EVM is designed to be used for evaluation of the TPSM843620, TPSM843820, and TPSM843320. Here are recommended BOM changes to be made to the evaluation module for the best performance of each device.

Table 3-3. BOM Modifications

COMPONENT	REFERENCE DESIGNATOR	TPSM843620 (6 A)(1)	TPSM843820 (8 A)	TPSM843320 (3 A)
MODULE	U1	TPSM843620	TPSM843820	TPSM843320
CFF	C9	100 pF	42 pF	100 pF
MODE	J4	Short pins 3-4 (4.87 kΩ)	Short pins 3-4 (4.87 kΩ)	Short pins 5-6 (11.3 kΩ)
FSEL	J5	Short pins 5-6 (11.8 kΩ = 1000 kHz)	Short pins 7-8 (8.06 kΩ = 1500 kHz)	Short pins 5-6 (11.8 kΩ = 1000 kHz)

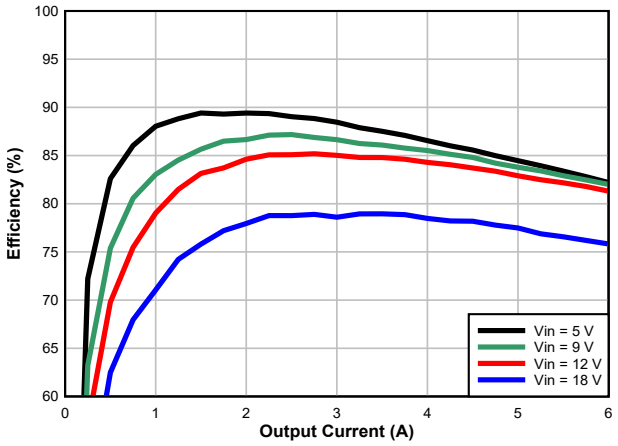
(1) Default Setting

3.3 Efficiency

Figure 3-1 through Figure 3-5 show the efficiency for the TPSM843620EVM. Using the selection jumpers for U1, the results for different output voltage and switching frequency combinations are included. The test points listed in Table 3-4 are used for efficiency measurements. Use these test points to minimize the contribution of PCB parasitic power loss to the measured power loss.

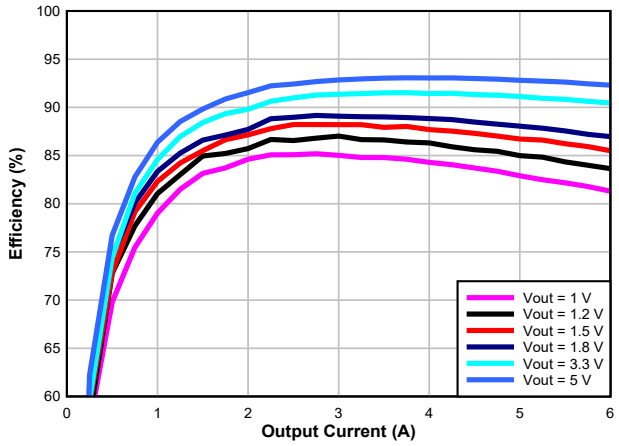
Table 3-4. Efficiency Measurement Test Points

TEST POINT NAME	REFERENCE DESIGNATOR	FUNCTION
VIN_EFF	TP3	Input voltage test point.
PGND_EFF	TP4	Input ground test point.
VOUT_EFF	TP9	Output voltage test point.
PGND_EFF	TP10	Output ground test point.



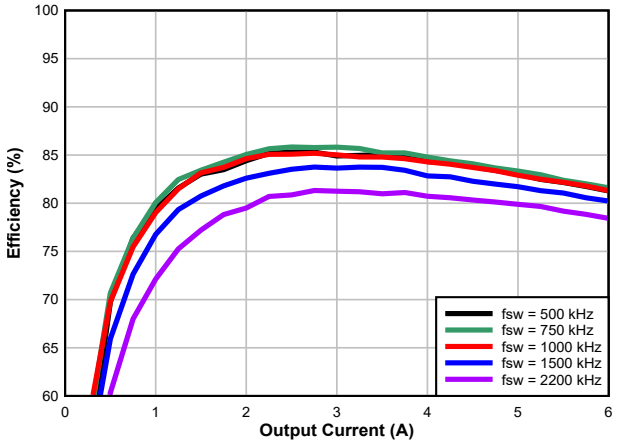
V_{OUT} = 1 V f_{SW} = 1000 kHz

Figure 3-1. U1 Efficiency - Default Configuration



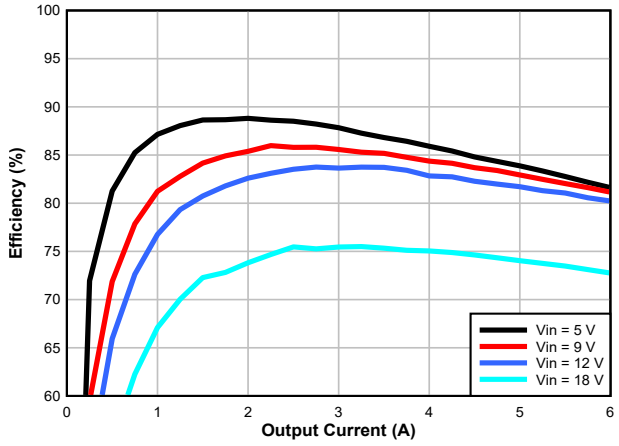
V_{IN} = 12 V f_{SW} = 1000 kHz

Figure 3-2. U1 Efficiency – 1000-kHz Switching Frequency with Different Output Voltages



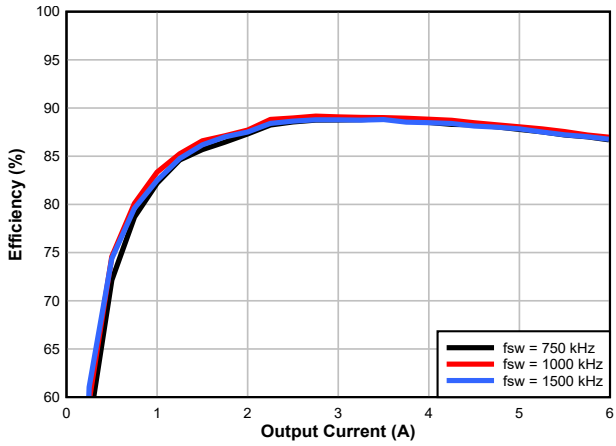
V_{IN} = 12 V V_{OUT} = 1 V

Figure 3-3. U1 Efficiency – 1-V Output with Different Switching Frequencies



V_{OUT} = 1 V f_{SW} = 1500 kHz

Figure 3-4. U1 Efficiency – 1-V Output and 1500-kHz Switching Frequency with Different Input Voltages



V_{IN} = 12 V V_{OUT} = 1.8 V

Figure 3-5. U1 Efficiency – 1.8-V Output with Different Switching Frequencies

3.4 Output Voltage Regulation

Figure 3-6 and Figure 3-7 show the load and line regulation for the TPSM843620.

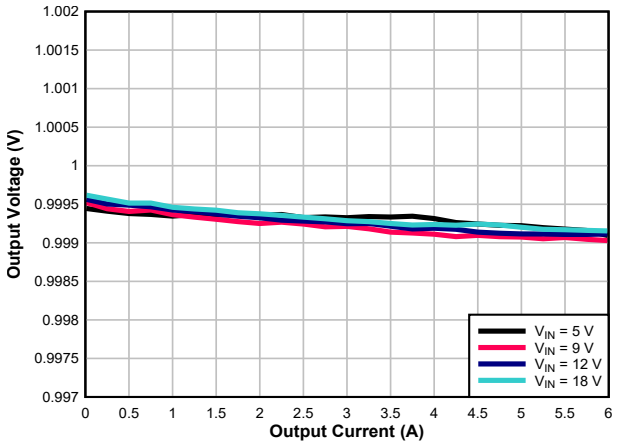


Figure 3-6. U1 Load Regulation

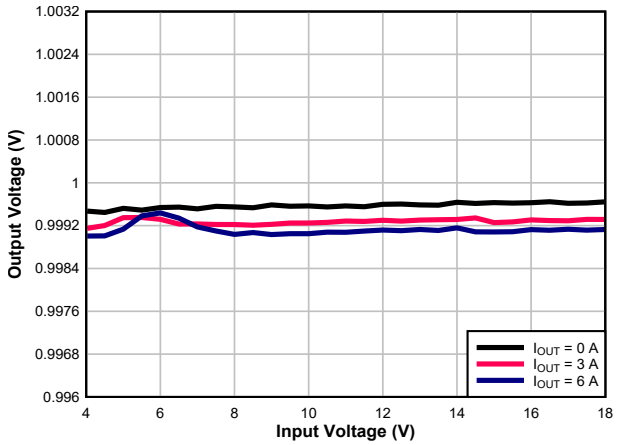


Figure 3-7. U1 Line Regulation

3.5 Load Transient and Loop Response

Figure 3-8 shows the load transient response for the TPSM843620EVM. The current step is from 0 A to 3 A and the current step slew rate is 1 A/µs. An electronic load is used to provide a 3-A step. The VOUT voltage is measured using SMB connector TP12.

Figure 3-9 shows the loop response. Gain and phase plots are shown for V_{IN} voltage of 12 V and a 6-A load.

Figure 3-10 shows the loop gain characteristics with 3 different ramp settings.

Figure 3-11 shows the loop phase characteristics with 3 different ramp settings.

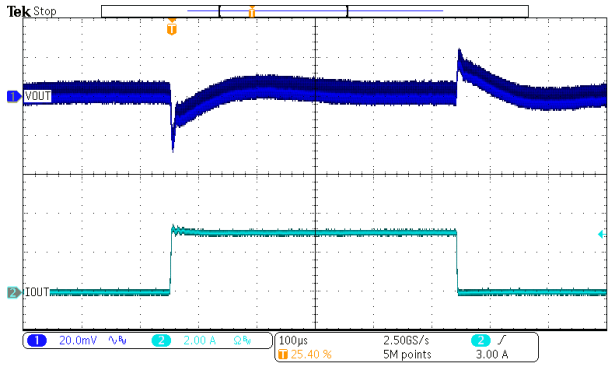


Figure 3-8. U1 Transient Response

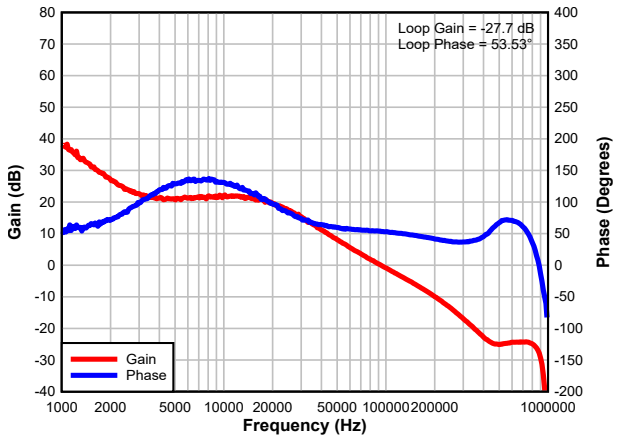


Figure 3-9. U1 Bode Plot

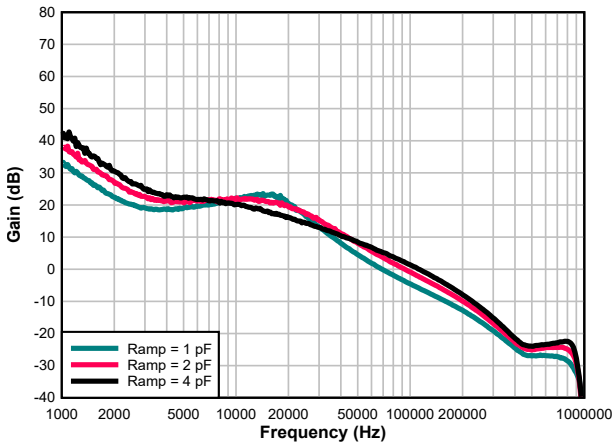


Figure 3-10. U1 Loop Gain with Different Ramp Settings

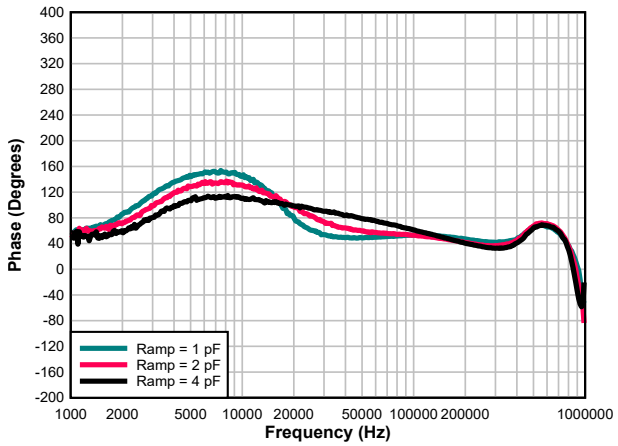


Figure 3-11. U1 Loop Phase with Different Ramp Settings

3.6 Output Voltage Ripple

Figure 3-12 through Figure 3-13 show the TPSM843620EVM output voltage ripple. The load currents are no load and 6 A. V_{IN} = 12 V. The VOUT voltage is measured using TP12, but TP7 and TP8 can also be used.

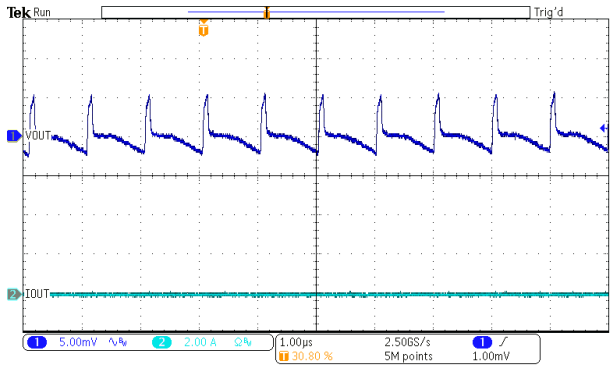


Figure 3-12. U1 Output Ripple – No Load

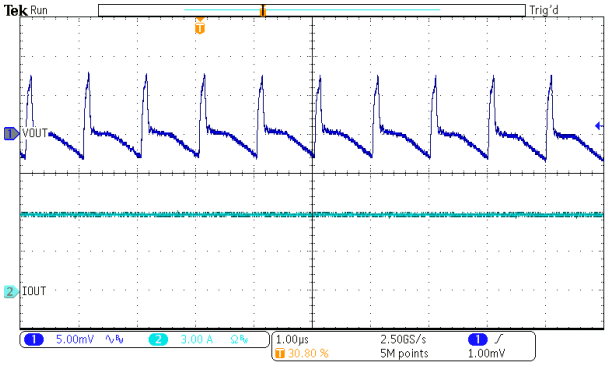


Figure 3-13. U1 Output Ripple – 6-A Load

3.7 Input Voltage Ripple

Figure 3-14 through Figure 3-15 show the TPSM843620EVM input voltage ripple. The load currents are no load and 6 A. V_{IN} = 12 V. The ripple voltage is measured across input capacitor C2.

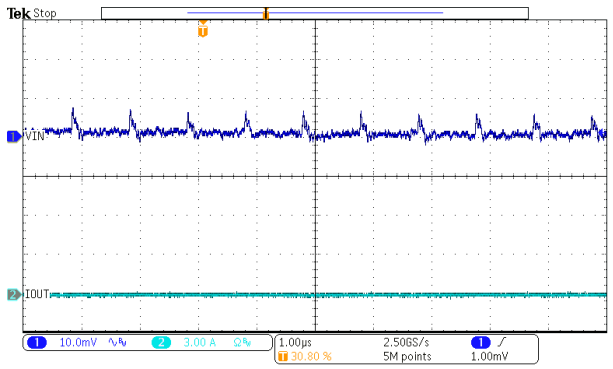


Figure 3-14. U1 Input Ripple – No Load

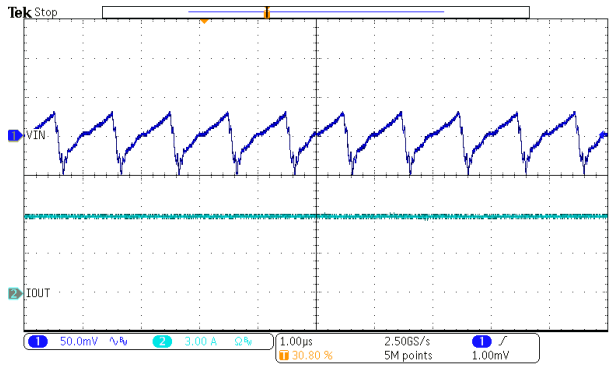


Figure 3-15. U1 Input Ripple – 6-A Load

3.8 Start-up and Shutdown with EN

Figure 3-16 and Figure 3-17 show the start-up and shutdown waveforms using EN. In Figure 3-16, the input voltage is initially applied and the output is inhibited by pulling EN to GND. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value. Figure 3-17 shows EN shutdown with no load.

Figure 3-18 shows EN start-up with a 6-A load.

TP11 for EN can be used to test the EN start-up. EN is high if there is power, and is low if tied to AGND.

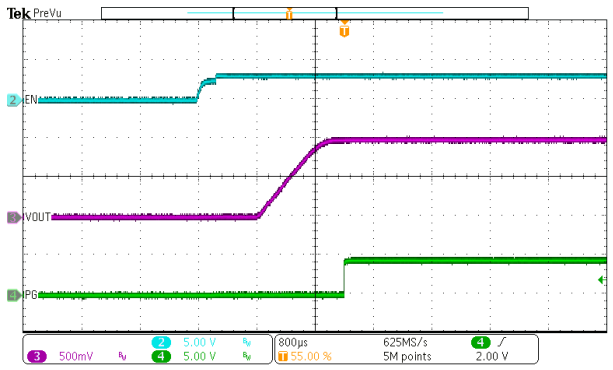


Figure 3-16. U1 Start-Up with EN – No Load

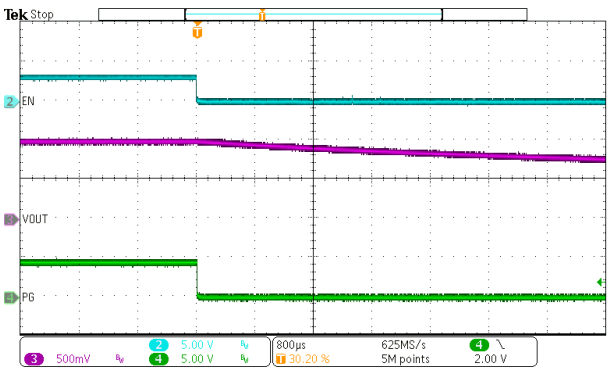


Figure 3-17. U1 Shutdown with EN – No Load

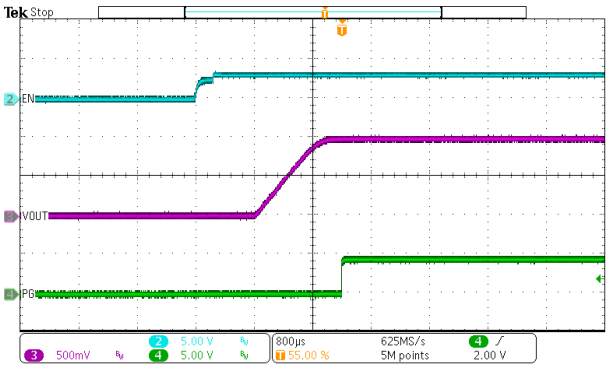


Figure 3-18. U1 Start-up with EN - 6-A Load

3.9 Start-up and Shutdown with VIN

Figure 3-19 and Figure 3-20 show the start-up and shutdown waveforms with VIN. In Figure 3-19, the VIN voltage ramps up and output voltage ramps up after the input and EN pin voltages reach their respective UVLO threshold. In Figure 3-20, the VIN voltage ramps down and the TPSM843620 shuts down when the input or EN pin voltage reach their respective UVLO threshold. The rate at which VIN ramps down changes as soon as the TPSM843620 is disabled because the device is no longer loading the input supply.

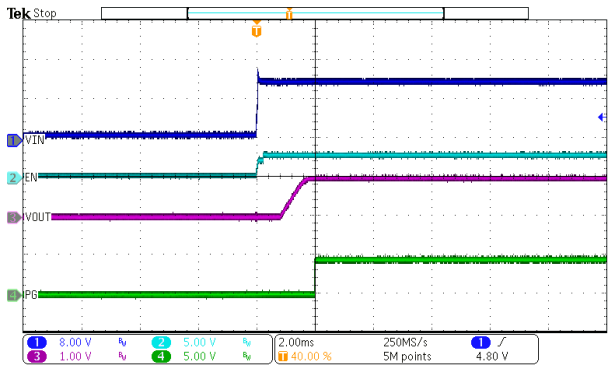


Figure 3-19. U1 Start-up with VIN – No Load

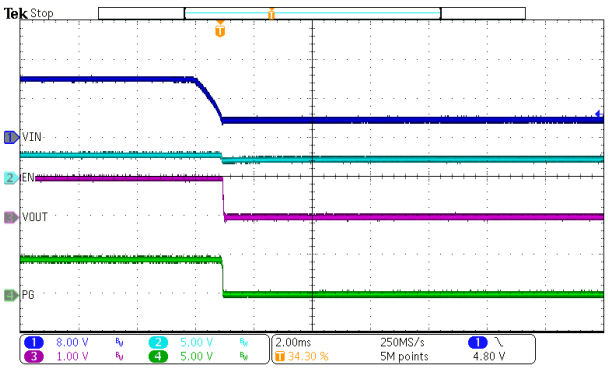


Figure 3-20. U1 Shutdown with VIN – 6-A Load

3.10 Start-up Into Pre-Bias

Figure 3-21 shows the EN start-up of U1 into a pre-biased output. The output voltage is pre-biased by toggling the EN pin low then high at a rate such that the output voltage does not fully discharge before EN goes high again.

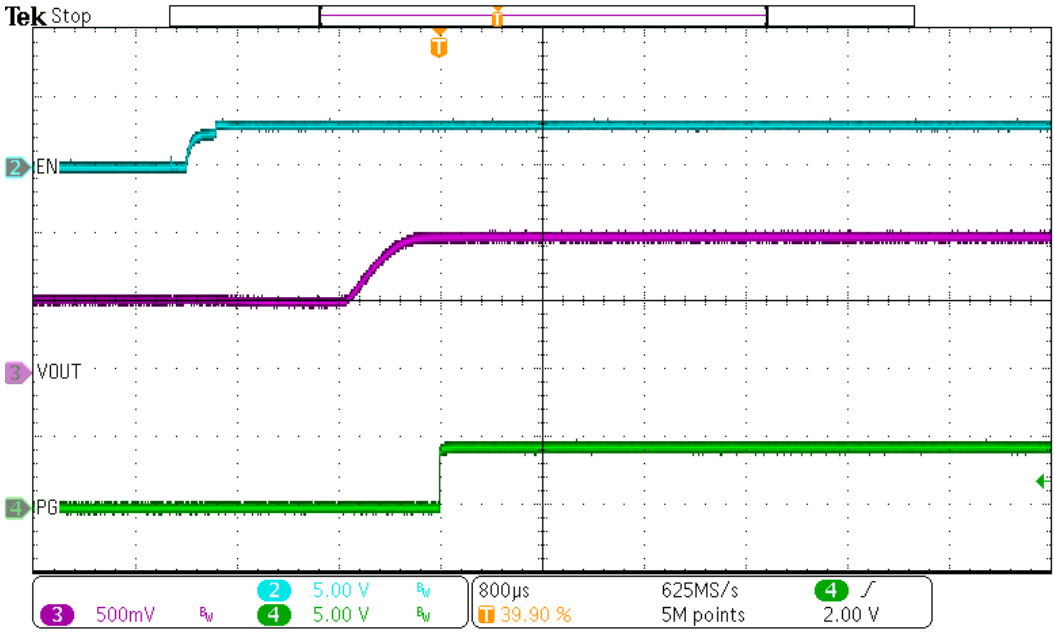


Figure 3-21. U1 Start-up Into 0.5-V Pre-Bias

3.11 Thermal Performance

Figure 3-22 shows the temperature rise of the TPSM843620 IC at full 6-A load. A minimum of a 10 minute soak time was used before taking each measurement.

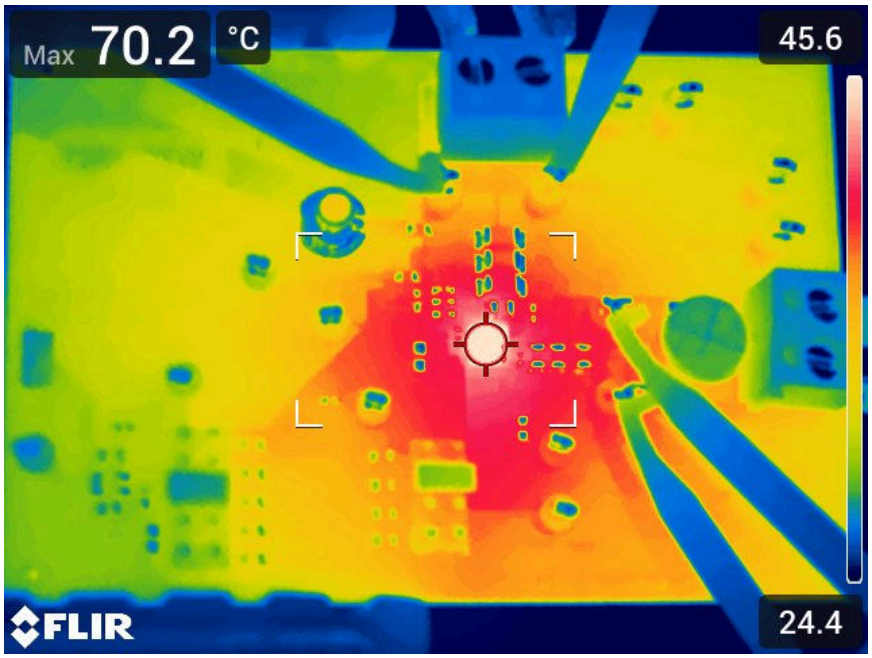


Figure 3-22. U1 Thermal Performance – 6-A Load

4 Board Layout

This section provides a description of the TPSM843620EVM board layout and layer illustrations.

4.1 Layout

The board layout for the TPSM843620EVM is shown in Figure 4-1 through Figure 4-6. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper. The small size circuit takes up an area of only approximately 115 mm^2 as shown on the silkscreen.

All of the required components for the TPSM843620 are placed on the top layer. The input decoupling capacitors, BP5 capacitor, and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. An additional input bulk capacitor is used near the input terminal to limit the noise entering the converter from the supply used to power the board. Critical analog circuits such as the voltage set point divider, MODE resistor, EN divider, and FSEL resistor are kept close to the IC and terminated to the quiet analog ground (AGND) island on the top layer.

The top layer contains the main power traces for VIN and VOUT. The top layer power traces are connected to the planes on other layers of the board with multiple vias placed around the board. There are multiple vias near the PGND pins of the IC to help maximize the thermal performance. The TPSM843620 circuit has a dedicated ground for quiet analog ground that is connected to the main power ground plane at a single point. Lastly, the voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} area on the top layer.

The mid layer 1 is a large ground plane with as few traces as possible to minimize cuts in the ground plane. The mid layer 1 is important to minimize cuts in the ground plane near the IC to help with minimize noise and maximize thermal performance.

The mid layer 2 is mainly used as a signal layer. This layer also has the trace to connect the FB divider to the output. There is also a trace for the BP5 signal to be connected to the buffer. Lastly, the remaining area of this layer is filled in with PGND.

The bottom layer is primarily used for another ground plane. This layer also has an additional VOUT copper area.

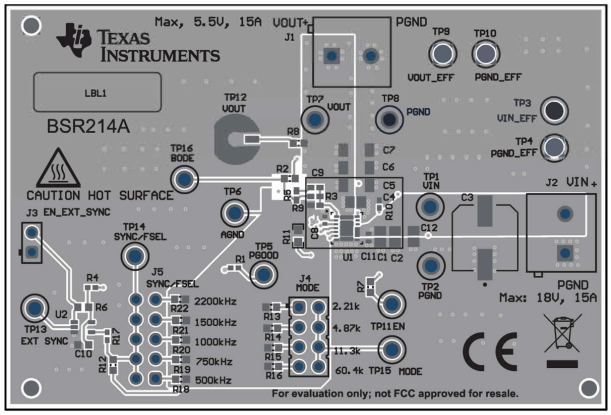


Figure 4-1. Top-Side Composite View

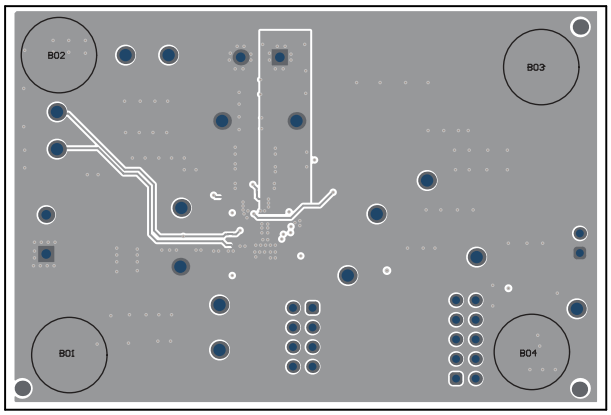


Figure 4-2. Bottom-Side Composite View (Viewed From Bottom)

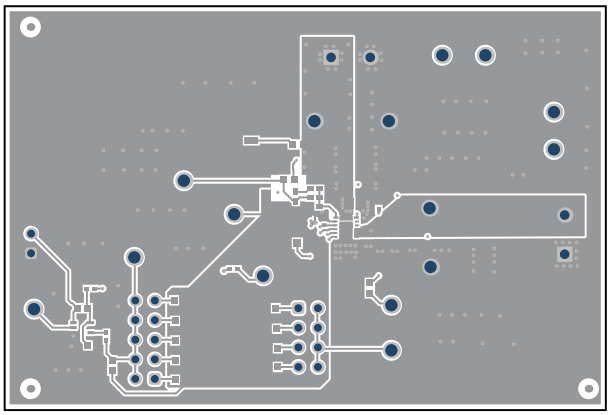


Figure 4-3. Top Layer Layout

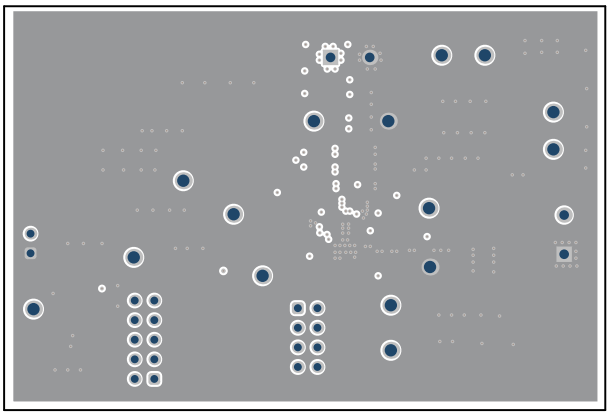


Figure 4-4. Mid Layer 1 Layout

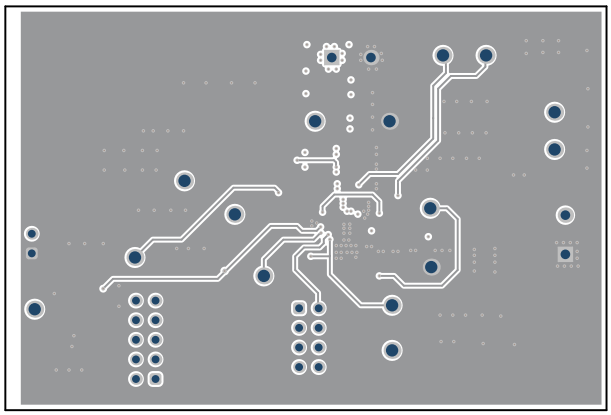


Figure 4-5. Mid Layer 2 Layout

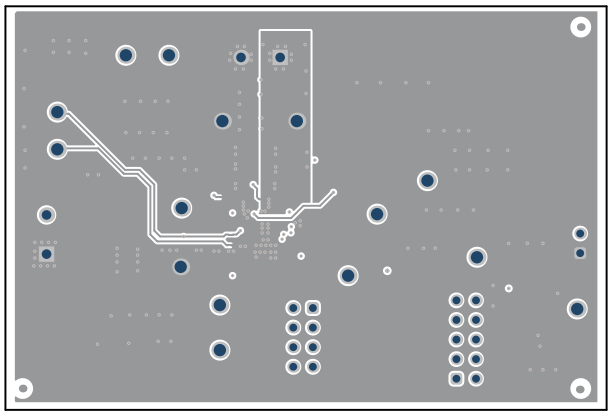


Figure 4-6. Bottom Layer Layout

5 Schematic and Bill of Materials

This section presents the TPSM843620EVM schematic and bill of materials.

5.1 Schematic

Figure 5-1 is the schematic for the TPSM843620EVM.

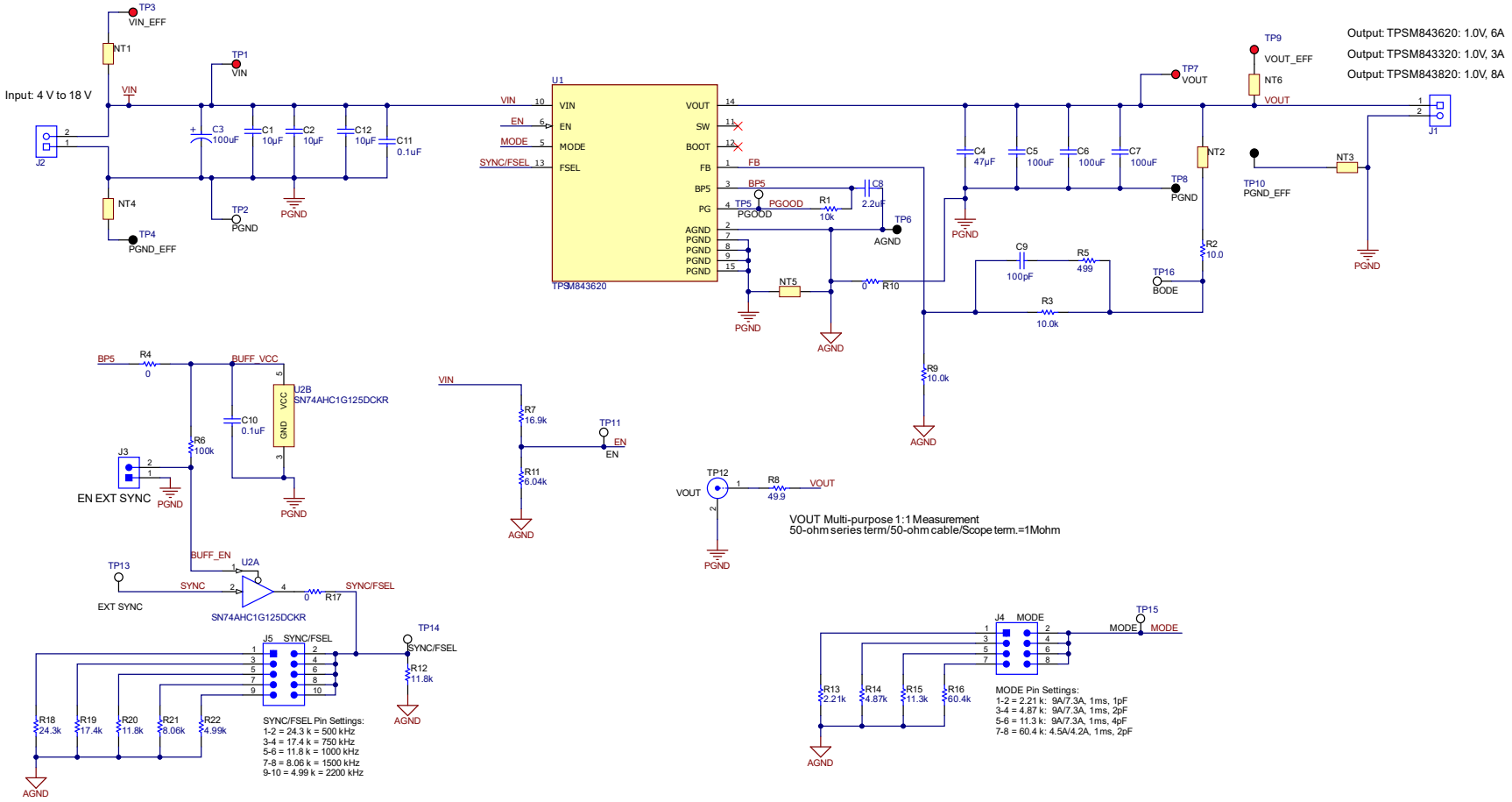


Figure 5-1. U1 Schematic

5.2 Bill of Materials

Table 5-1 presents the bill of materials for the TPSM843620EVM.

Table 5-1. TPSM843620EVM Bill of Materials

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
!PCB	1		Printed Circuit Board	BSR214	Any	
BO1, BO2, BO3, BO4	4		Bumpon, Hemisphere, 0.375 X 0.235, Black	SJ61A2	3M	Black Bumpon
C1, C2, C12	3	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7S, 0805	GRM21BC71E106KE11L	MuRata	0805
C3	1	100 µF	Cap Aluminum 100uF 35 V 20% (8 X 10.2mm) SMD Cylindrical 600 mA 5000hr 105°C T/R	EXV107M035A9MAA	Kemet	SMT_CAP_8MM3_8MM3
C4	1	47uF	CAP, CERM, 47 µF, 10 V,+/- 20%, X5R, 0805	GRM21BR61A476ME15L	MuRata	0805
C5, C6, C7	3	100uF	CAP, CERM, 100 uF, 10 V, +/- 20%, X5R, 1206_190	C3216X5R1A107M160AC	TDK	1206_190
C8	1	2.2µF	Multi-Layer Ceramic Capacitor 2.2uF 10 V X7S ±10% 0402 Paper T/R	GRT155C71A225KE13D	Murata	0402
C9	1	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H101J050BA	TDK	0402
C10	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	C0603C104J3RACTU	Kemet	0603
C11	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	GRM155R71E104KE14D	MuRata	0402
J1, J2	2		Terminal Block, 5.08 mm, 2x1, Brass, TH	ED120/2DS	On-Shore Technology	2x1 5.08 mm Terminal Block
J3	1		Header, 2.54mm, 2x1, Gold, TH	TSW-102-08-G-S	Samtec	Header, 2.54mm, 2x1, TH
J4	1		Header, 2.54mm, 4x2, Gold, TH	TSW-104-08-L-D	Samtec	Header, 2.54mm, 4x2, TH
J5	1		Header, 2.54mm, 5x2, Gold, TH	TSW-105-08-G-D	Samtec	Header, 2.54mm, 5x2, TH
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady	PCB Label 0.650 x 0.200 inch
R1	1	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GEJ103X	Panasonic	0402
R2	1	10	RES, 10.0, 1%, 0.1 W, 0603	RC0603FR-0710RL	Yageo	0603
R3, R9	2	10.0k	RES, 10.0 k, 0.5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040210K0DHEDP	Vishay-Dale	0402
R4, R17	2	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0ED	Vishay-Dale	0402
R5	1	499	RES, 499, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402499RFKED	Vishay-Dale	0402
R6	1	100k	RES, 100 k, 5%, 0.1 W, 0603	CRCW0603100KJNEAC	Vishay-Dale	0603
R8	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	RC0603FR-0749R9L	Yageo	0603
R13	1	2.21k	RES, 2.21 k, 1%, 0.1 W, 0603	RC0603FR-072K21L	Yageo	0603
R14	1	4.87k	RES, 4.87 k, 1%, 0.1 W, 0603	RC0603FR-074K87L	Yageo	0603
R15	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	RC0603FR-0711K3L	Yageo	0603
R16	1	60.4k	RES, 60.4 k, 1%, 0.1 W, 0603	RC0603FR-0760K4L	Yageo	0603
R18	1	24.3k	RES, 24.3 k, 1%, 0.1 W, 0603	RC0603FR-0724K3L	Yageo	0603
R19	1	17.4k	RES, 17.4 k, 1%, 0.1 W, 0603	RC0603FR-0717K4L	Yageo	0603
R20	1	11.8k	RES, 11.8 k, 1%, 0.1 W, 0603	RC0603FR-0711K8L	Yageo	0603
R21	1	8.06k	RES, 8.06 k, 1%, 0.1 W, 0603	RC0603FR-078K06L	Yageo	0603
R22	1	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	RC0603FR-074K99L	Yageo	0603
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	Samtec	Shunt
TP1, TP3, TP7, TP9	4		Test Point, Multipurpose, Red, TH	5010	Keystone Electronics	Red Multipurpose Testpoint
TP2, TP4, TP6, TP8, TP10	5		Test Point, Multipurpose, Black, TH	5011	Keystone Electronics	Black Multipurpose Testpoint
TP5, TP11, TP13, TP14, TP15, TP16	6		Test Point, Multipurpose, White, TH	5012	Keystone Electronics	White Multipurpose Testpoint
TP12	1		Connector, Receptacle, 50 ohm, TH	SMBR004D00	JAE Electronics	SMB Connector
U1	1		4-V to 18-V Input,6A Synchronous SWIFT™ Step-Down MicroSip™ Module with Integrated Inductor and Internally Compensated Advanced Current Mode Control	TPSM843620	Texas Instruments	MicroSIP15
U2	1		Single Bus Buffer Gate with 3-State Output, DCK0005A, LARGE T&R	SN74AHC1G125DCKR	Texas Instruments	DCK0005A

Table 5-1. TPSM843620EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R7	0	16.9k	RES, 16.9 k, 1%, 0.1 W, 0603	RC0603FR-0716K9L	Yageo	0603
R10	0	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0ED	Vishay-Dale	0402
R11	0	6.04k	RES, 6.04 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06036K04FKEA	Vishay-Dale	0603
R12	0	11.8k	RES, 11.8 k, 1%, 0.1 W, 0603	RC0603FR-0711K8L	Yageo	0603

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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