Sequencing With TPS54x80 and TPS54x73 SWIFT DC/DC Converters

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ABSTRACT

Design of a power supply for a high-performance point-of-load processor requires special attention to manage core and input/output (I/O) voltage sequencing, which is critical to device operation and long term reliability. The TPS54x80 devices of low input voltage synchronous-buck dc/dc converters are designed for easily implementing sequential, ratio-metric, or simultaneous sequencing schemes. For pre-biased conditions on the core supply, the TPS54x73 family is designed to disable sinking during start-up (DSDS) and maintain prebiasing diode reliability.

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1 Introduction

The TPS54x80 family was specifically designed for applications that have critical power supply sequencing requirements. The devices have a TRACKIN pin to implement different sequencing methods, such as sequential, ratio-metric, and simultaneous sequencing (see SLVA117, *Dual Output Power Supply Sequencing for High Performance Processors* for a detailed explanation of these sequencing methods). The TRACKIN pin has an analog multiplexer that compares the 0.891-V internal voltage reference to the voltage on the TRACKIN pin and connects the lower of the voltages to the noninverting node of the error amplifier, see Figure 1. When the TRACKIN pin voltage is lower than the internal voltage reference, the TRACKIN pin voltage is effectively the reference for the power supply. The selection of the resistors of the voltage divider on the TRACKIN pin (e.g. R1 and R2) determines the power sequencing method. By selecting the TRACKIN voltage divider to have the same ratio as the voltage divider in the feedback compensation loop (i.e. R3 and R4) the core and I/O supply powers up and down with waveforms similar to Figures 9 and 10. Assuming R3 and R1 are the same resistance value, by making the R2 value less than or greater than R4, the power sequencing waveforms in Figures 5 through 8 can be obtained. Resistor selection is discussed later in greater detail.

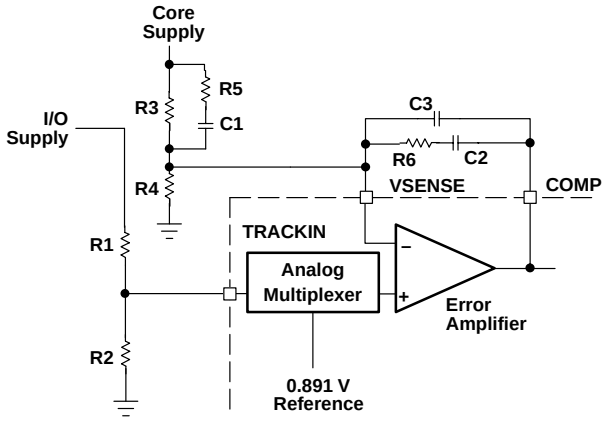

Figure 1. Analog Multiplexer

2 Dual Output Power Supply Design Example

A dual output power supply was designed using the SWIFT™ designer software tool. Since the software tool designs single output designs, two separate designs were performed with the software using the TPS54610 for the 3.3-V I/O supply and the TPS54680 for the +1.8-V core supply. The input voltage rail is a nominal 5 V with ±10% tolerance. The power supplies were designed with a switching frequency of 700 kHz so that smaller value inductors can be used to minimize the physical size and still maintain a low output voltage ripple. The dual output power supply schematic is shown in Figure 2.

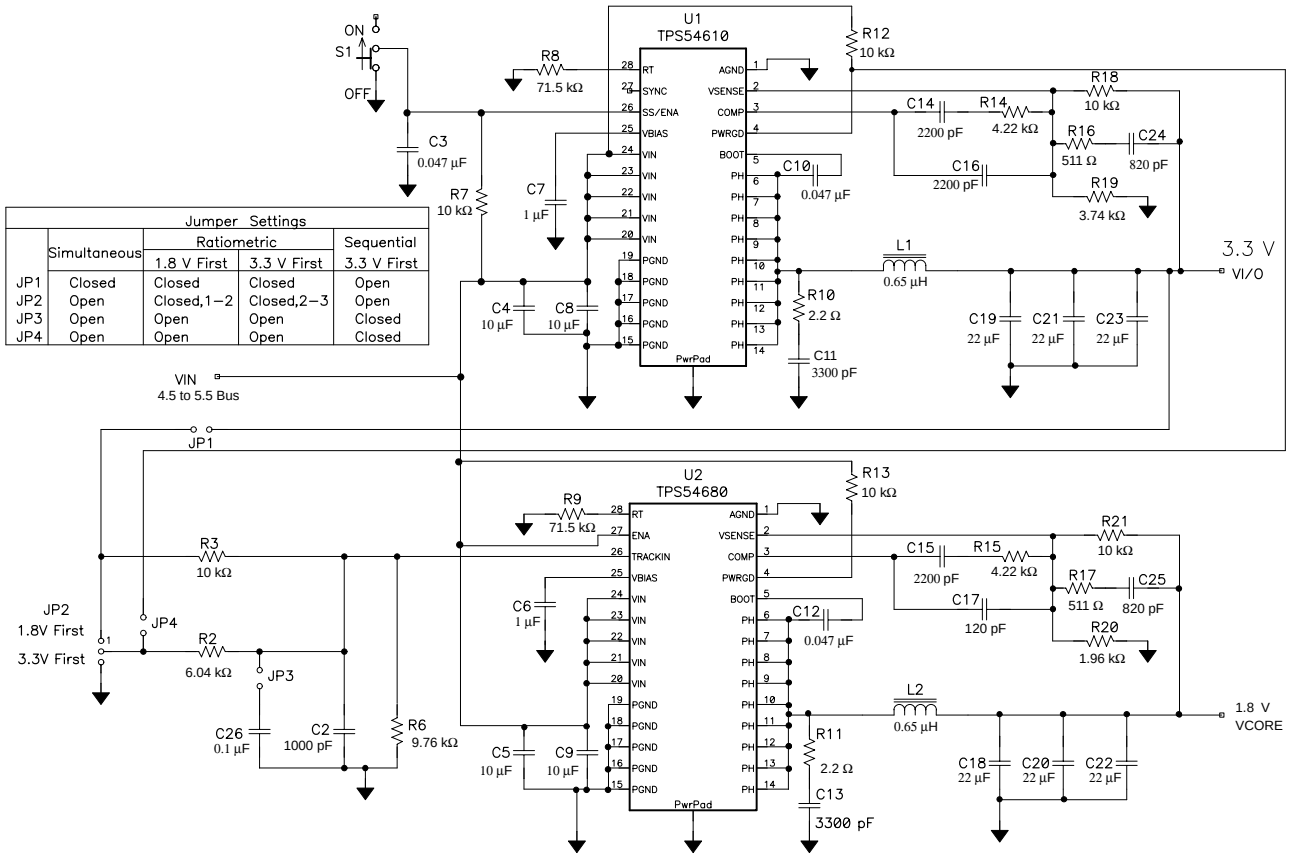

Figure 2. Dual Output Power Supply Schematic

3 Sequential Implementation

Sequential start-up is implemented by connecting the power good (PWRGD) pin of U1 to the TRACKIN pin of U2 with a resistor–capacitor (RC) circuit. See Figure 2 for the schematic, and refer to the jumper setting table for the proper connection. The power up and down waveforms in Figures 3 and 4 were measured using a 10-kΩ and 0.1-µF RC circuit. Resistor R12 is connected to the input voltage supply and TRACKIN pin. Capacitor C26 is connected from the TRACKIN to ground. In Figure 3, the +3.3-V I/O supply ramps up first. When supply reaches its final 3.3-V steady state value, the open drain output of the PWRGD pin releases the TRACKIN pin and the core supply rises at the rate of the RC time constant. The C26 capacitor is used to minimize the inrush current during start-up of the core supply. The PWRGD pin asserts, pulling the TRACKIN pin low, when the SSENA of U1 pin is pulled low or when the I/O voltage is below 90% of the desired regulated voltage. Ideally, the I/O and core supply powers down in the opposite order in which the supplies powered up. If there is no load or a light load on the core, when the I/O rail powers down, the TPS54x80 devices have the ability to sink current and transfer the energy stored in the output capacitor to the input capacitor. Figure 4 shows the power down with 1-kΩ loads on both outputs.

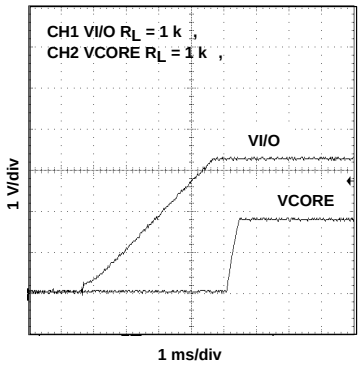

Figure 3. Sequential Sequencing Power Up

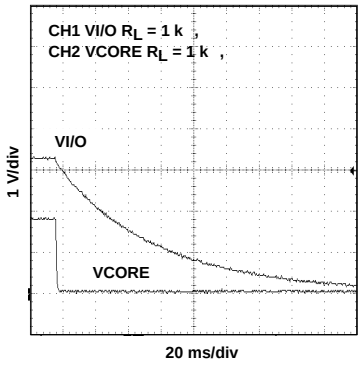

Figure 4. Sequential Sequencing Power Down

4 Ratio-Metric Implementation

Ratio–metric sequencing is implemented by the selection of the resistor values of the voltage divider on the TRACKIN pin. Resistors R3 and R4, in Figure 1, adjust the output voltage of the core supply during normal operation. Resistors R1 and R2, in Figure 1, determine the sequencing method that is implemented. To simplify the sequencing design, R1 should equal the resistance value of R3 regardless of the sequencing method. For sequencing applications that need the core supply to be less than the I/O supply during start up, R2 should be less than the value of R4. Similarly, in applications when the core supply should be greater than the I/O supply during power up, R2 should be greater than R4. If there is a maximum voltage difference that can not be exceeded between the rails, use equation 1 to calculate R2.

$$R2 = R1 \times \left[\frac{0.891}{(Vcore + \Delta V - 0.891)} \right] \quad (1)$$

ΔV is the maximum voltage difference between the I/O and core supply and is a positive number for the sequencing illustrated in Figure 5. The waveforms in Figures 5 and 6 were measured using the circuit illustrated in Figure 2. Resistors R2, R3, and R6 in Figure 2 form the voltage divider on the TRACKIN pin. R2 and R6 are in parallel with an equivalent resistance of approximately 3731 Ω. Resistor R3 is 10 kΩ. Equation 1 can be rearranged to solve ΔV. Substituting 3731 Ω for R2 and 10000 Ω for R1 in equation 1, ΔV equals +1.48 V. The waveforms in Figures 7 and 8 were also measured with the power supply shown in Figure 2. The difference is R2 and R3 are paralleled with an equivalent resistance of 3765 Ω in the voltage divider. Substituting 3765 Ω for R1 and 9760 Ω for R2 in equation 1, ΔV is therefore calculated to be –1.56 V.

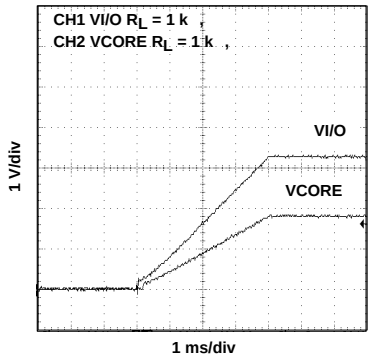

Figure 5. Ratio-Metric Power Up (Core)

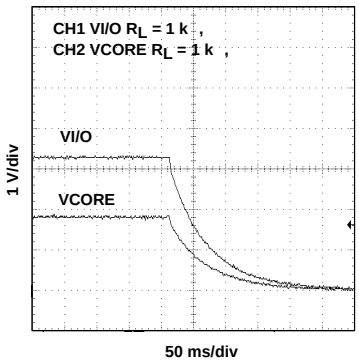

Figure 6. Ratio-Metric Power Down (Core)

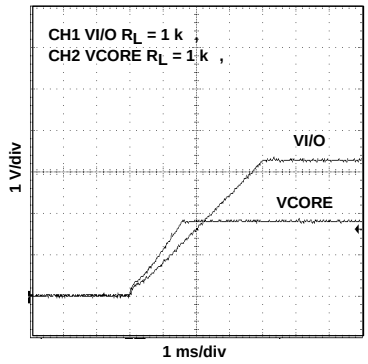

Figure 7. Ratio-Metric Power Up (I/O)

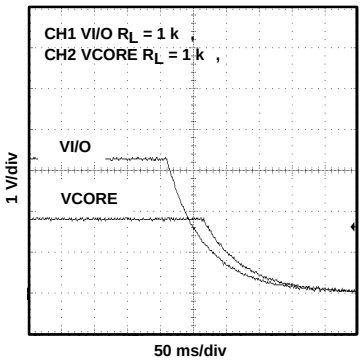

Figure 8. Ratio-Metric Power Down (I/O)

5 Simultaneous Implementation

Similar to the ratio-metric implementation, simultaneous sequencing is implemented using a voltage divider on the TRACKIN pin. For simultaneous sequencing, the objective is to minimize the voltage difference between the power supply outputs during power up and down. Using equation 1, R2 is calculated by substituting zero volts for ΔV. For simultaneous sequencing R2 is always equal to R4, if R1 and R3 are equal, referencing the schematic in Figure 1. The waveforms in Figures 9 and 10 were measured with both outputs loaded with 1-kΩ resistors. It can be observed from the waveforms that the voltage difference between the rails is minimal during power down. If the I/O supply is heavily loaded and the core supply is lightly loaded during power down there may be a voltage difference between the rails. This is because the core supply can not sink current as fast as the I/O supply falling. Adding more bulk capacitance on the I/O output can control this effect.

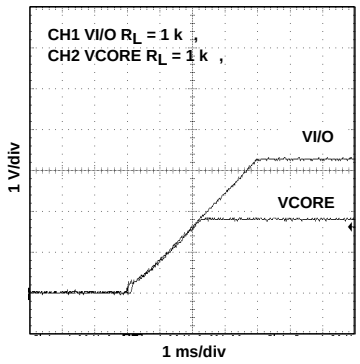

Figure 9. Simultaneous Power Up

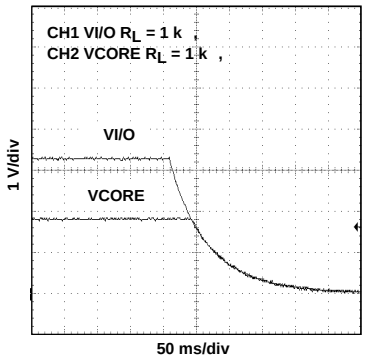

Figure 10. Simultaneous Power Down

6 Prebiased Conditions

The TPS54x80 family is suited for sequencing applications when the core and I/O supplies turn on at relatively the same time. When the I/O voltage supply has been on for a length of time before the processor core voltage is to be turned on, certain processors require the core and I/O supply not to exceed a specified voltage differential during start-up. In this case, the TPS54x73 series of synchronous buck SWIFT converters is specifically designed for applications that require a prebias condition on the core voltage supply. To accomplish this, the output of the core voltage supply is connected to the output of the I/O voltage supply with a number of series diodes. Therefore, the core voltage is at a level equal to the I/O voltage minus the diode voltage drops during start-up. A circuit was constructed to demonstrate prebiasing using the TPS54673 and is shown in Figure 11. The I/O supply of 3.3 V is used to prebias the core supply of 2.5 V. Figure 12 shows that the differential voltage between the core and I/O supplies does not exceed the voltage drop of the two series diodes. Additional diodes can be added in series when the core voltage requirement decreases. The TPS54x73 family features disabled current sinking during start-up (DSDS) to prevent the prebiased load from being pulled to ground during start-up. The synchronous rectifier of the TPS54x73 devices is kept off during start-up to maintain diode reliability without the need of additional circuitry. Once the TPS54x73 is in regulation, it is allowed to source and sink current.

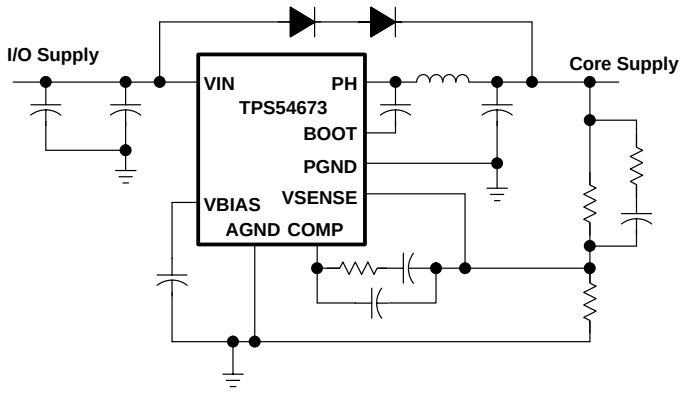

Figure 11. Prebiasing Application Example

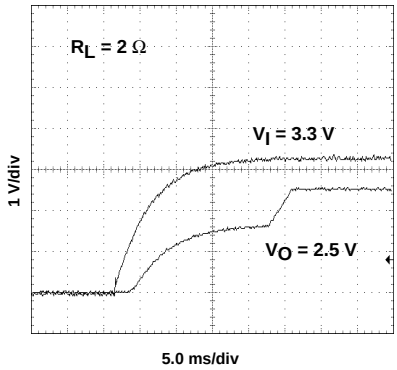

Figure 12. Prebiasing Start-Up Waveform

7 Conclusion

Special attention must be given to power supply sequencing when designing reliable power supplies for performance processors. Sequencing techniques are easily implemented using the TPS54x80 and TPS54x73 families of SWIFT dc/dc converters. Additionally, the SWIFT™ Designer software tool is available to help with the entire power supply design and supports both families.

8 Acknowledgements

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