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Designing Fast Response Synchronous Buck Regulators Using the TPS5210

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Designing Fast Response Synchronous Buck Regulators Using the TPS5210

ABSTRACT

This application report describes the operation and performance of a 12-V to 2-V 20-A synchronous buck regulator evaluation design using the TPS5210 Programmable Synchronous Buck Regulator Controller. Experimental data shows tight static and dynamic regulation (±55 mV), fast transient response (within 1 μs), high efficiency (up to 90%), and stable operation with good noise immunity. The TPS5210 architecture is also presented describing the major functional blocks: 1% reference, fast hysteretic comparator with noise suppression, droop compensation, 30-V rating from BOOT pin to ground, 8-V/2-A gate drive with adaptive deadtime control, Vds current sensing, slowstart, OVP, powergood, UVLO, and INHIBIT. Finally, a simple mathematical description of switching frequency and output voltage for a ripple regulator is derived and presented, showing good correlation with experimental data.

1 Introduction

This application report describes how to design and construct a 12-V to 2-V 20-A synchronous buck regulator (example design) using a TI TPS5210 Programmable Synchronous Buck Regulator Controller (TPS5210) and appropriate external components. The example design illustrates measured performance, component selection, design considerations, and board layout guidelines.

Forthcoming workstations, driven by next-generation high-performance microprocessors, may require from 40 to 80 watts of power for the CPU alone. Although the nominal supply output voltage may be 2 V, the supply should still be capable of providing an output voltage range from 1.3 V to 3.5 V, determined by a 5-bit DAC code. Parasitic interconnect impedances between the power supply and the processor must be kept to a minimum[1] since maximum current could be anywhere from 20 A to 40 A. Load current must be supplied with up to 30 A/μs slew rate, while keeping the output voltage within tight regulation and response time tolerances.[2] Fast response synchronous buck converters controlled by the Texas Instruments TPS5210 are ideally suited for microprocessor power applications requiring fast response and precise regulation to rapidly changing loads.

Conventional regulator control techniques include fixed frequency voltage-mode, fixed frequency current-mode, variable frequency current-mode, variable on-time, or variable off-time. CPU power supplies that are designed using these types of control methods require additional bulk storage capacitors on the output to maintain V_O within the regulation limits during the high di/dt load transients because of the limited bandwidth of the controller. Some controllers add a fast loop around the slower main control loop to improve the response time, but V_O must deviate outside a fixed tolerance band before the fast loop becomes active. The hysteretic control method employed by the TPS5210 offers superior performance with no requirements for additional output capacitance or difficult loop compensation design.

The TPS5210 was optimized for tight V_O regulation under static and dynamic load conditions, for improved system efficiency, and for operation in systems that derive main power from 12 V, 5 V, and at 3.3 V.

1.1 Synchronous Buck Regulator Operation

The synchronous buck converter is a variation of the traditional buck converter. The main switching device is usually a power MOSFET and is driven in the same manner as in a traditional buck converter. The freewheeling rectifier, usually a Schottky device, is replaced by a power MOSFET and is driven in a complementary or synchronous fashion relative to the main switching device; when one MOSFET is on, the other is off. The freewheeling MOSFET is selected so that its ON voltage drop is less than the forward drop of the original freewheeling rectifier, thus increasing conversion efficiency. A very important design issue when using a synchronous buck converter is preventing cross-conduction of the two power MOSFETs, i.e., preventing both MOSFETs from being on simultaneously. A small amount of deadtime is necessary.

Figure 1 shows a simplified schematic of a synchronous buck converter. The TPS5210 senses the output voltage and then drives Q1 and Q2 depending on the sensed voltage. The TPS5210 senses the voltage at the junction of Q1, Q2, and L1 and uses it to actively prevent simultaneous conduction of Q1 and Q2.

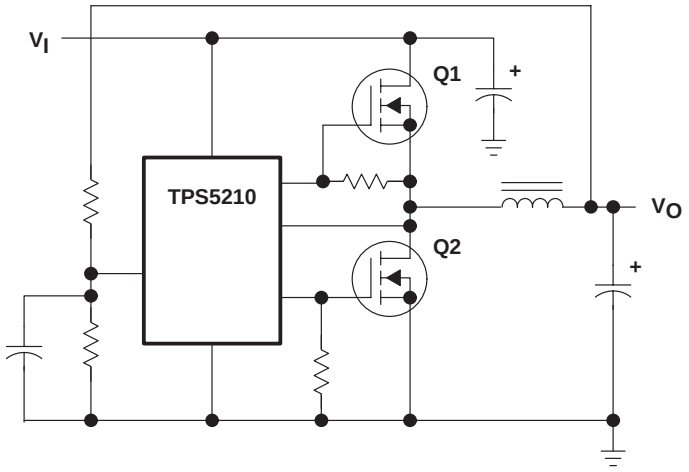


Figure 1. Simplified Synchronous Buck Converter Schematic

1.2 Hysteretic Control Operation

Hysteretic control, also called bang-bang control or ripple regulator control, maintains the output voltage within the hysteresis band centered about the internal reference voltage. Figure 2 shows a simplified example of a hysteretic controlled output voltage with a reference voltage of 2.000 V and a hysteresis band of 50 mV. If the output voltage is at or below the level of the reference minus one-half of the hysteresis band (V_{Lo} = 1.975 V), the TPS5210 turns off the low-side MOSFETs (Q2 in Figure 1) and turns on the high-side MOSFETs (Q1 in Figure 1) of the synchronous buck converter power stage. This is the power stage on-state, and it causes the output voltage to increase. When the output voltage reaches or exceeds the reference plus one-half of the hysteresis band (V_{Hi} = 2.025 V), the TPS5210 turns off the high-side MOSFETs and turns on the low-side MOSFETs. This is the power stage off-state, and it causes the output voltage to decrease. This hysteretic method of control keeps the output voltage within the hysteresis band around the reference voltage. If output-load current steps or input-voltage transients force the output voltage out of the hysteresis band, the TPS5210 sets the power-stage MOSFETs in the continuous on or off state as required to return the output voltage to the hysteresis band. Thus, the output voltage is corrected as quickly as the output filter allows. There are no error amplifier sensing and adjusting delays, as is the case with either voltage- or current-mode controllers. Other advantages of hysteretic control include no loop compensation design and no input filter interaction problems.

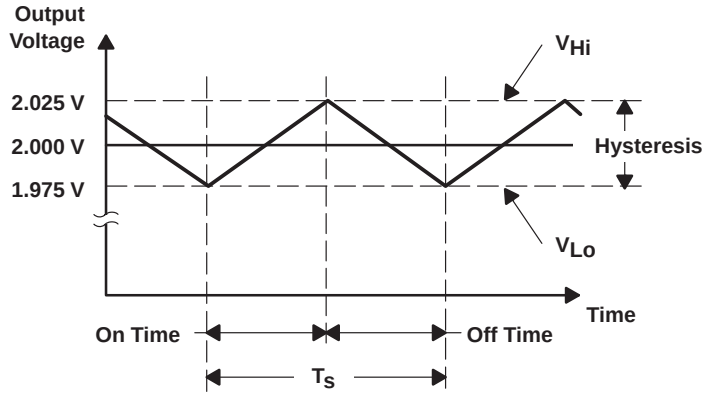


Figure 2. Simplified Hysteretic Controlled Output Voltage Waveform

2 TPS5210 Operation Overview

The TPS5210 is a controller for a high-performance synchronous buck hysteretic regulator. Figure 3 shows the schematic and waveforms of a hysteretic regulator, including a simplified block diagram of the TPS5210. The TPS5210 block diagram shows only the hysteretic regulator functions. The main function blocks are shown: synchronous-buck gate drivers with adaptive deadtime control, 1% reference, hysteresis level control, droop compensation control, and current sense control. Not shown in the block diagram are the protective functions such as slowstart and overcurrent protection, control functions such as Inhibit and VID inputs, or the separate power and analog grounds or floating high-side drive.

The main hysteretic control block is a fast comparator with a hysteresis level that is symmetrical about the reference voltage. Excluding delays, the high-side gate drive signal toggles on when the instantaneous output voltage decreases below the lower hysteresis limit, V_{Lo}; the gate drive signal toggles off when the instantaneous output voltage increases above the upper hysteresis limit, V_{Hi}. The low-side gate drive signal toggles synchronously so that when the high side is on, the low side is off. The hysteresis is symmetrical with respect to the reference voltage. The TPS5210 regulates V_O to the reference value while also regulating the ripple voltage on V_O. The hysteretic regulator provides a fast response to load transients and is well suited for CPU power supplies. The operating frequency of the hysteretic regulator depends upon V_I, V_O, the output inductor and the output capacitors and is very predictable because V_I typically has a 5% regulation limit in CPU systems. Section 4.4.2 in this application report describes how to predict the operating frequency with design equations.

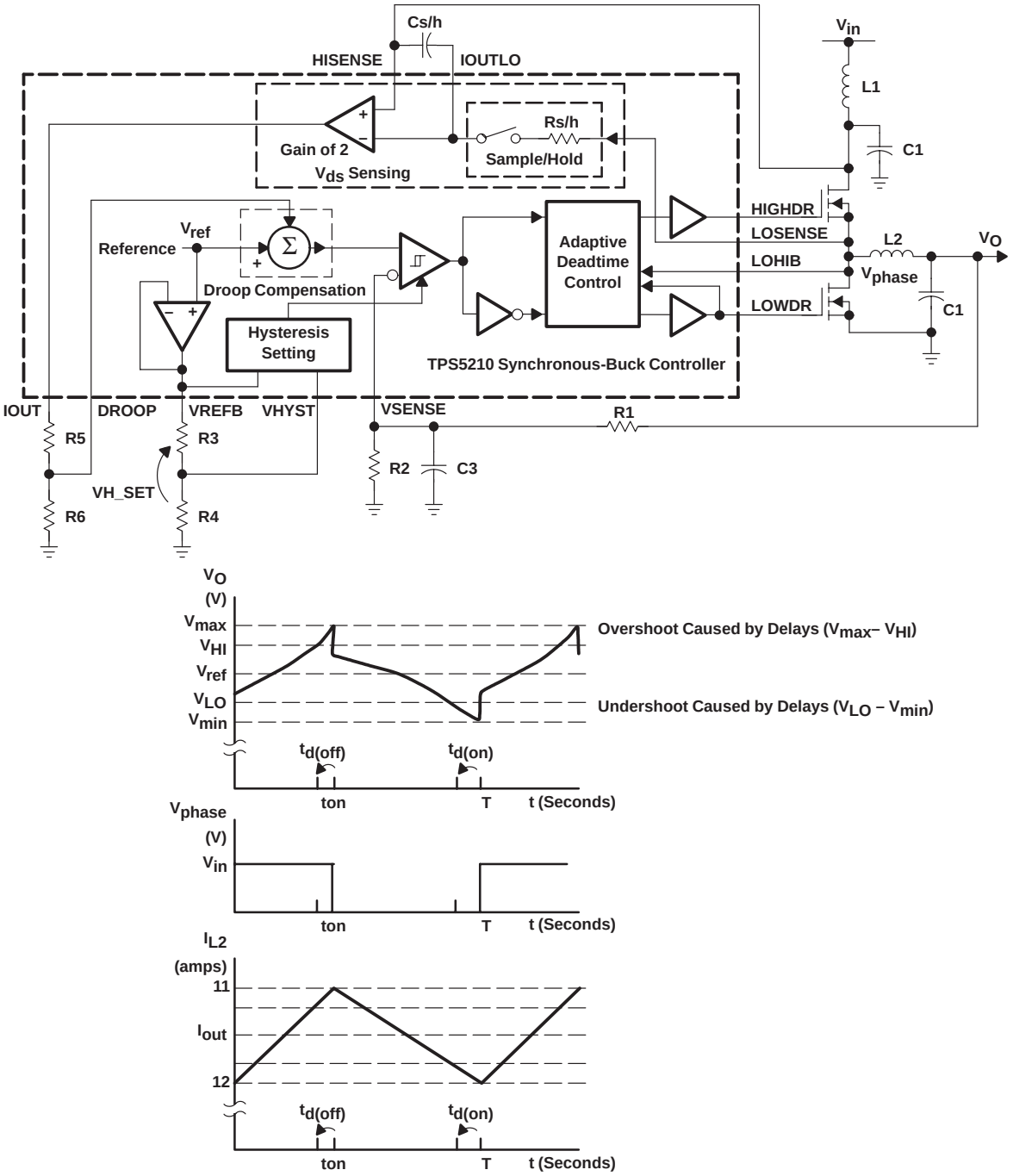


Figure 3. Hysteretic Regulator and Waveforms

Referring again to Figure 3, delays in the feedback path cause the ripple voltage to exceed the hysteresis levels set by the TPS5210. The source of the delays includes the propagation delay from the comparator inputs to the synchronous buck gate driver outputs (250ns maximum), the turn-on/turn-off delays of the power MOSFETs, the non-overlap delay time of the deadtime control circuit (100ns maximum), and the delay from the external RC filter between V_O and the VSENSE pin (R1 and C3 in Figure 3). The ripple voltage is regulated to Vmax–Vmin. This higher ripple voltage should be taken into account when determining the programmed ripple voltage versus the actual ripple voltage.

The hysteresis band ($V_{HI} – V_{LO}$) is set with a voltage divider from the buffered reference (VREFB); the hysteresis band is equal to twice the difference voltage between VREFB and VHYST (V_{H_SET} in Figure 3). The hysteresis band is set to a percentage of Vref within the hysteretic comparator.

The synchronous buck gate drivers have adaptive deadtime control to minimize the conduction time through the body-drain diode of the low-side MOSFET and prevent simultaneous conduction of the power MOSFETs, which would cause shoot-through currents.

The output current is indirectly sensed by sampling and holding the voltage across the high-side MOSFET. The RC time constant of the sample/hold switch resistance and hold capacitor is set to be greater than the conduction time of the high-side MOSFET so that the average voltage across the high-side MOSFET is sampled, and is proportional to the DC output current. The differential voltage across the sample/hold capacitor is amplified by 2 and converted to a single-ended signal on the IOUT pin; the voltage on IOUT is proportional to the output current.

The DROOP compensation circuit provides additional margin to maintain V_O within the load transient tolerance limits required by the processor. V_O is offset above the reference by the resistor divider from V_O to VSENSE (R1 and R2 in Figure 3). The voltage on the DROOP pin is made proportional to the load current by the resistor divider from IOUT to DROOP (R5 and R6 in Figure 3) such that V_O will be offset below the reference under full-load conditions. Section 3.2.3 contains test results that illustrate the advantage of DROOP compensation during a transient load.

Operation of the TPS5210 relies on the output ripple voltage waveform characteristics. The output voltage consists of an ac waveform riding on the average dc waveform. The ac component is influenced predominantly by the output capacitor ESL, ESR, and capacitance values in conjunction with the inductor ripple current. The output voltage is composed of:

$$vout(t) = Vdc + vac(t) = Vdc + ESL \times \frac{d\left(i_{ripple}(t)\right)}{dt} + ESR \times i_{ripple}(t) + \frac{1}{Cout} \times \int i_{ripple}(t)dt$$

The ripple component from ESL causes the voltage steps; ESR causes the ramps; and capacitance causes the curvature in the ripple voltage during the switching transitions, as shown in Figure 3. Section 4 gives a more detailed analysis of the switching frequency and output voltage waveforms.

3 Example Design Circuit

The circuit shown in Figure 4 was designed and tested to demonstrate the performance attainable from a synchronous buck regulator using the TPS5210. The example was designed for typical server application operating conditions; Vin = 12 V, V_O = 2.0 V, Iout = 20 A peak. Table 1 lists the critical power stage components for the example design of Figure 4.

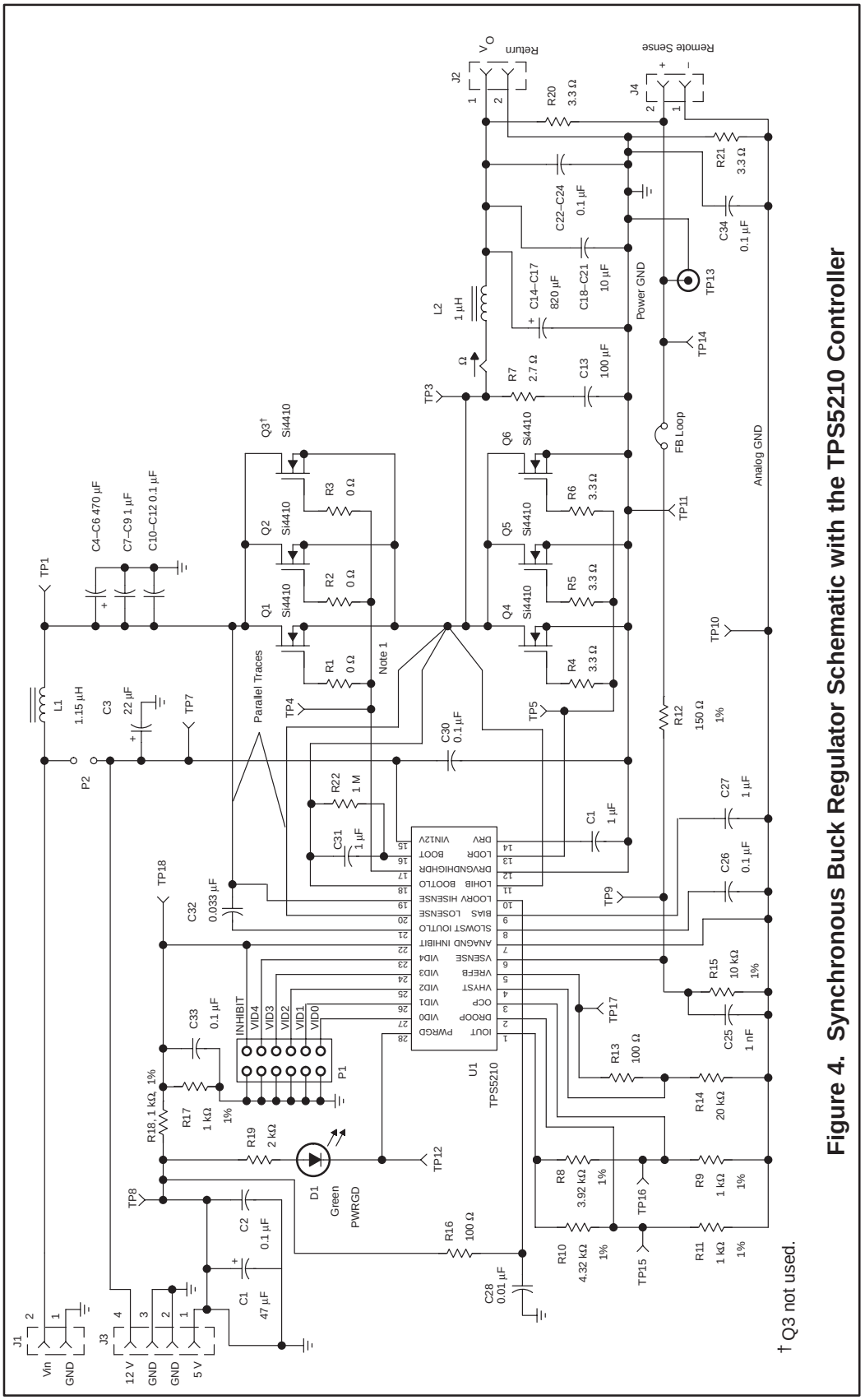


Figure 4. Synchronous Buck Regulator Schematic with the TPS5210 Controller

Table 1. Critical Power Stage Components

Component Designator	Description
Q1 – Q6†	Si4410
C4 – C6	470 µF, 16 V, Sanyo OS-CON #16SA470M
L1	8 turns, 18 AWG on Micrometals T44-8/90 toroid
L2	7 turns, 16 AWG on Micrometals T68-8/90 toroid
C14 – C17	820 µF, 4 V, Sanyo OS-CON #4SP820M
C18 – C21	10 µF, 16 V ceramic; Murata #GRM235Y5V106Z16
C7 – C9	1 µF, 16 V; Panasonic #ECSH1CY105R

† Q3 not used.

3.1 Measured Performance

The tight line and load regulation of the example design with droop disabled, are shown in Figures 5 and 6 respectively with V_O = 2 V. Regulation is maintained well below 1%.

3.1.1 Line and Load Regulation

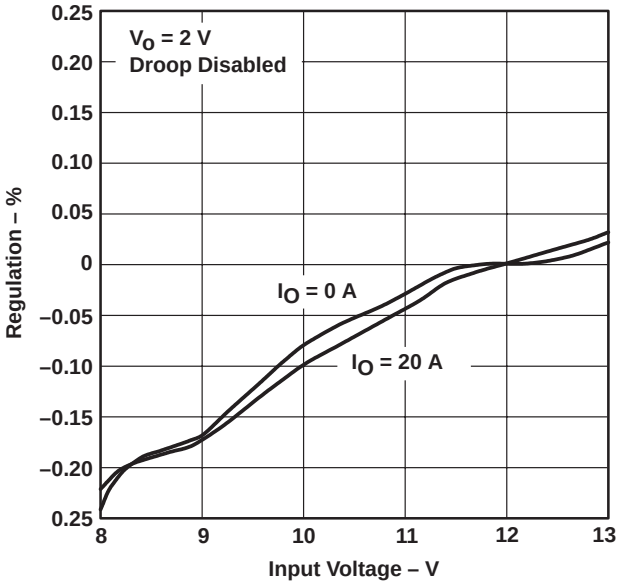


Figure 5. Normalized Line Regulation

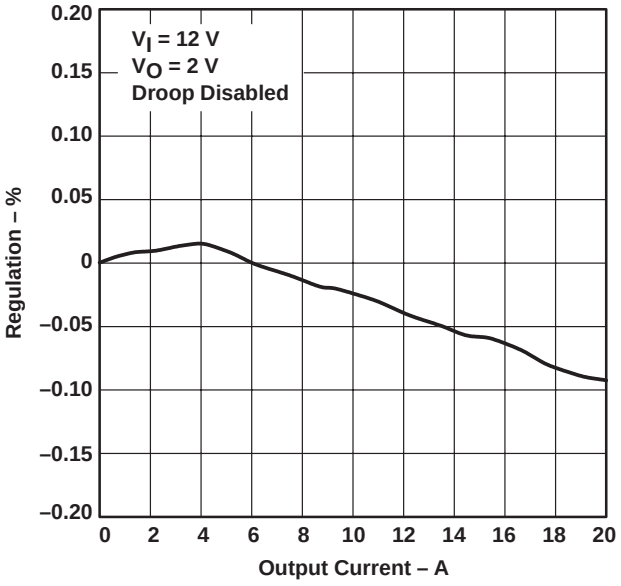


Figure 6. Normalized Load Regulation

3.1.2 Efficiency

Since no current sense resistor is used, and adaptive delay circuitry is included for optimum drive, the efficiency is above 90% at 10 A and 88% at 20 A, as shown in Figure 7.

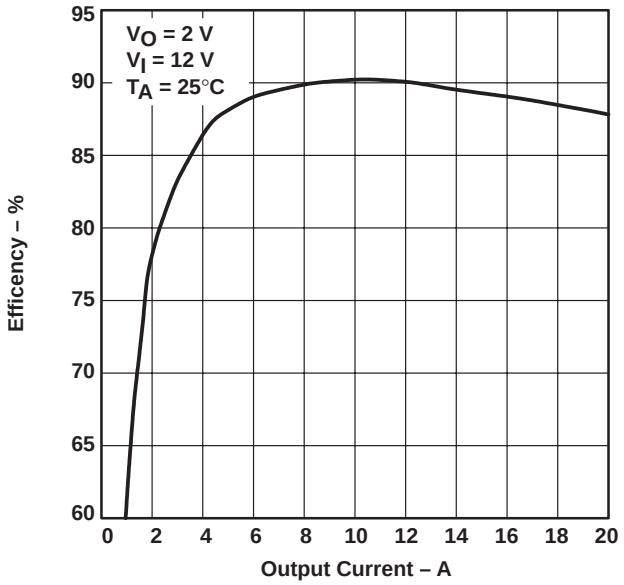
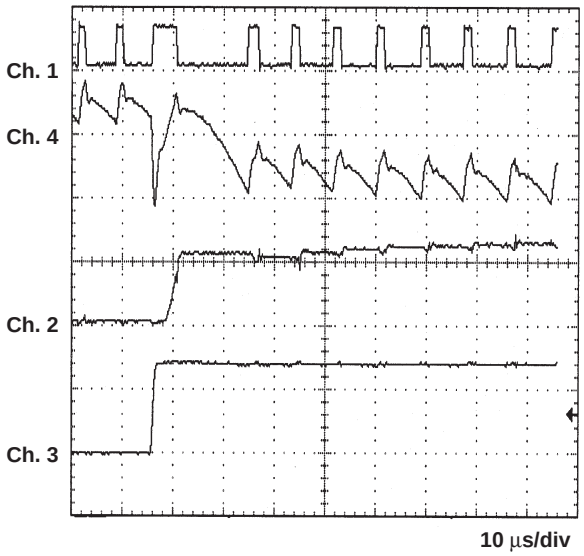


Figure 7. Efficiency vs Load Current

3.1.3 Transient Load Response

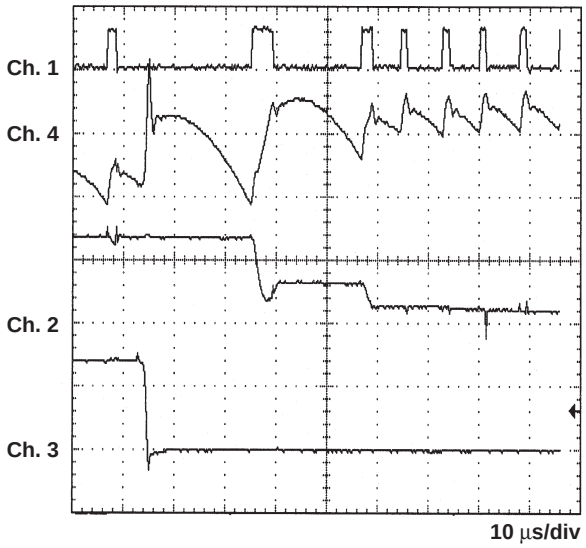
Transient load operation of the TPS5210 is similar to the dc ripple regulation operation. The high-side gate drive signal maintains its state until the one hysteresis limit is reached, then the complement state remains fixed until the other hysteresis limit is reached. Propagation delays still apply. This characteristic allows extremely fast response times to load transitions.

A load transient response test was conducted with a 0.1-A to 20.4-A load step at a 30-A/μs slew rate, and 1-kHz repetition rate (V_I = 12 V, V_O = 2 V). Figures 8 and 9 show the transient response for a light-to-full load transition and a full-to-light load transition, respectively, with droop active. After quickly regaining regulation, the voltage droop compensation circuit reduces the regulation set point by 50 mV in Figure 8, and increases it by 50 mV in Figure 9. With droop active, the transient regulation on V_O is ±55 mV. The controller response time is less than 1 μs.



Ch. 1: Voltage at the junction of high-side MOSFETs and low-side MOSFETs (20 V/div)
Ch. 4: Output ripple voltage (50 mV/div)
Ch. 2: Voltage on DROOP pin (50 mV/div)
Ch. 3: Output load current (14.5 A/div)

Figure 8. Light-to-Full Load Transient Response



Ch. 1: Voltage at the junction of high-side MOSFETs and low-side MOSFETs (20 V/div)
Ch. 4: Output ripple voltage (50 mV/div)
Ch. 2: Voltage on DROOP pin (50 mV/div)
Ch. 3: Output load current (14.5 A/div)

Figure 9. Full-to-Light Load Transient Response

3.1.4 Overcurrent Protection

Overcurrent protection, OCP, is demonstrated in Figure 10 with load shorted, and in Figure 11 with the terminal common to MOSFETs shorted.

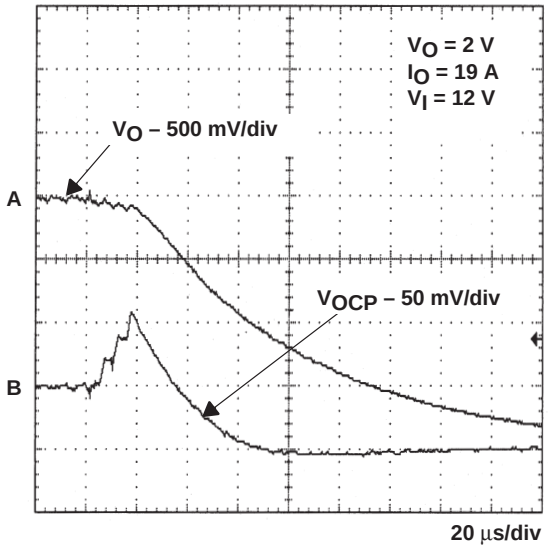


Figure 10. OCP Shorted Load Waveforms

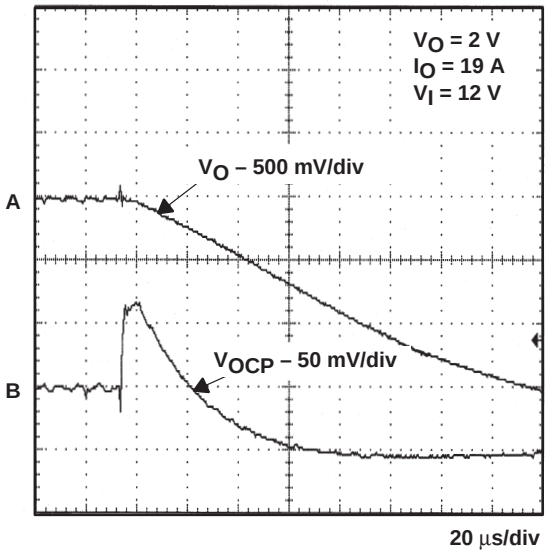
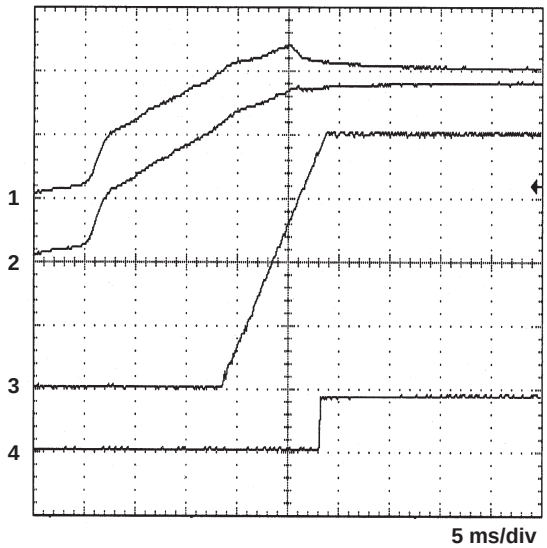


Figure 11. OCP Short-to-Ground Fault

3.1.5 Power-Up Performance

Figure 12 shows the power-up performance for a 20-A load. Its performance, similar to no load, is well behaved with almost no output voltage overshoot. The 12-V supply must be greater than the 10-V UVLO start threshold, and the 5 V supply must be greater than 4.2 V (set by a resistor divider from 5 V input to the INHIBIT pin in Figure 4) before the TPS5210 is enabled.



Ch. 1: 12-V supply voltage (5 V/div)
Ch. 2: 5-V supply voltage (2 V/div)
Ch. 3: Output voltage (0.5 V/div)
Ch. 4: POWERGOOD pin (5 V/div)

Figure 12. Power-Up Performance (I_O = 20 A)

4 Example Circuit Design Procedure

This section shows the procedure used in designing and selecting the power stage components to meet the performance parameters shown in Table 2 for the example circuit shown in Figure 4.

Before proceeding with any power supply design, certain decisions must be made that impact the course of the design. For this example design, the following performance parameters are adopted:

Table 2. Power Stage Design Parameters

PARAMETER	VALUE
Nominal output voltage	2 V
Output voltage static tolerance (see Note 1)	±60 mV
DC output voltage tolerance	±22 mV
Output ripple and noise	35 mV pk–pk
Output load regulation	±0.1% V_O
Output line regulation	±0.25% V_O
Output voltage transient tolerance (see Note 2)	±100 mV
Load transient response	60 mV pk
Load transient response time	2 µs
Maximum output current	20 Amps
Nominal switching frequency	125 kHz
Ambient temperature range	0°C – 60°C

NOTES: 1. Output voltage static tolerance includes:
– DC output initial voltage tolerance and set point adjust tolerance
– Output ripple and noise
–Output load regulation
– Temperature
2. Output voltage transient tolerance includes:
– Load transient output voltage deviation
–Response time for output voltage return to within static tolerance limits.

4.1 Duty Cycle Estimate

An estimate of the duty cycle is used frequently in the following sections. The duty cycle, D, is the ratio of the high-side power-switch conduction time to the period of one switching cycle. The duty cycle for a continuous mode step-down converter is given by:

$$D = \frac{V_O + V_{DS(ON)}}{V_I}$$

Where:

$V_{DS(ON)}$ = An estimate of the on-voltage of the power MOSFETs.

For an initial estimate for $V_{DS(ON)}$, use 0.2 V. So, for an output voltage of 2 V and an input voltage of 12 V, the duty cycle calculates to:

$$D = \frac{2\ V + 0.2\ V}{12\ V} = 0.18$$

4.2 Input Capacitance

The input capacitance provides a low-impedance voltage source for the power stage. The ESR, ESL, RMS current rating and capacitance value of the input capacitance are important parameters in the selection process. The most stringent requirement is often the RMS current that the capacitance must handle. An equation for the RMS current seen by the input capacitance for a buck converter is given by:

$$I_{Cin(RMS)} = \sqrt{D \times (1–D) \times I_O^2}$$

The above equation assumes that the output ripple current is small, that there is an input inductor, and that its ripple current is small. For V_I = 12 V and I_O = 20 A, we get:

$$I_{Cin(RMS)} = \sqrt{0.18 \times (1–0.18) \times 20^2} = 7.7\ A\ RMS$$

The input capacitance for this design uses three 470-µF, 16-V Sanyo OS-Con type electrolytic capacitors in parallel. They are C4, C5, and C6 in Figure 4. The ripple current rating for one of these capacitors is 6.08 A RMS at 45°C and is reduced to 4.26 A RMS at 85°C. Using linear interpolation to get an estimate for the rating at 60°C gives a rating of 5.5 A RMS for each capacitor. The total ripple current rating for the input capacitance is 3×5.5 = 16.5 A RMS.

4.3 Output Filter Design

Unlike fixed-frequency PWM-controlled power supplies, the output filter design is driven primarily by the need to provide satisfactory output voltage performance in response to fast load transients encountered when supplying power to current- and next-generation microprocessors. A secondary consideration is the switching frequency resulting from the output filter component values. This section discusses important considerations when selecting/designing the output filter elements. A detailed analysis of the output voltage ripple characteristics is also presented, resulting in an expression for predicting the power supply switching frequency.

4.3.1 Output Capacitance

Normally, the output capacitor is selected to limit ripple voltage to the level required by the specification, but in a hysteretic regulator, such as this one, the TPS5210 essentially determines the output voltage ripple. The output ripple is previously chosen to be 35 mV and is relatively independent of the output capacitor characteristics. Since output voltage ripple is set by the comparator hysteresis band, the output capacitor is chosen to provide satisfactory response to fast load transients.

To show the importance of the output capacitor characteristics, consider the following: This example circuit is designed for a worst case load step of no load (0 Amps) to full load (20 Amps) with a slew rate of 30 A/μs. This implies that the load transient occurs 667 ns $\left(\frac{20\ A}{30\ A/\mu s} = 667 ns\right)$. For a transient of this duration, the output filter alone controls the initial output voltage deviation. Further examination shows that the output filter inductor current changes little during the load transient. Therefore, for fast load transients, the output capacitor characteristics dominate the output filter performance. In this design, the output capacitor's ESR (equivalent series resistance) and ESL (equivalent series inductance) are the parameters that are most critical.

To calculate the ESR requirement, assume that all the load transient current is supplied by the output capacitor. Also assume that the output voltage change due to the capacitor's capacitance is much smaller than the voltage change due to the ESR, and that the capacitor's ESL is negligible. In most practical applications, these assumptions are reasonable and they greatly simplify calculations. The ESR required to limit output voltage change to 60 mV due to a 20 amp load step is:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} = \frac{60\ mV}{20\ A} = 3\ m\Omega$$

The required level of ESR requires a large amount of capacitance. For this design, four Sanyo OS-Con type electrolytic capacitors connected in parallel are selected. These capacitors are a good compromise between performance, cost, and board area requirements. Less costly capacitors are available but more capacitors are required to achieve equivalent ESR levels. Even though the Sanyo parts may be more expensive, the cost is offset by providing savings in board area and number of parts required. The particular part used is an 820-μF, 4-V capacitor with a specified maximum ESR of 12 mΩ, giving a total maximum ESR of 3 mΩ. These capacitors are C14, C15, C16, and C17 in Figure 4. For good design practice, C18–C21, four 10-μF ceramic capacitors, are placed in parallel with C14–C17. Ceramic capacitors are very effective for suppressing high frequency switching spikes and reducing the effects of the ESL of C14–C17.

To summarize, the output capacitance must be selected to provide a sufficiently low ESR. The capacitor(s) must have an adequate voltage rating for the particular application. In addition, the capacitor(s) must have an ample ripple current rating to handle the applied ripple current. This ripple current is dependent on the ripple current in the output inductance that is calculated in the next section. The RMS current in the output capacitance is calculated as follows:

$$I_{CRMS} = \Delta I_L \times \frac{\sqrt{3}}{6} = \Delta I_L \times 0.289 = 10.6\ A \times 0.289 = 2.9\ A_{RMS}$$

Where ΔI_L is the peak-to-peak ripple current in the output inductor.

The ripple current rating for one of these capacitors is 5.04 A RMS at 45°C and is reduced to 3.53 A RMS at 85°C. Using linear interpolation to get an estimate for the rating at 60°C, gives a rating of 4.47 A RMS for each capacitor. The total ripple current rating for the output capacitance is $4 \times 4.47 = 17.9$ A RMS.

4.3.2 Output Inductance

The output filter inductance is the next quantity to be determined. Like the output capacitance selection, the primary consideration is providing satisfactory response to a fast load transient.

The inductance affects the output voltage response to transient loads by governing the rate at which its current can increase (or decrease). For example, during a load transient where the output current increases from no load to full load, the output capacitor supplies all of the output current until the inductor current has time to increase to full load. So, a relatively small inductance is desired.

On the other hand, the inductance also plays a part in the power supply switching frequency, because the inductance limits how fast the output voltage traverses through the hysteresis band. As the inductance decreases, the output voltage changes faster, giving rise to higher switching frequencies.

Therefore, the inductor value is fairly critical and should be stable over the expected load and temperature range. Care should be exercised in the inductance selection because design requirements for hysteretic regulators are different from PWM controlled converters. Recall that for a fixed frequency PWM controlled buck converter, for a given operating point, the output inductance governs the peak-to-peak amplitude and the slope (di/dt) of the inductor current. In a hysteretic regulator, the ripple current is set by the output voltage ripple setting and the output capacitance impedance.

Other important factors to be considered when designing or selecting the inductor are current capability, allowable operating frequency, and DC resistance.

After choosing an initial inductance value, the power supply switching frequency must be estimated to insure that it is within the desired range. The switching frequency for the example design given in Figure 4 is nominally 125 kHz. A detailed analysis of the switching frequency and an equation to predict it is given later.

To calculate the maximum inductance allowed for a given response time, load step, and operating point, the following simple relationship is used:

$$V_L = L \times \frac{I_{TRAN}}{\Delta t} \Rightarrow L \leq \frac{V_L}{I_{TRAN}} \times \Delta t$$

Where:

V_L= the voltage applied across the output inductor,
I_{TRAN} = the magnitude of the load step, and
Δt = the desired response time.

For a load step from light load to heavy load, the voltage applied across the inductor can be assumed to be $V_I - V_O$. This also assumes that the duty cycle is 100% as the output voltage is corrected. Alternatively, for a load step from heavy load to light load, the voltage across the inductor can be assumed to be V_O. This assumes that the duty cycle is 0% as the output voltage is corrected.

For the example circuit described here, the condition which gives the smallest inductor value is a load step from heavy load to light load. This is because the voltage applied to the output inductor is the lowest, i.e., the output voltage. For this case, allowing 15 μs for the inductor current to change, an inductance value is calculated as follows:

$$L \leq \frac{V_L}{I_{TRAN}} \times \Delta t = \frac{2}{20} \times 15 \times 10^{-6} = 1.5\ \mu H$$

For convenience, a 1.2-μH inductor was designed for this circuit. Figures 8 and 9 illustrate satisfactory transient load performance for the output filter values selected in this and the previous sections.

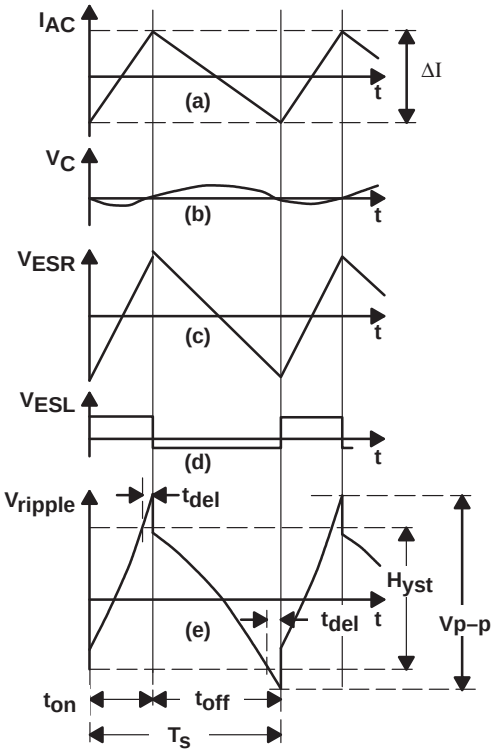
4.4 Switching Frequency Analysis

After the elements of the output filter are determined, the power supply switching frequency must be estimated. If the estimated switching frequency is too high, the switching losses in the power MOSFETs will be high, resulting in less than optimum efficiency. If the estimated switching frequency is too low, the inductor value may be too high, resulting in unsatisfactory transient response. A switching frequency outside the desired range should be corrected by changing either the output ripple setting, the output capacitance, or the output inductance.

To accurately predict the switching frequency of a hysteretic regulator, the output voltage ripple must be investigated. This should be expected, since the power supply switching instants are based upon the state of the output voltage. A simple and accurate method of determining the switching frequency is described below.

4.4.1 Output Ripple

The three elements of the capacitor that contribute to ripple are ESR, ESL, and capacitance. Assume that all three elements are in series and there are no other parasitic components to consider. Figure 13 shows the voltage waveforms across each component of the output capacitor and the corresponding equations.



(a) **Current waveform through output capacitor**

(b) **Voltage waveform across ideal capacitor with initial value at beginning of high-side MOSFET on-time**

High-side MOSFET ON

$$V_C = \frac{\Delta I \times t^2}{2 \times Co \times D \times Ts} - \frac{\Delta I \times t}{2 \times Co}$$

High-side MOSFET OFF

$$V_C = \frac{\Delta I \times t}{2 \times Co} - \frac{\Delta I \times t^2}{2 \times Co \times (1-D) \times Ts}$$

(c) **Voltage waveform across ESR**

High-side MOSFET ON

$$V_{ESR} = ESR \times \frac{\Delta I \times t}{D \times Ts} - \frac{\Delta I}{2}$$

High-side MOSFET OFF

$$V_{ESR} = ESR \times \frac{\Delta I}{2} - \frac{\Delta I \times t}{(1-D) \times Ts}$$

(d) **Voltage waveform across ESL**

High-side MOSFET ON

$$V_{ESL} = \frac{ESL \times \Delta I}{D \times Ts}$$

High-side MOSFET OFF

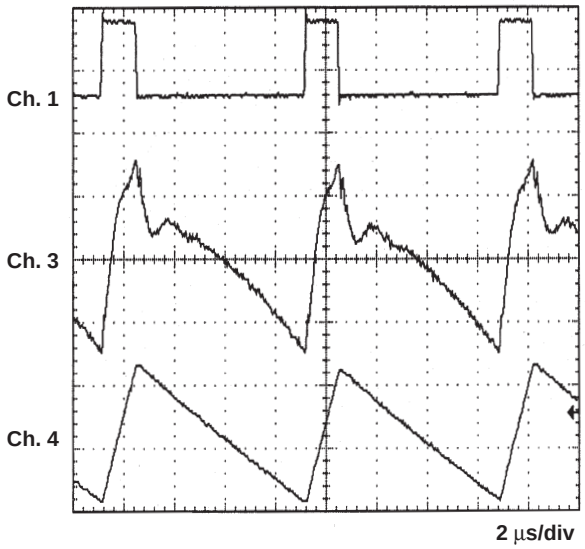
$$V_{ESL} = -\frac{ESL \times \Delta I}{(1-D) \times Ts}$$

(e) **Composite output voltage ripple waveform**

$$V_{ripple} = V_C + V_{ESR} + V_{ESL}$$

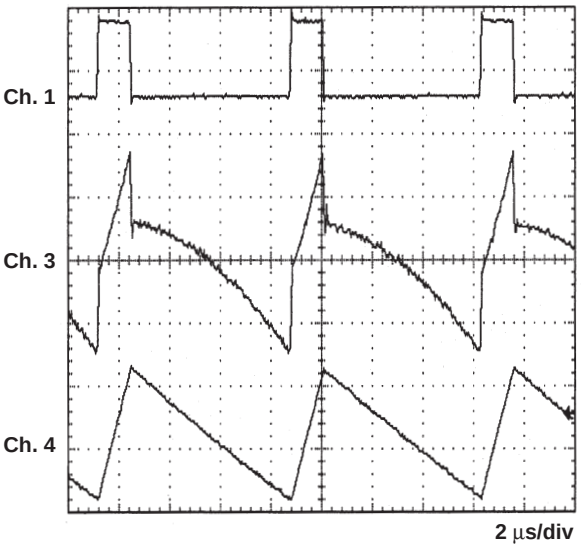
Figure 13. Output Ripple Voltage Detail

Figure 14 shows the phase voltage (voltage at junction of high-side MOSFET with low-side MOSFET), output voltage, and inductor current waveforms for the example circuit of Figure 4. The output voltage waveform is slightly different from the theoretical waveform of Figure 3 due to the smoothing effect of the four 10-μF ceramic capacitors in parallel with the OS-CON electrolytic capacitors. Some resonance due to the ceramic and electrolytic capacitors is also noticeable as the voltage begins to drop. Figure 15 demonstrates how the waveforms, with the ceramic capacitors removed, closely resemble the theoretical waveforms of Figure 3. The waveforms are very similar to ideal waveforms, and the ESL, ESR, and capacitive effects are noticeable.



Ch. 1: Voltage at the junction of high-side MOSFETs and low-side MOSFETs (10 mV/div)
Ch. 3: Output ripple voltage (10 mV/div)
Ch. 4: Output inductor current (5 A/div)

Figure 14. Output Voltage Ripple With 4 × 10 μF Ceramic Capacitors



Ch. 1: Voltage at the junction of high-side MOSFETs and low-side MOSFETs (10 mV/div)
Ch. 3: Output ripple voltage (10 mV/div)
Ch. 4: Output inductor current (5 A/div)

Figure 15. Output Voltage Ripple Without 4 × 10 μF Ceramic Capacitors

4.4.2 Switching Frequency Equation

Assume that the input and output voltage ripple magnitudes are relatively negligible compared to the dc component. Also assume that the time constant $L/(R_{DS(on)} + R_L)$, where L is the output inductance, R_L is the inductor resistance and $R_{DS(on)}$ is the on-state resistance of the high-side MOSFET(s), is high in comparison with the switching period. Assume the body diode conduction time and switching transition time are much smaller than the switching period. These assumptions are reasonable for low voltage ripple and high efficiency regulators. In such a case the output inductor current can be modeled as the sum of the dc component, which is equal to the output current *Io*, and the ac linear ramp component, which flows through the output capacitor (Figure 13).

The numbered equations in this section are used to derive the switching frequency equation.

Peak to peak value of the inductor current ΔI is given by the following equation:

$$\Delta I = \frac{V_I - Io \times \left(R_{DS(on)} + R_L\right) - V_O}{L} \times D \times Ts \quad (1)$$

Where:

V_I =the input voltage
V_O = the output voltage
Ts = the switching period

$D = \frac{V_O + Io \times \left(R_{DS(on)} + R_L\right)}{V_I}$ is the duty cycle which is defined as : $D = \frac{t_{ON}}{Ts}$ and t_{ON} is the on time of the high-side MOSFET.

Referring to Figure 13 (e), the output voltage ripple, V_{p-p}, is higher than the hysteresis band, *Hyst,* because of the delays, t_{del}, that were described in Section 2. Assume that delays for both switching instants are equal for simplicity. The ideal capacitor voltage component has the same initial value during switching instants t_{ON} and $(Ts–t_{ON})$ (see Figure 13 (b)). In this case the voltage V_{p-p} is:

$$V_{p-p} = \frac{ESL}{L} \times V_I + \Delta I \times ESR \quad (2)$$

On the other hand, the hysteresis band is equal to the difference between the peak-peak values of the V_O ripple, $v_{ripple,}$ at the moments $t_{ON} - t_{del}$ and $t_{OFF} - t_{del}$

$$Hyst = V_{ripple}\left(t_{ON}–t_{del}\right)–V_{ripple}\left(t_{OFF}–t_{del}\right) \quad (3)$$

After substituting equation (1) into equations for v_C, v_{ESR} and v_{ESL} (Figure13) and using equations (2) and (3), the following equation for the switching frequency, f_S, can be derived:

$$f_s = \frac{V_O \times \left(V_I - V_O\right) \times \left(ESR–t_{del} / Co\right)}{V_I \times \left(V_I \times ESR \times t_{del} + Hyst \times L–ESL \times V_I\right)} \quad (4)$$

Equation (4) shows that the switching frequency strongly depends on *ESR* and *ESL*. It is important that *ESL* meet the following condition:

$$ESL < \left(ESR \times t_{del} + Hyst \times L \times D / Vout\right)$$

If it does not, the voltage step across the ESL during switching exceeds the hysteresis window, and the switching frequency becomes too high and uncontrollable.

The switching frequency does not depend on the load current in equation (4), because a synchronous regulator has the same two stages of operation during the switching period over the load current range, including no load condition. There is no discontinuous mode operation at very light loads. In reality there is a weak dependence of the switching frequency on the load current because of power losses and additional voltage drops through non-ideal components. Equation (4) should be sufficiently accurate for the first frequency estimate at the beginning of a design.

Figure 16 gives theoretical estimate and measurement results of the frequency for the example circuit of Figure 4 without the four 10-μF ceramic decoupling capacitors (C18–C21), under no-load and 20-A load conditions. There is good agreement with theoretical and measured results; the maximum difference is less than 7%. Four Os-Con 820-μF, 4-V capacitors were used in this example circuit. The measured values for ESR and ESL for each capacitor were 8 mΩ, and 4.8 nH, respectively, using an impedance analyzer with lead length error compensation. Since there are four capacitors in parallel, these values were divided by four and substituted in equation (4). The other values that were substituted in equation (4) are the following:

L = 1.2 μH; R_L, = 11 $m\Omega$; $Hyst$ = 20.25 mV, t_{del} = 570 ns.

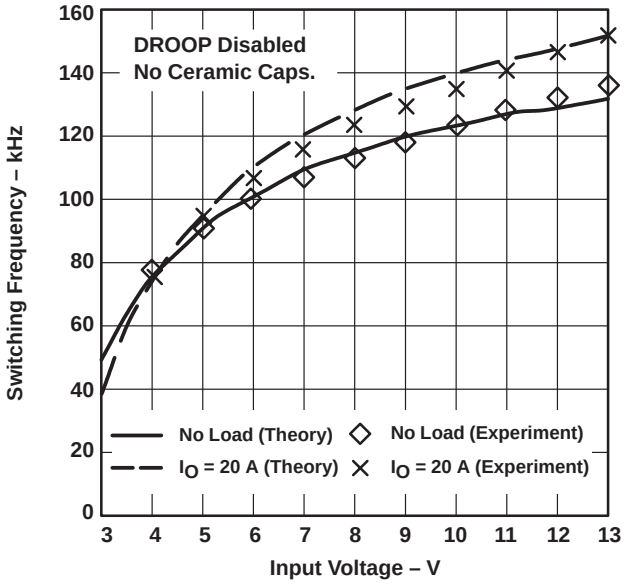


Figure 16. Switching Frequency vs Input Voltage

The switching frequency was also measured with the 4 × 10 μF ceramic capacitors (C18–C21) in the example circuit of Figure 4. Comparison results with and without ceramics are given in Figure 17. For low input voltages, the switching frequencies are about the same. For V_I ranging between 7 V and 11 V, the frequency is lower with ceramics because the resonant period between ceramics and the OS-CON capacitors is close to the on-time of the converter, resulting in a longer on-time; the off-time increases to regulate V_O to the correct value, causing a decrease in switching frequency. Adding decoupling ceramic capacitors decreases ESL from 1.2 nH to 0.8 nH; consequently, decreasing the switching frequency.

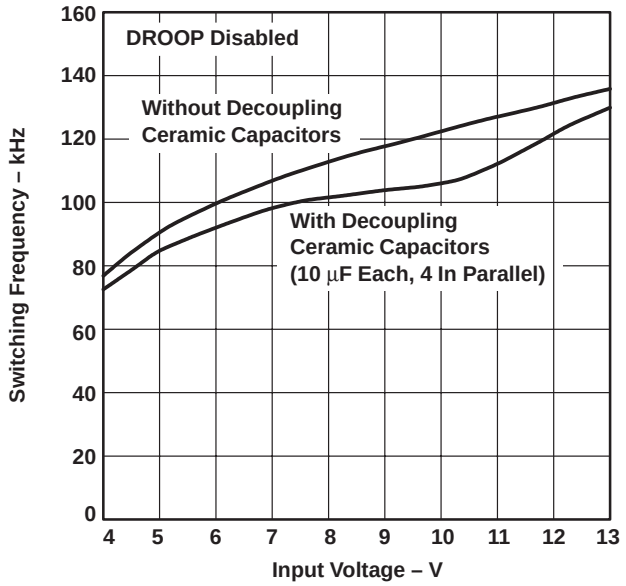


Figure 17. Switching Frequency With and Without Ceramic Capacitors

Theoretical output voltage waveforms based on the frequency calculation were obtained using Mathcad™ software (Figure 18). These calculations are very close to the experimental waveforms measured without decoupling capacitors (Figure 19).

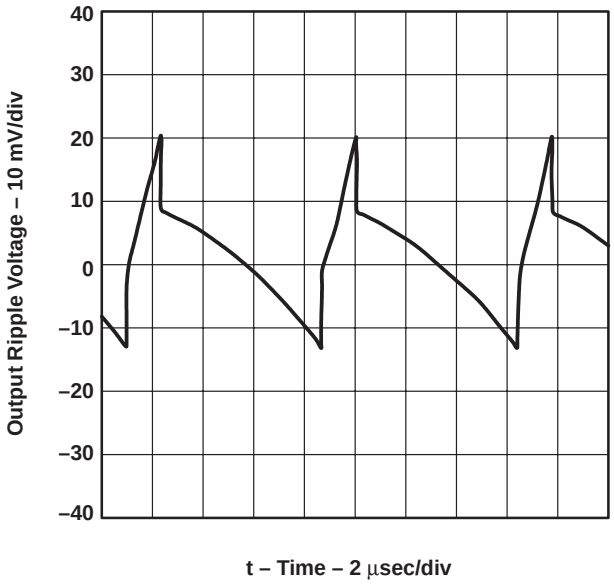
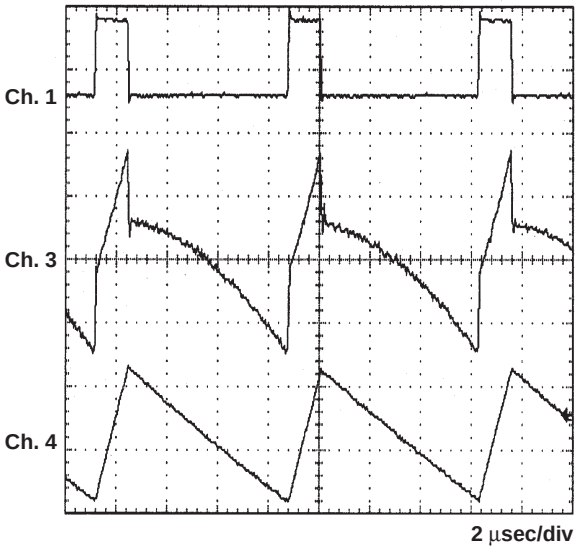


Figure 18. Theoretical Output Ripple Waveform



Ch. 1: Voltage at the junction of high-side MOSFETs and low-side MOSFETs (10 mV/div)
Ch. 3: Output ripple voltage (10 mV/div)
Ch. 4: Output load current (5 A/div)

Figure 19. Measured Output Ripple Waveform

4.5 Power MOSFET Selection

The TPS5210 is designed to drive N-channel power MOSFETs in a synchronous rectifier configuration. The MOSFET chosen for this design is the Siliconix Si4410DY. This device is chosen for its low $r_{DS(on)}$ of 13.5 mΩ and drain-to-source breakdown voltage rating of 30 V. In addition, to reduce power dissipation, two power MOSFETs (Q1 and Q2) are paralleled for the high-side switch and three power MOSFETs (Q4, Q5, and Q6) are paralleled for the low-side switch.

Power dissipation for the switching MOSFETs, which includes both conduction and switching losses, is given by:

$$P_{D\,(Q1-Q2)} = \left(I_D^2 \times r_{DS(on)} \times D\right) + \left(0.5 \times V_i \times I_D \times t_{r+f} \times f_{sw}\right)$$

$$P_{D\,(Q4-Q6)} = \left(I_D^2 \times r_{DS(on)} \times (1-D)\right) + \left(0.5 \times V_i \times I_D \times t_{r+f} \times f_{sw}\right)$$

An example MOSFET power dissipation calculation for Q1 and Q3 is shown below with the following assumptions:

The total switching time, t_{r+f} = 100 ns,
An $r_{DS\,(on)}$ high temperature adjustment factor = 1.4,
A 60°C maximum ambient temperature,
V_I = 12.0 V, V_O = 2 V, and I_O = 20 A then :

$$P_{D\,(Q1)} = \left(\frac{20.0}{2}\right)^2 \times (0.0135 \times 1.4) \times 0.18 + 0.5 \times 12 \times \left(\frac{20}{2}\right) \times 100 \times 10^{-9} \times 125\ kHz = 0.34 + 0.75 = 1.09\ W$$

$$P_{D\,(Q4)} = \left(\frac{20}{3}\right)^2 \times (0.0135 \times 1.4) \times 0.82 + 0.5 \times 12 \times \left(\frac{20}{3}\right) \times 100 \times 10^{-9} \times 125\ kHz = 0.69 + 0.50 = 1.19\ W$$

The thermal impedance of these devices, $R_{\theta JA}$ = 90°C/W for FR-4 with 2-oz. copper and a one-inch-square pattern, thus:

$$T_{J\,(Q1)} = T_A + \left(R_{\theta J-A} \times P_D\right) = 60 + (50 \times 0.90) = 115°C$$

$$T_{J\,(Q3)} = T_A + \left(R_{\theta J-A} \times P_D\right) = 60 + (50 \times 1.19) = 120°C$$

It is good design practice to check power dissipation at the extreme limits of input voltage to find the worst case.

The total losses in both the high-side switches (2 in parallel) and low-side switches (3 in parallel) can simply be summed up as follows:

$$P_{D(Total)} = (2) \times (1.09\ W) + (3) \times (1.19\ W) = 5.75\ W$$

5 TPS5210 Functions

The functional block diagram of the TPS5210 is given in Figure 20. The controller has the following main features:

- VID/DAC that conforms to Intel's VRM8.3 specification; reference levels between 1.8 V and 1.3 V decremented by 50 mV, and 3.5 V to 2.1 V decremented by 0.1 V.
- 1% reference over 0°C to125°C junction temperature range for reference voltages between1.3 V and 2.5 V.
- Synchronous-buck gate drivers with adaptive deadtime control
- High-side MOSFET driver voltage rating of 30 V
- MOSFET driver peak current rating of 2 A
- Hysteretic comparator: 250 ns propagation delay to gate driver outputs, 2.5 mV offset voltage, symmetrical hysteresis, hysteresis setting is a percentage of Vref.
- Lossless output current sensing circuit
- Accurate, fast droop compensation circuit
- Slowstart circuit; slowstart time independent of VID setting
- Internal 8 V drive regulator for reduced gate charge power losses
- POWERGOOD comparator, 93% of Vref trip
- UVLO, Vcc undervoltage lockout, 10 V start, 2 V hysteresis
- INHIBIT comparator that can also monitor UVLO of the system logic supply, 2.1 V start, 100 mV hysteresis.
- Latched overcurrent shutdown circuit
- Latched overvoltage shutdown circuit
- LODRV pin that activates the low-side MOSFETs as a crowbar to protect against a short across the high-side MOSFETs.

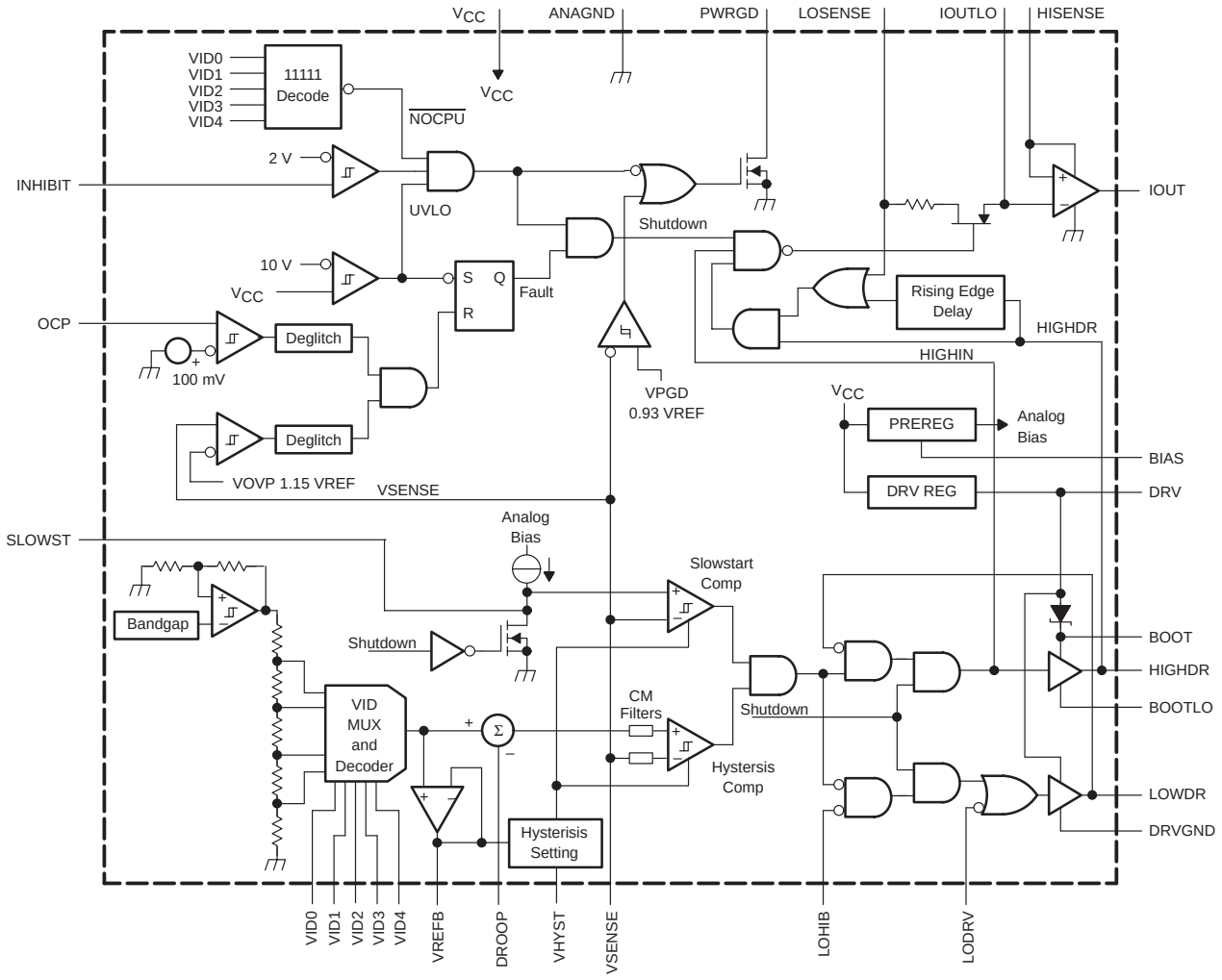


Figure 20. TPS5210 Functional Block Diagram

This section describes the functions governed by the TPS5210. A procedure is given to determine the values of components used in the example design given in Figure 4. Example calculations accompany the design equations. There are many possible ways to proceed when designing power supplies and some iteration may be necessary when actual performance differs from design predictions. Reference designators refer to the circuit in Figure 4.

5.1 V_{CC} Undervoltage Lockout

The V_{CC} undervoltage lockout circuit disables the controller while V_{CC} is below the 10-V start threshold during power-up. While the controller is disabled, the output drivers will be low and the slowstart capacitor will be shorted. When V_{CC} exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2-V hysteresis in the undervoltage lockout circuit for noise immunity.

5.2 Inhibit

The inhibit circuit is a comparator with a 2.1-V start voltage and a 100-mV hysteresis. When inhibit is low, the output drivers are low and the slowstart capacitor is discharged. When inhibit is above the start threshold, the short across the slowstart capacitor is released and normal operation begins.

When the system logic supply is connected to the inhibit pin, the inhibit pin also controls power sequencing by locking out controller operation until the system logic supply exceeds the input threshold voltage of the inhibit circuit; thus, the 12-V supply and the system logic supply (either 5 V or 3.3 V) must be above UVLO thresholds before the controller is allowed to start up.

In applications that derive main power from 5 V or 3.3 V for the power stage, the inhibit circuit can be the UVLO circuit for the main power supply.

5.3 Slowstart Design

Slowstart or soft-start is added to reduce power-up transients. Without slowstart, when input power is first applied, the TPS5210 attempts to raise the output voltage (initially zero) to its normal operating level by turning on the top MOSFET until the voltage is approximately Vref. This can cause high transient currents to flow in the output inductor and output capacitor. Although this form of startup usually does not cause component failures, it does apply stresses much greater than those typically encountered in normal operation. It is good design practice to include slowstart circuitry to avoid these unnecessary stresses.

The slowstart circuit in the TPS5210 controls the rate at which the output voltage powers up. A capacitor, C26, connected between SLOWST (pin 8) and ANAGND (pin 7), is charged by an internal current source. This current source is proportional to the reference voltage and is adjustable by an external resistance selected by the user. The output voltage follows the voltage on the slowstart capacitor during startup. Since the charging current is proportional to the reference voltage, the slowstart time is independent of the reference voltage for a given resistor value.

Choices of the slowstart time and the slowstart capacitor value are largely arbitrary as long as system startup time requirements are met. For this example design, a slowstart time of 10 ms is chosen, and the slowstart capacitor is chosen to be 0.1 μF. Therefore, to charge 0.1 μF from zero volts to 2 V in 10 ms, the following equation holds:

$$I_{SLOWSTART} = C_{SLOWSTART} \times \frac{\Delta V_C}{\Delta t_{ss}} = 0.1\ \mu F \times \frac{2\ V}{10\ ms} = 20\ \mu A$$

The slowstart charging current is determined by the following equation:

$$I_{SLOWSTART} = \frac{I(VREFB)}{5}$$

where I(VREFB) = the current out of VREFB (pin 5).

For an $I_{SLOWSTART}$ current equal to 20 μA, I(VREFB) should be set to:

$$I(VREFB) = 5 \times I_{SLOWSTART} = 5 \times 20\ \mu A = 100\ \mu A$$

The voltage on VREFB (pin 5) is a buffered reference voltage from the output of the VID network. For this design, the VID inputs are driven to produce a reference (and output) voltage of 2 V.[4] The resistance from the VREFB pin to ANAGND can be calculated as:

$$R_{VREFB} = \frac{2\ V}{100\ \mu A} = 20\ k\Omega$$

This value is used to determine the values of R13 and R14 that set the hysteresis level.

The equations above can be used to derive a simplified relationship for the slowstart time as shown:

$$t_{SLOWSTART} = 5 \times C_{SLOWSTART} \times R_{VREFB}$$

V_O start-up waveforms for different VID (and reference voltage) settings are given in Figure 21, showing that slowstart time is independent of the VID setting.

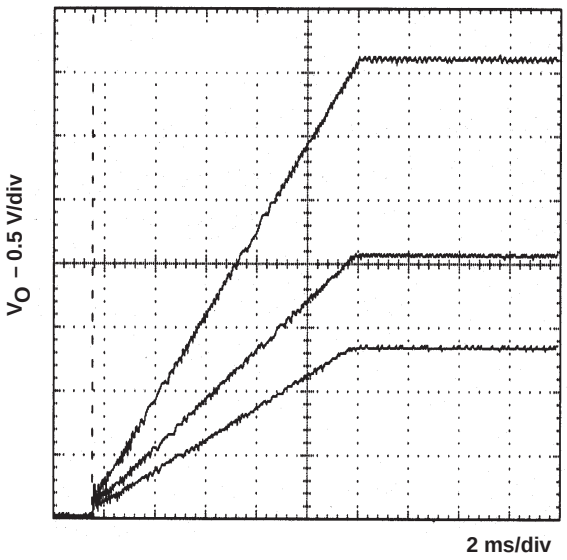


Figure 21. Output Voltage Slowstart at 1.3 V, 2 V, 3.5 V Settings

5.4 Hysteresis Setting

The next step in this design is choosing the desired output voltage ripple. As a first approximation, the output voltage ripple is simply the difference between the two levels (V_{LO} and V_{Hi}) shown in Figure 2. The hysteresis setting of the hysteresis comparator of the TPS5210 sets these two levels. The hysteresis is set by two external resistors and is centered around VREF (pin 5). The hysteretic comparator is designed with low input offset voltage (±2.5 mV max) low propagation delays (250ns max to gate driver outputs with 10mV overdrive) and accurate hysteresis setting (±3.5 mV max). The hysteresis is proportional to the reference voltage; programming Vref to a new value automatically adjusts the hysteresis to be the same percentage of Vref.

To accurately choose the output voltage ripple, all of the propagation delays must be considered. The first step is to calculate the amount of ripple expected due to the delays, in addition to the ripple set by the hysteresis comparator. Using the terminology of Section 4.4.1, this additional ripple is equal to V_{p-p} – Hyst and will be referred to V_{del} for ease of reference. Or:

$$V_{p\text{-}p} = Hyst + V_{del}$$

Where:

V_{p-p} =the total output ripple,
Hyst = the hysteresis setting of the hysteretic comparator, and
V_{del} = the output ripple exceeding Hyst and due to all propagation delays.

Assuming the output ripple during the delay time is primarily caused by the inductor ripple current flowing through the output capacitors' ESR, the additional ripple, V_{del}, can be estimated as:

$$V_{del} = \left[\frac{V_I - V_O}{L} \times t_{del}\right] \times ESR + \left[\frac{V_O}{L} \times t_{del}\right] \times ESR$$

To calculate V_{del} for this example design, use the measured components given in Section 4.4.2. They are repeated here for convenience:

L = 1.2 μH
ESR = 2 mΩ
T_{del} = 570 ns

Now calculate V_{del}:

$$V_{del} = \left[\frac{12-2}{1.2 \times 10^{-6}} \times 570 \times 10^{-9}\right] \times 0.002 + \left[\frac{2}{1.2 \times 10^{-6}} \times 570 \times 10^{-9}\right]$$

$$\times 0.002 = 11.4\ mV$$

Since the total output voltage ripple was set to 35 mV in Table 2 of Section 4, the hysteresis needs to be set for 35 mV – 11.4 mV = 23.6 mV. For convenience, and allowing a little margin, the hysteresis will be designed for 20 mV.

To set the hysteresis, connect two external resistors to form a resistor divider from VREFB (pin 5) to ANAGND (pin 7) with the center of the divider connected to VHYST (pin 4). The hysteresis of the comparator is equal to twice the voltage that is between the VREFB (pin 5) and VHYST (pin 4) pins. Or,

$$V_{Hysteresis} = 2 \times (VREFB - VHYST)$$

For this design, 20 mV of hysteresis was chosen for a 2.0 V output voltage.

$$V_{Hysteresis} = 20\ mV = 2 \times (2\ V - VHYST)$$

Solving for VHYST:

$$VHYST = VREFB - \frac{V_{Hysteresis}}{2} = 2 - \frac{20\ mV}{2} = 1.99\ V$$

Referring to the schematic, Figure 4, the two external resistors are R13 and R14. From the previous section, the total resistance required is 20 kΩ. Since R13 is very small compared to R14, for simplicity set R14 = 20 kΩ. To calculate the value of R13:

$$VHYST = VREFB \times \frac{R14}{R14 + R13}$$

Solving for R10:

$$R13 = \frac{VREFB \times R14}{VHYST} - R14 = \frac{(2\ V)\ (20\ k\Omega)}{1.99\ V} - 20\ k\Omega = 100\ \Omega$$

The controller hysteresis is now set to 20 mV. This, in addition to the 11.4 mV due to propagation delays, results in a total ripple voltage of less than the design goal of 35 mV.

5.5 Noise Suppression

Hysteretic regulators, by nature have a fast response time to V_O transients and are thus inherently noise sensitive due to the very high bandwidth of the controller. Noise suppression circuits were added to the TPS5210 to improve the noise immunity, as shown in Figure 22. Internal low-pass filters with a pole frequency of 5 MHz were added to the inputs of the hysteretic comparator. These low-pass filters are referenced to the same analog ground as the hysteretic comparator. There is a common-mode filter with a 4-MHz pole between VREFB and VHYST to filter out noise between these pins. A double pulse suppression circuit prohibits spurious pulses from propagating to the gate drivers. The double pulse suppression circuit becomes active when the comparator has toggled or when the LOHIB pin (which is connected to the power MOSFETs) has transitioned, providing additional noise immunity from internally and externally generated noise. The suppression circuit is active for 150 ns.

A low-pass filter is recommended between V_O and the VSENSE pin (R1 and C3 in Figure 22); recommended values are 150 ohms and 1 nF. This low-pass filter is included in the evaluation design of Figure 4 (R12, R15, and C25). In addition to providing low-pass filtering, a resistive divider offsets the output voltage from VREF and is discussed in the droop compensation section (Section 5.8).

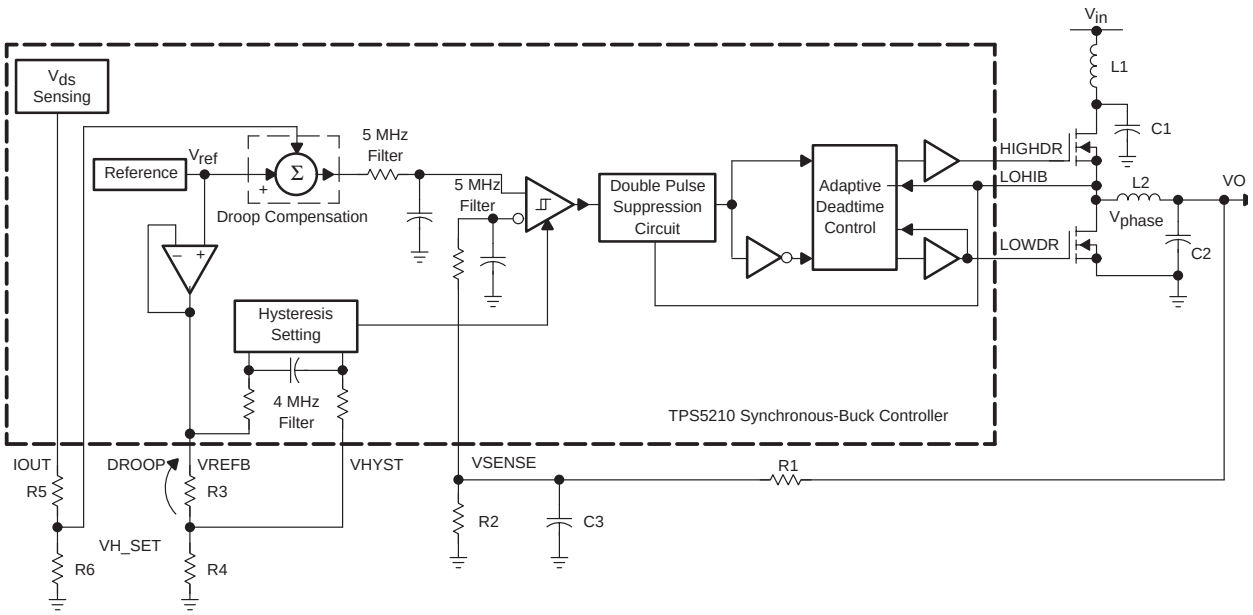


Figure 22. Block Diagram Showing Noise Suppression Circuits

5.6 Overcurrent Protection

Overcurrent protection is provided by measuring the on-state voltage of the high-side MOSFETs, conditioning the measured voltage, and comparing the result to a reference voltage. If the output current exceeds the current limit setpoint, a fault latch is set and the output drivers are turned off. Vcc (12 V) must be reduced to below the undervoltage lockout value to restart the converter.

A sample-and-hold circuit measures the power supply output current by sensing the on-state drain-to-source voltage of the high-side MOSFETs (Q1 and Q2 Figure 4). This arrangement improves efficiency over solutions having a separate current sensing resistor. The drains of the high-side MOSFETs are connected to HISENSE (pin 19). The sources of the high-side MOSFETs are connected to LOSENSE (pin 20). When the high-side MOSFETs are on, a TPS5210 internal switch is also on and samples the source voltage of the high-side MOSFETs. This sampled voltage is applied to IOUTLO (pin 21) and is held by the external 0.033-µF capacitor, C32, which is connected from IOUTLO (pin 21) to HISENSE (pin 19). The TPS5210 amplifies (gain=2) the sampled-and-held voltage on C32 and sends the output voltage to IOUT (pin 1).

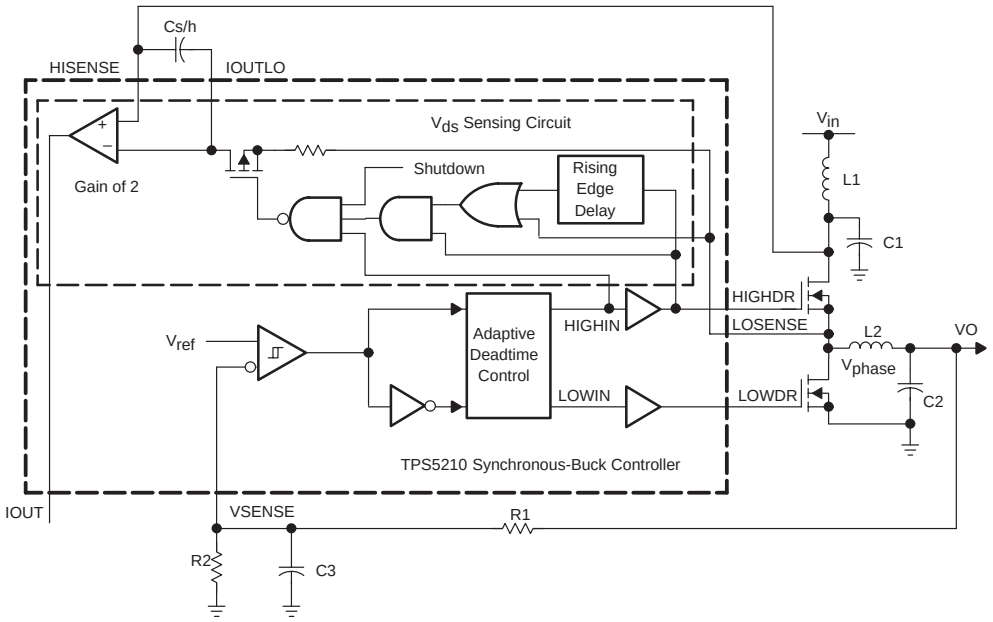


Figure 23. V_{DS} Sensing Circuit

Figure 23 gives a simple block diagram of the Vds sensing circuit. The Vds sensing circuit measures the average voltage across the high-side MOSFET when the high-side MOSFET is on, and holds that value on a sample/hold capacitor when the high-side MOSFET is off. The voltage on the sample/hold capacitor is directly proportional to the load current. Sensing across the high-side MOSFET rather than the low-side MOSFET ensures that shorted loads can be detected. The RC time constant of the sample/hold network must be greater than the conduction-time of the high-side MOSFET, otherwise the sample/hold circuit will function as a peak detector circuit and will not hold the average Vds voltage. The differential voltage across the sample/hold capacitor is amplified by 2 and converted to a single-ended signal on the IOUT pin. The DC CMRR of the Vds sensing amplifier is 69 dB minimum. Added logic ensures that sampling begins and ends while the high-side MOSFET is conducting. The turn-on and turn-off delays of the sample/hold switch are less than 100 ns. Additional logic and a rising edge delay circuit are included to guarantee sampling during a short-to-ground fault across the low-side MOSFET; the rising edge delay time is 500 ns. Figure 24 shows waveforms of the Vds sensing circuit; the 2-µs RC time constant of the sample/hold circuit is less than the conduction time of the high-side MOSFET to more clearly illustrate the ripple waveform on the sample/hold capacitor. Viout lags V(Cs/h) by 1 µs due to the response time of the Vds sensing amplifier.

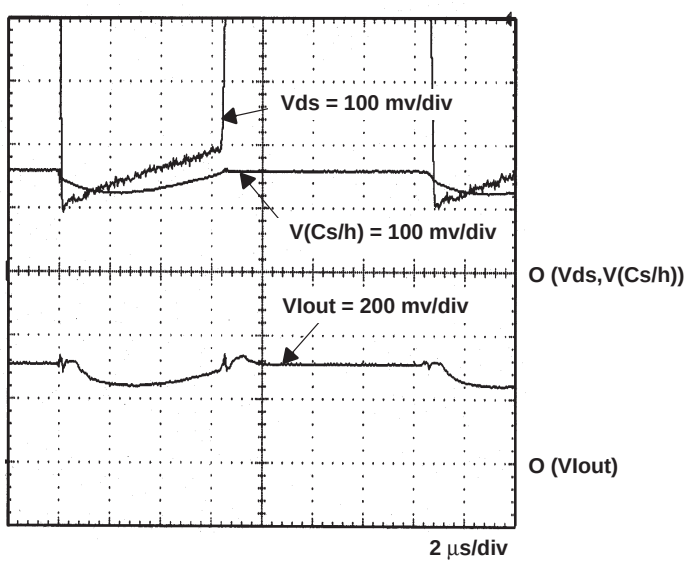


Figure 24. V_{DS} Sensing Waveforms

Resistors R8 and R9 in Figure 4 set the current limit setpoint. A resistor-divider network (R8 and R9, Figure 4) applies the IOUT output voltage to OCP (pin 3). The resistor-divider network is designed so that the voltage applied to OCP is 100 mV for the desired output current limit point. If the voltage on OCP exceeds 100 mV, a fault latch is set and the output drivers are turned off. The latch remains set until VCC (pin 15) goes below the undervoltage lockout value.

The following equations summarize the relationships discussed above.

The on state drain-to-source voltage of the high-side MOSFETs, Q1 and Q2, is:

$$\left(V_{HISENSE} - V_{IOUTLO}\right) = I_O \times R_{DS(on)}$$

where $R_{DS(on)}$ is the value obtained from the two high-side MOSFETs in parallel and includes correction for elevated temperature if necessary.

The voltage difference, $V_{HISENSE} - V_{IOUTLO}$, is internally amplified by a fixed gain of two to produce the IOUT (pin 1) signal.

$$V_{IOUT} = \left(V_{HISENSE} - V_{IOUTLO}\right) \times 2$$

The V_{IOUT} signal is scaled for the desired current limit level and applied to the OCP pin:

$$V_{OCP} = V_{IOUT} \times \frac{R9}{R9 + R8}$$

Therefore, to set the power supply output current, first calculate the quantity $I_O \times R_{DS(on)}$ for the value of I_O desired for current limit. Variations in $R_{DS(on)}$, including its temperature dependence, should be considered, since this parameter can vary a significant amount for typical MOSFETs. Next, multiply this voltage by two. Finally, set the R8 and R9 voltage divider to produce 100 mV at the desired current limit point.

For this design, the maximum output current is 20 A. In most power supply designs, the exact current limit set point rarely needs to be very accurate. Limiting the current to a level that is not destructive is the main consideration. In this case, the nominal current limit is set for approximately 60% above the maximum, including an elevated temperature correction factor of 1.4 applied to a nominal $R_{DS(on)}$ of 11 mΩ. The current limit set point, I_{OCP}, is given by:

$$I_{OCP} = I_{O(Max)} \times 1.6 = 20 \times (1.6) = 32 \ Amps$$

For the above current level, V_{IOUT} is given by:

$$V_{IOUT} = \left(I_O \times R_{DS(on)}\right) \times 2 = \left(32 \ A \times \frac{0.011 \ \Omega \times 1.4}{2}\right) \times 2 = 0.49 \ V$$

Now, V_{OCP} is easily calculated:

$$V_{OCP} = V_{IOUT} \times \frac{R9}{R9 + R8} = 0.49 \ V \times \frac{1 \ k\Omega}{1 \ k\Omega + 3.9 \ k\Omega} = 0.1 \ V$$

In the above calculations, the nominal value for $R_{DS(on)}$ of 11 mΩ was used. Worst case analysis should always be performed to insure that current limit does not interfere with delivering maximum load.

An alternate current sensing scheme is to insert a current sense resistor in series with the drain of Q1. Higher accuracy may be obtained at the expense of lower efficiency.

5.7 Overvoltage Protection

If V_O exceeds Vref by 15%, a fault latch is set and the output gate drivers are turned off. The latch remains set until VCC (pin 15) goes below the undervoltage lockout value.

In addition to the standard OVP protection, the LODRV circuit is designed to protect the processor against overvoltages due to a short across the high-side power MOSFET. External components to sense an overvoltage condition are required to use this feature. When a shorted high-side MOSFET occurs, the low-side MOSFETs are used as a crowbar. LODRV is pulled low and the low-side MOSFET is turned on, overriding all control signals inside the controller. The crowbar action shorts the input supply to ground through the faulted high-side MOSFETs. A fuse in series with V_I must be added to disconnect the short-circuit.

5.8 Droop Compensation

The droop compensation network provides additional margin to maintain V_O within the load transient tolerance limits required by the processor. Under no-load conditions, V_O is programmed to a voltage greater than V_{REF} by an external resistor divider from V_O to VSENSE (R12 and R15 in Figure 4). This reduces the undershoot of V_O during a low-to-high load transient. The output voltage is programmed to decrease with an increase in load by the droop compensation network. The amount that the output voltage decreases from its no-load value is equal to the voltage applied to DROOP (pin 2). In order to cause the output voltage to be adjusted as a function of load, the voltage on IOUT (pin 1) is divided down with an external resistor divider, and connected to DROOP. So, for a high-to-low load transient, the overshoot is reduced by subtracting the voltage on DROOP from V_{REF}. Test results that illustrate the advantage of droop compensation during a transient load are shown in Section 3.2.3 in this application report.

The output voltage is increased from V_{REF} to:

$$V_{O(NL)} = V_{REF} \times \left(\frac{R15 + R12}{R15}\right) = 2\ V \times \left(\frac{10\ k\Omega + 150\ k\Omega}{10\ k\Omega}\right) = 2.03\ V$$

Using the procedure of the previous section, it is simple to calculate the voltage applied to the DROOP pin at a given load current. Assuming an ambient temperature of 25°C, an $R_{DS(on)}$ temperature correction factor (25°C) of 1.25, and a load current of 20 Amps, the VIOUT voltage is:

$$V_{IOUT} = \left(I_O \times R_{DS(on)}\right) \times 2 = \left(20\ A \times \frac{0.011\ \Omega \times 1.25}{2}\right) \times 2 = 0.275\ V$$

And the voltage applied to the DROOP pin is:

$$V_{DROOP} = V_{IOUT} \times \frac{R11}{R10 + R11} = 0.275\ V \times \frac{1\ k\Omega}{4.32\ k\Omega + 1\ k\Omega} = 0.052\ V$$

To summarize, the output voltage is set to 2.03 V at no-load (0 Amps) and is reduced to (2.03 – 0.052 =) 1.978 V at maximum load (20 Amps).

5.9 Power Good

The power-good circuit monitors for an undervoltage condition on V_O. If V_O drops below 93% of VREF, then the PWRGD is pulled low. PWRGD is an open-drain output and needs a pullup resistor.

5.10 Bias

Analog BIAS (pin 9), the output of the internal analog bias regulator, is designed to provide a quiet bias supply for the internal TPS5210 circuitry. External loads should not be driven by the bias regulator. A 1-µF capacitor, C27, is connected from BIAS to ANAGND.

5.11 Gate Drivers

The gate drivers were designed to drive large capacitive loads quickly and efficiently. Figure 25 is a block diagram of the drivers. The output stage of the drivers consists of bipolar and MOS transistors in parallel. The bipolar transistors provide the majority of the 2-A drive current. The driver outputs get pulled to ground (during sinking) or to the supply rail (during sourcing) by the MOS transistors. If the MOS transistors were not in the design, the voltage level on the driver outputs could only be driven to the saturation voltage level of the bipolar transistors. This could be a serious limitation, especially if logic-level power MOSFETs are used in the power stage, resulting in shoot-through current through the power MOSFETs.

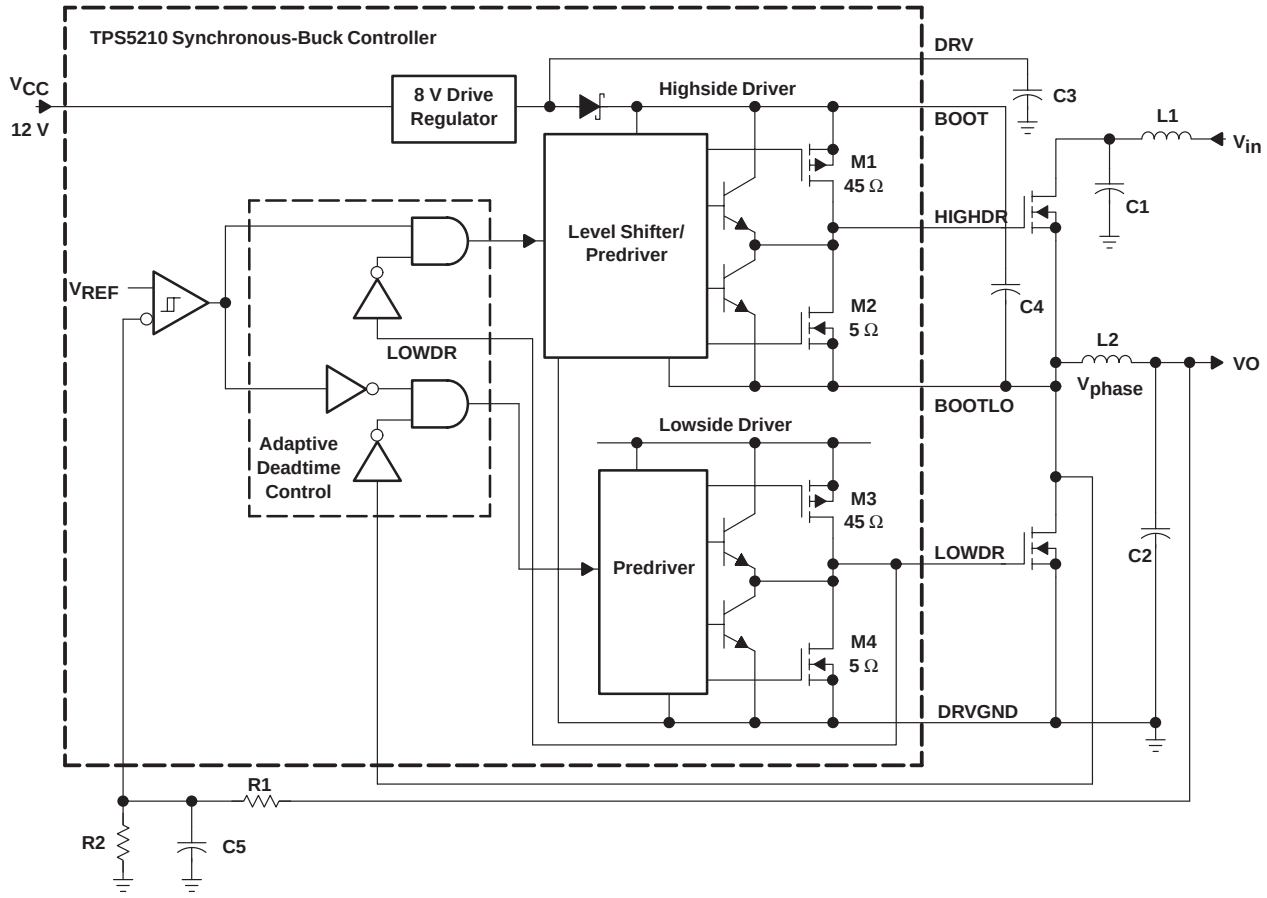


Figure 25. Gate Driver Block Diagram

Figure 26 gives an I–V sweep of the low-side driver during sinking. The Rds(on) of the MOS transistors for the sink stage is 5 Ω at T_J = 125°C and is 45 Ω for the source stage. The Rds(on) is lower for the sink stage to provide a low impedance path for the displacement current that flows through the Miller capacitance of the power MOSFET when the drain switches. This is especially important for the low-side driver to keep the low-side MOSFET off when the high-side MOSFET is turned on.

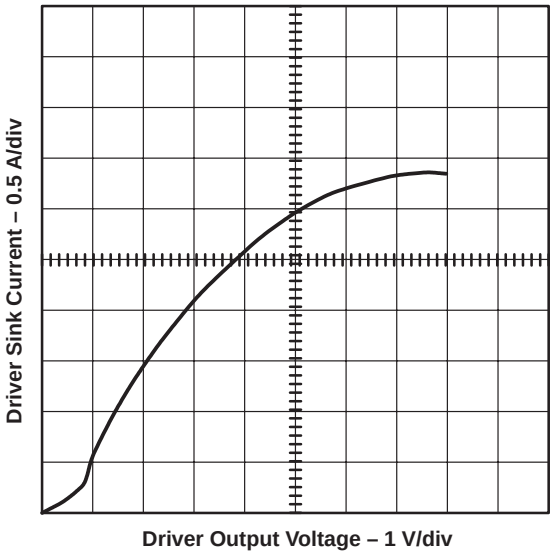


Figure 26. I–V Characteristic Curve for Low-Side Gate Drivers

The high-side gate driver is a bootstrap configuration with an internally integrated Schottky bootstrap diode. The voltage rating of the BOOT pin is 30 V. The gate drivers are biased from an internal 8-V drive regulator to minimize the gate drive power losses that are dissipated inside the TPS5210. As an example, the gate charge requirements for a Si4410 power MOSFET is 32 nC at a Vgs of 8 V, and is 49 nC at a Vgs of 12 V. If a system uses 6 Si4410s, and operates at 200 kHz, the total power dissipation within the controller for both cases will be:

8 V gate drive – 6×200 kHz $\times$ 32nC $\times$ 12 V = 0.46 watts

12 V gate drive – 6×200 kHz $\times$ 49nC $\times$ 12 V = 0.71 watts

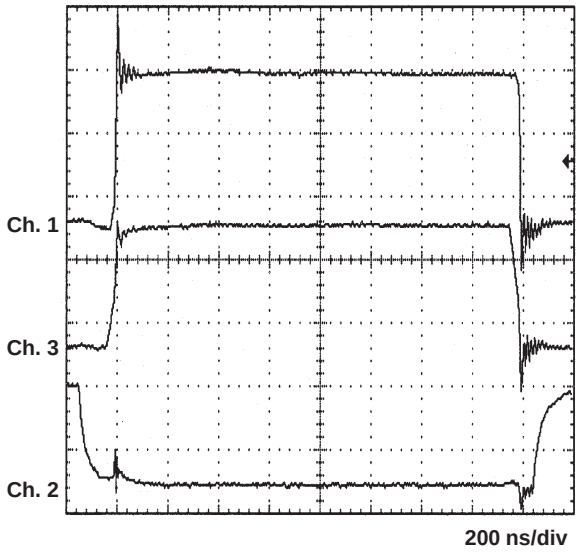
With a package θ_{JA} of 84°C/W, the TPS5210 will run 21°C hotter with a gate drive voltage of 12 V compared to 8 V, which can be a significant increase if the maximum ambient temperature is 70°C. The gate drivers have also been optimized to reduce the amount of internal shoot-through current, which will result when either the low-side or high-side driver is switching states.

The adaptive deadtime control minimizes the deadtime between conduction intervals of the power MOSFETs.

The low-side gate driver is not allowed to turn on until the Vphase voltage is below 2 V; the high-side gate driver is not allowed to turn on until the LOWDR pin falls below 2 V.

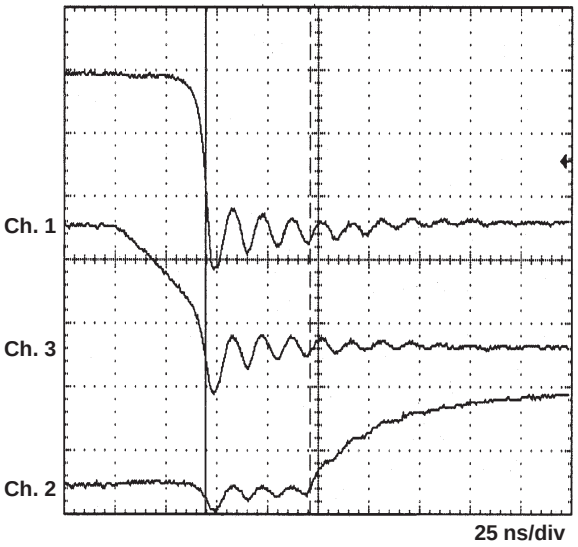
Figures 27, 28, and 29 show gate driver waveforms of the example design that is shown in Figure 4. In these figures, the high-side gate driver drives two Si4410s (Qg=64nC) and the low-side gate driver drives three Si4410s (Qg=96nC). Figure 27 shows the turn-on and turn-off of the high-side MOSFETs. Figure 28 shows 51.5 ns deadtime between the high-side MOSFETs turning off and the low-side MOSFETs turning on, measured from when phase voltage equals 2 V until gate of low-side MOSFETs begin to turn on. Figure 29 shows 69 ns deadtime between the low-side MOSFETs turning off and high-side MOSFETs turning on, measured from when the LOWDR pin falls to 2 V and the high-side MOSFET begins to turn on.

Fast switching and short dead times improve efficiency. There is 100-mA current limiting within the internal 8-V voltage regulator to protect the regulator and IC against a short fault on one of the driver pins.



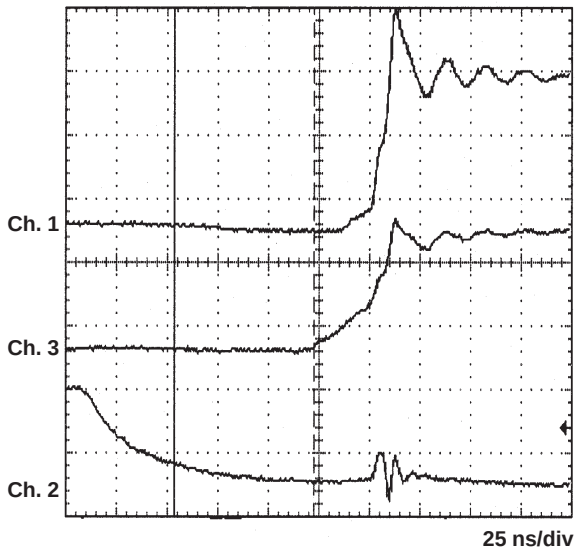
Ch. 1: Phase Voltage (Junction of high-side MOSFETs and low-side MOSFETs) (5 V/div)
Ch. 3: Gate voltage to ground of high-side MOSFET at HIGHDR pin, (10 V/div)
Ch. 2: Gate voltage to ground of low-side MOSFET at LOWDR pin, (5 V/div)

Figure 27. Switching Waveforms of Example Design



Ch. 1: Phase Voltage (Junction of high-side MOSFETs and low-side MOSFETs) (5 V/div)
Ch. 3: Gate voltage to ground of high-side MOSFET at HIGHDR pin, (10 V/div)
Ch. 2: Gate voltage to ground of low-side MOSFET at LOWDR pin, (5 V/div)

Figure 28. Expanded Turn-Off Switching Waveforms of Example Design



Ch. 1: Phase Voltage (Junction of high-side MOSFETs and low-side MOSFETs) (5 V/div)
Ch. 3: Gate voltage to ground of high-side MOSFET at HIGHDR pin, (10 V/div)
Ch. 2: Gate voltage to ground of low-side MOSFET at LOWDR pin, (5 V/div)

Figure 29. Expanded Turn-On Switching Waveforms of Example Design

5.11.1 Low-Side Driver Controls

The TPS5210 contains two control inputs to control the low-side MOSFET drive for various applications. They are LODRV (pin 10) and LOHIB (pin 11).

LODRV (pin 10) is an enable input for the low-side MOSFET driver. This pin is connected to the 5-V input supply for normal synchronous operation.

For added overvoltage protection, external sensing circuitry can be included to drive the LODRV input low in the event of an overvoltage. Applying a logic low to LODRV causes the driver for the low-side MOSFET to go to a high state causing the low-side MOSFET to turn on and act as a crowbar for the output. This input has precedence over any input present at LOHIB (pin 11); i.e., a low input to LODRV (pin 10) overrides the inhibit function.

LOHIB (pin 11) is an inhibit input for the low-side MOSFET driver. This input has to be logic low before the low-side MOSFET is allowed to be turned on, i.e., a logic high on LOHIB prevents the low-side MOSFET driver from turning on the low-side MOSFET. For normal synchronous operation, this pin is connected to the junction of the high and low-side MOSFETs. This prevents cross-conduction of the two MOSFETs by constraining the low-side MOSFET to be OFF unless its drain-to-source voltage is at a low level. Shoot-through current caused by both MOSFETs being ON simultaneously is actively prevented. However, if LODRV is low, the low-side MOSFET is turned ON regardless of the LOHIB input.

5.11.2 High-Side Driver

The driver for the high-side MOSFET can be configured either as a ground–referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting V_{cc} to BOOT. A 1-μF capacitor, C31, is connected from BOOT (pin 16) to BOOTLO (pin 18) for bypassing.

5.11.3 Grounding

There are two separate ground connections enabling the user to isolate high-current grounds from low current logic grounds. The low-current logic circuitry should be connected to ANAGND (pin 7). The high-current circuitry should be connected to DRVGND (pin 12). The maximum voltage difference between ANAGND (pin 7) and DRVGND (pin 12) should be limited to less than ±0.2 V.

Please refer to the Layout Guidelines section of the TPS5210 Data Sheet, literature number SLVS171.

6 Layout Guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB design. The general design should proceed from the switching node to the output, then back to the driver section and, finally, to place the low-level components.

Below are several specific layout recommendations to consider before layout of a TPS5210 design begins. Failure to implement these recommendations could result in a design that does not work.

- All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, DROOP, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
- Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O , and drive ground will connect to the main ground plane close to the source of the low-side MOSFET.
- Connections from the drivers to the gate of the power MOSFETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
- The bypass capacitor for the DRV regulator should be placed close to the TPS5210 and be connected to DRVGND.
- The bypass capacitor for V_{CC} should be placed close to the TPS5210 and be connected to DRVGND.
- When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power MOSFETs should be as short and as wide as possible. The other pins that also connect to the power MOSFETs, LOHIB and LOSENSE, should have a separate connection to the MOSFETS since BOOTLO will have large peak currents flowing through it.
- When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS5210.
- When configuring the high-side driver as a ground-referenced driver, BOOTLO should be connected to DRVGND.
- The bulk storage capacitors across V_I should be placed close to the power MOSFETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side MOSFET and to the source of the low-side MOSFET.
- High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
- HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side MOSFET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed

close to where HISENSE connects to Vin, to reduce high-frequency noise coupling on HISENSE.

Figure 30 shows a layout for the example design.

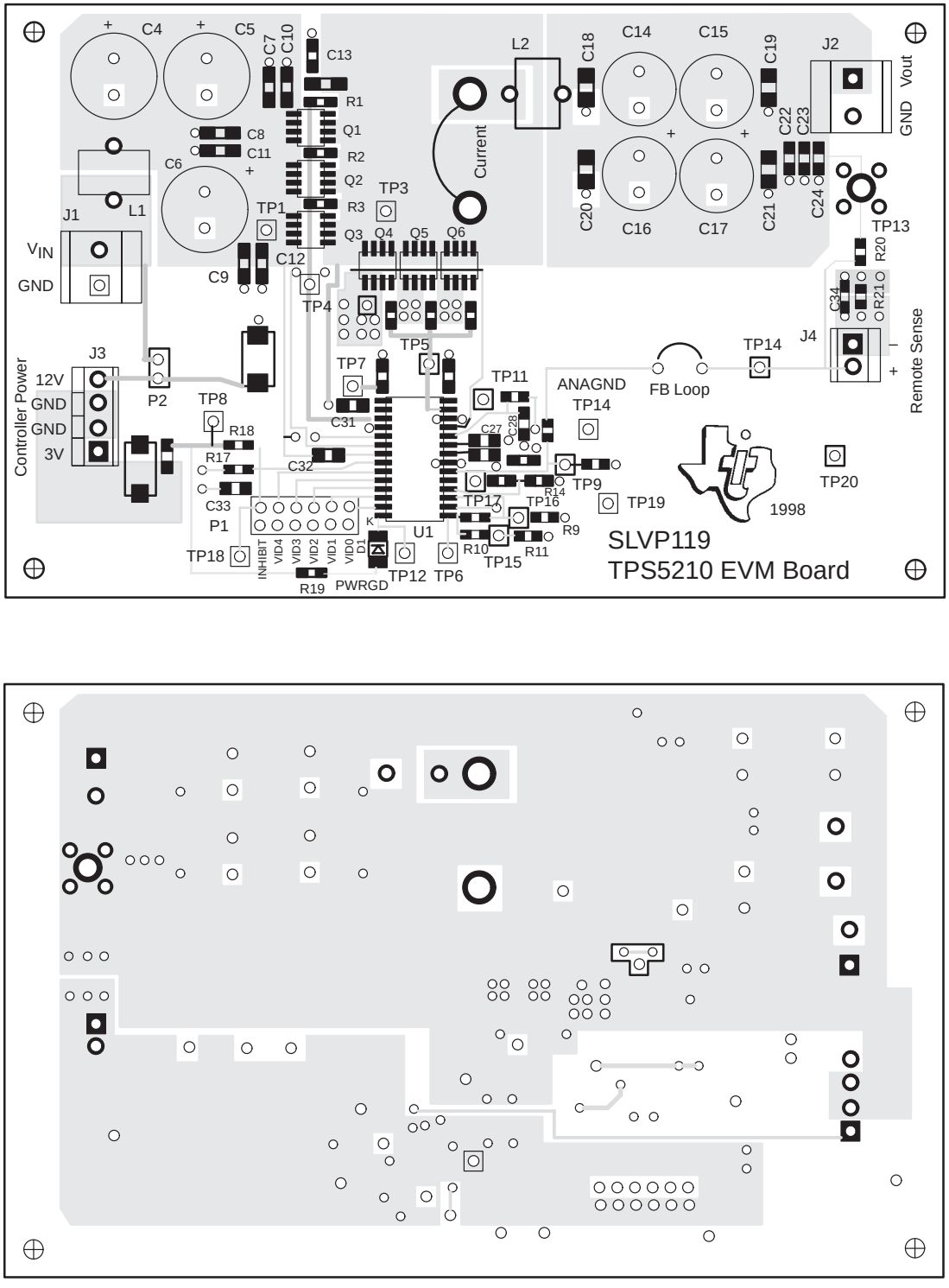


Figure 30. Example Layout

7 Summary

This application report described the operation and performance of a 12-V to 2-V 20-A example power supply design using the TPS5210 Programmable Synchronous Buck Regulator Controller. Experimental data for the example design showed tight static and dynamic regulation, fast transient response, high efficiency, and stable operation with good noise immunity. The report discussed the major functional blocks of the TPS5210, and derived a simple mathematical description of switching frequency and output voltage for a ripple regulator that showed good correlation with experimental data.

The report provided detailed mathematical procedures for defining and selecting the external component values required to set all limits and setpoints for the example design.

The TPS5210, designed specifically to address power supply design issues for next-generation microprocessors, ensures high efficiency; the absence of a sense resistor reduces conduction losses, and 8V/2A drive capability with adaptive-deadtime control reduces switching losses. The ripple regulator architecture greatly reduces the output capacitor requirements, while meeting tight regulation specifications.

8 Acknowledgements

This application report is the result of many individual efforts. The work included characterization of the controller chip, design, breadboarding, and debugging of the application example; and preparation of the report itself. Every effort has been made to provide a document that is useful and understandable to the customer/designer. The following list, though not all inclusive, represents the major contributors to this document.

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9 References

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3. David Briggs, Robert Martinez, Rais Miftakhutdinov, and Dale Skelton, “A Fast, Efficient Synchronous-Buck Controller for Microprocessor Power Supplies,” Proceedings HFPC Nov. 1998.

4. *TPS5210 Programmable Synchronous-Buck Regulator Controller* Data Sheet, Literature Number SLVS171.