Application Report
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# Power for the Virtex™-5 Transceiver Using DC/DC Converters With Integrated FETs

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**ABSTRACT**

This power supply was designed to power the transceivers in the Xilinx™ Virtex™-5 LXT and FXT platforms.

## Voltage Requirements

Two separate buck converters, the TPS54610 and the TPS54310 (U1 and U2, respectively, in Figure 1), transform the 3.3-V input voltage into 1-V and 1.2-V rails for the Xilinx™ Virtex™-5 transceivers. The 1-V output supports the AVCC node, whereas the 1.2-V output supports the AVTTTX, AVTTRX, and AVTTRXC nodes simultaneously. Additionally, the node AVCC_PLL is designed to handle either 1 V or 1.2 V (selectable through jumper J1) to support FXT or LXT, respectively. This reference design meets the transceiver voltage requirements summarized in Table 1.

**Table 1. Transceiver Voltage Requirements**

| VOLTAGE NET NAME TO MAIN BOARD | FXT/LXT TYPICAL VOLTAGE | REGULATION TOLERANCE | MAXIMUM RIPPLE |
|---|---|---|---|
| VCC33 (input voltage) | 3.3 V | 5% | 10 mV |
| AVCC | 1 V | 5% | 10 mV |
| AVCC_PLL | 1 V/1.2 V | 5% | 10 mV |
| AVTTTX | 1.2 V | 5% | 10 mV |
| AVTTRX | 1.2 V | 5% | 10 mV |
| AVTTRXC | 1.2 V | 5% | 10 mV |

## Current Requirements

This reference design can power 12 LXT/FXT transceiver pairs. (This is the maximum number of transceiver pairs in the largest FPGA for a total of 24 transceivers.)

Table 2 summarizes the maximum current each output can supply.

**Table 2. Maximum Output Current**

| OUTPUT VOLTAGE | MAXIMUM OUTPUT CURRENT |
|---|---|
| 1 V | 6 A |
| 1.2 V | 2 A |

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The current requirements in Table 2 are specifically for the FXT platform. The LXT platform has a lower requirement for the 1-V output current, but because this design exceeds those requirements, it can be used to power the LXT as well as the FXT..

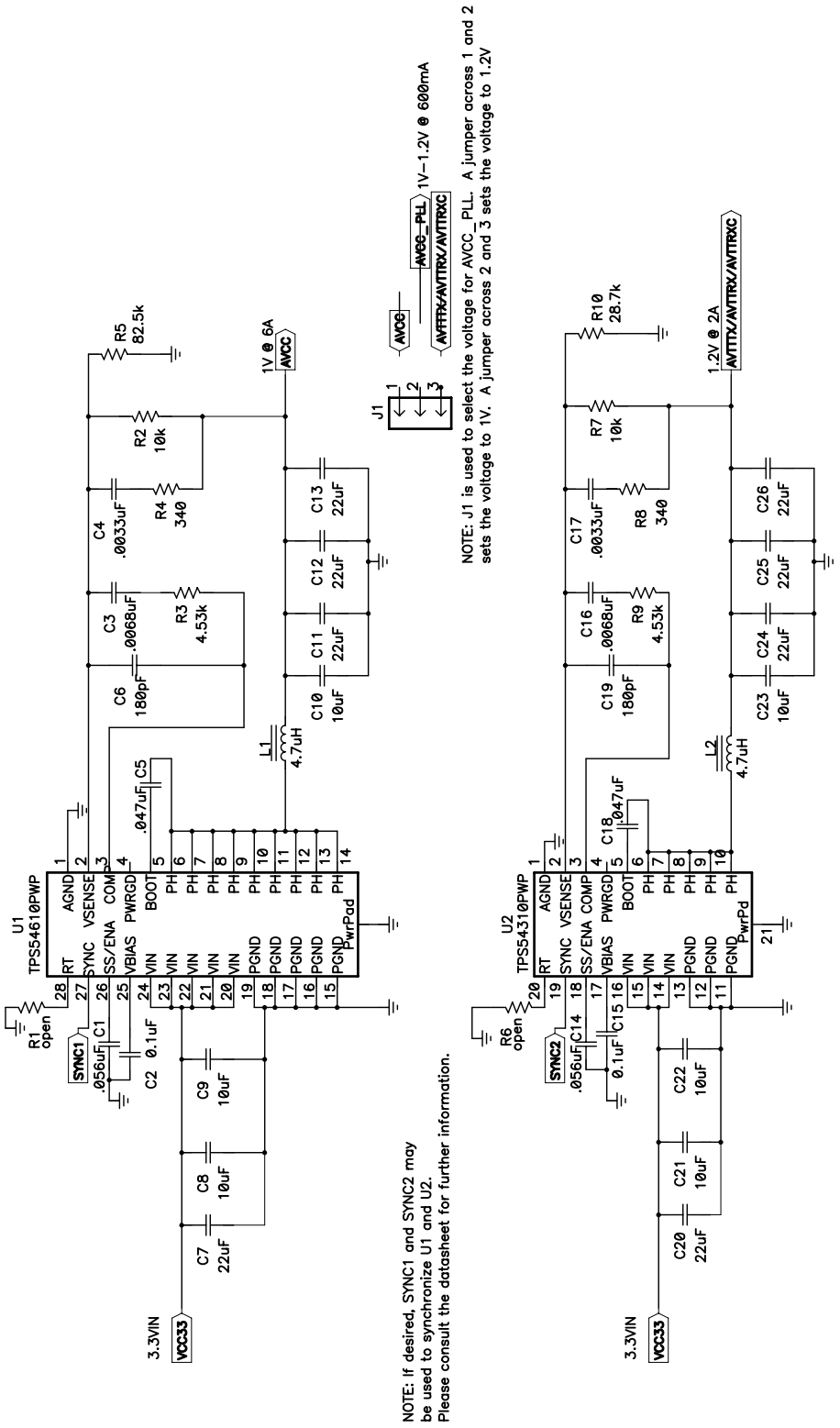


**Figure 1. Schematic**

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