Application Report
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TPS61500 SEPIC Configuration

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ABSTRACT

The TPS61500 is an inductive boost white LED driver with a 3-V to 18-V input voltage range. The boost has an integrated 130-mΩ, 40-V switch, with a 3-A (minimum) current limit. The LED current is regulated by controlling the feedback voltage across an external low-side current setting resistor. Dimming control is provided through the PWM input, which is fed into a low pass filter and made to adjust the feedback set point from 200 mV down to 0.

The boost configuration of the TPS61500 allows for an easy implementation of a SEPIC type power converter where the input voltage can be either higher or lower than the output voltage. Because the TPS61500's input voltage has a wide variation (3 V to 18 V), the SEPIC configuration makes it ideal for driving 3 to 5 series LEDs from a 12-V nominal battery voltage. This application note demonstrate the SEPIC converter design using the TPS61500 with nominal V_{OUT} of 12.3 V and a V_{IN} variation from 5 V to 18 V.

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1 Device Overview

The typical SEPIC application schematic for the TPS61500 is shown in Figure 1. A description of the devices pin function is given in Table 1.

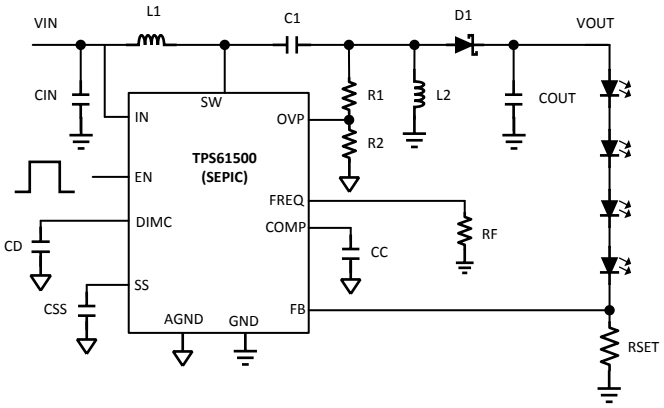

Figure 1. TPS61500 SEPIC Typical Application Schematic

Table 1. TPS61500 Pin Descriptions

PIN	FUNCTION	VOLTAGE RANGE	NOTES
IN	Input voltage connection	3 V to 18 V	
EN	Enable Input. This is also used as the PWM input for brightness control.	1.8-V logic level compatible, but can withstand voltages up to VIN	If EN is held low for > 10 ms the device is shut down
DIMC	external capacitor connection to set the low pass filter for the PWM to analog dimming (see TPS61500 data sheet)	up to 7 V	the low pass filter corner frequency is set by CD and an internal 25kΩ resistor (fc = 6.4 Hz with CD = 1 µF). DIMC pin varies proportional with PWM duty cycle from 0 to 1.2 V at D = 100%.
SS	Soft-start programming pin. Connect a capacitor from SS to GND. (see TPS61500 data sheet)	up to 7 V	Soft-start pin is ramped up to 1.8 V with a 6-µA current into CSS. See *Section 13.3* with CSS = 0.1 µF.
COMP	error amplifier output and compensation capacitor connection	up to 3 V	see *Section 12*
FREQ	Boost switching frequency setting resistor (see TPS61500 datasheet)	up to 3 V	SEPIC set to 1.37 MHz with RF = 75 kΩ
OVP	Over voltage protection input sense. Connect a resistive divider from OUT to OVP to set the trip threshold for OVP	up to 3 V	SEPIC circuit set to 15-V OVP (R1 = 210 kΩ and R2 = 13.7 kΩ)
SW	Inductor switching node. This is the connection for the primary inductor (L1) and the series capacitor C1.	up to 40 V	Voltage at this pin detects (V_{IN} + V_{OUT})

2 SEPIC Description

A SEPIC converter has the ability to regulate a voltage that is above or below the input voltage. In continuous conduction mode the SEPIC has a conversion ratio (VIN to VOUT) as:

$$VOUT = \frac{VIN \times efficiency \times D}{(1 - D)} \quad (1)$$

The input current (or average value of inductor L1 current) is given as:

$$IIN = IL1(AVE) = \frac{VOUT \times IOUT}{VIN \times efficiency} = \frac{IOUT \times D}{(1 - D)} \quad (2)$$

shows the switched voltages for L1 and L2. From the typical circuit, we can see that the SEPIC is basically the combination of a boost converter feeding an inverting buck-boost. The series capacitor C1, which is charged to VIN, forces L2's switched node to -VIN during the switch on time (when SW pulls low). This inverts the voltage at the top side of L2 compared to a traditional inverting buck-boost, and allows for a positive output voltage. During the off time, SW and L2's switched node pull high. This forward biases the Schottky diode causing L2's switched node to go to VOUT. SW then gets clamped at (VIN + VOUT).

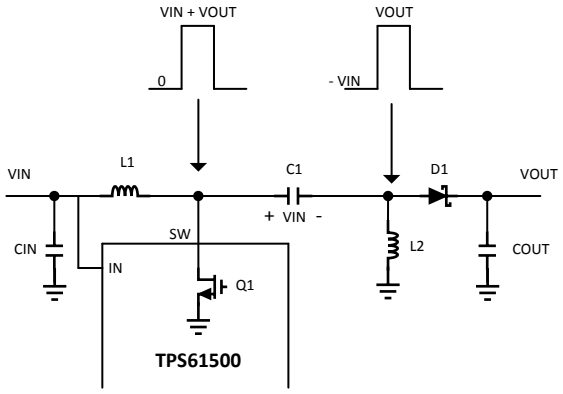

Figure 2. SEPIC Switching Voltages (CCM)

The SEPIC inductor current waveforms are shown in Figure 3. During the switch on time (when SW is pulled to GND), L1 current ramps up at:

$$\Delta IL1 = \frac{VIN \times D}{fsw \times L1} \quad (3)$$

Like wise, L2's current ramps up at the same rate (assuming L1 = L2) with its positive terminal connected to GND and its switching node at the inverting side of C1 (-VIN). Because L2's switched side is held at -VIN during the switch on-time, the Schottky is off and blocking (VOUT + VIN). L2's current is forced through C1 and into the boost switch (Q1). This causes Q1's current to be the sum of both IL1 and IL2 during the on time (green path). During the off time L1's current ramps down at:

$$\Delta IL1 = \frac{-VOUT \times (1 - D)}{fsw \times L1} \quad (4)$$

Likewise, L2 ramps down at the same rate and both inductor currents sum together through the Schottky diode (red path).

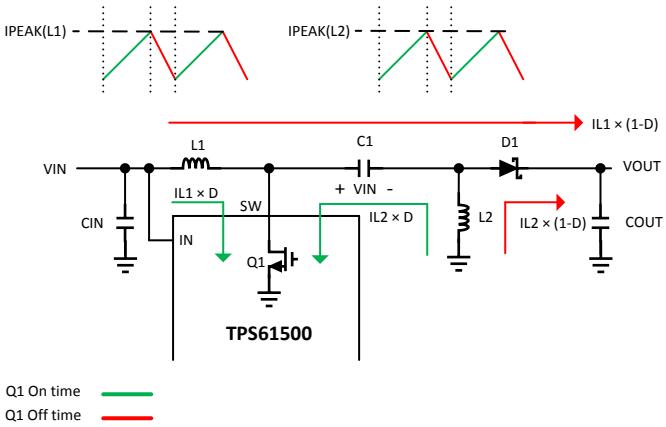

Figure 3. SEPIC Inductor Currents (CCM)

The operation of the SEPIC shown in Figure 2 and Figure 3 reveal some important design considerations:

1. During the SW off-time, Q1 will be forced to (VIN + VOUT).
2. During the SW on-time Q1 will conduct the sum peak current of both L1 and L2 (IL1(Peak) + IL2(Peak))
3. During the SW off-time the Schottky diode will detect the sum peak current of both L1 and L2 (IL1(Peak) + IL2(Peak))
4. During the SW on-time the Schottky diode reverse voltage will be the sum of (VIN + VOUT)
5. The series capacitor (C1) voltage is fixed at approximately VIN and is assumed to have negligible voltage ripple
6. The input current is continuous and is equal to the average current through IL1.
7. The output current is discontinuous (COUT supports ILED during Q1 on time), and IOUT is equal to the average current through IL2.

3 Inductor Value

The TPS61500 is designed to operate with an inductance range of 4.7 µH to 22 µH. A 4.7 µH value is chosen for both L1 and L2 to give a common inductance value (widely available) with a relatively small case size. A coupled inductor is also evaluated, which results in a smaller circuit size due to the core being shared between both primary and secondary windings (see Figure 12 for coupled inductor performance).

4 Configuring the Switching Frequency

The SEPIC switching frequency is closely tied to the inductor selection. Once the inductor value is selected, the switching frequency can be selected in order to achieve a set amount of inductor current ripple (K) in the input side inductance (L1). The typical rule is to target the inductor current ripple in the range of 20% to 40% of the max inductor current. Having an inductor current ripple that is too large limits the maximum output power because the switch peak current rating (3A min) will be hit during the switch on-time (see *Section 5*). Too small an inductor current ripple requires a switching frequency that is too high, which will unnecessarily cause high switching losses and lower efficiency (see *Section 7.3.1*).

Solving for f_{SW} based on a K value, starts with knowing the DC current in the input inductor L1. This is targeted at the highest output power and the minimum VIN. This is given as:

$$IIN(MAX) = \frac{IOUT(MAX) \times VOUT(MAX)}{VIN(MIN) \times efficiency} \quad (5)$$

L1's peak current is equal to IIN(MAX) + 1/2 the inductor current ripple:

$$IPEAK(L1) = IIN(MAX) + \frac{\Delta IL1}{2} \quad (6)$$

The inductor current ripple is given again as:

$$\Delta IL1 = \frac{VIN \times D}{fsw \times L1} \quad (7)$$

We can re-write (2) in terms of the K value:

$$(1 + \frac{K}{2}) \times IIN(MAX) = IIN(MAX) + \frac{\Delta IL1}{2} \quad (8)$$

Combining (1), (3), and (4) and solving for f_{SW} yields the solution for f_{SW} based on a given K value:

$$fsw = \frac{VIN(MIN)^2 \times efficiency \times D}{VOUT(MAX) \times IOUT(MAX) \times K \times L} \quad (9)$$

where D for the SEPIC operating in continuous conduction mode is given as:

$$D = \frac{VOUT(MAX)}{VOUT(MAX) + VIN(MIN) \times efficiency} \quad (10)$$

Based on a target VIN(MIN) = 5V, VOUT(MAX) = 12.3 V, IOUT(MAX) = 500mA, K = 40%, L = 4.7µH, and an estimated efficiency of 80%, the switching frequency target is 1.3MHz. We can select a standard 65 kΩ value for RF, which sets f_{SW} at typically 1.4MHz. Selecting a higher K value allows for a lower switching frequency, which provides for higher efficiency (provided that the peak current limit is not exceeded, see *Section 5*).

5 Peak Switch Current

As stated previously, the SEPIC's peak switch current during the switch on-time is the sum of both L1's peak current and L2's peak current. L1's peak current is composed of IIN + 1/2 the inductor current ripple. L2's peak current is composed of IOUT + 1/2 the inductor current ripple. If we assume L1 and L2 are equal then both L1 and L2's ripple current is equal.

The TPS61500 power switch has a peak current of 3 A (minimum). When the switch current hits this peak current limit the switch is turned off and switching is suspended until the next switching cycle. This puts a limit on the total output power which the circuit can support. The switch peak current is given by the following:

$$ISW(PEAK) = IL1(PEAK) + IL2(PEAK) = \frac{VOUT(MAX) \times IOUT(MAX)}{VIN(MIN) \times efficiency} + IOUT(MAX) + \frac{VIN(MIN) \times D}{L1 \times fsw} \quad (11)$$

Equation 11 is useful for calculating the operating peak current based on tolerances in inductance, switching frequency, and potential dips in VIN below 5V due to transient events.

Equation 11 can also be written in terms of IOUT(MAX), while including the K value in place of the inductor current ripple:

$$IOUT(MAX) = \frac{ISW(PEAK) \times VIN(MIN) \times efficiency}{VOUT(MAX) \times (1 + K) + VIN(MIN) \times efficiency} \quad (12)$$

Based on VIN(MIN) = 5 V, VOUT(MAX) = 12.3 V, IOUT(MAX) = 500 mA, a –20% inductor tolerance (L = 3.76µH), -20% shift in f_{SW} (f = 1.12 MHz), and an estimated efficiency of 80%, the operating peak current is estimated to be 2.93A, which is in line with being less than the 3-A mininimum current limit.

6 Inductor Selection

6.1 Discrete Inductor Selection

The TPS61500 is designed to operate with an inductance range of 4.7 µH to 22 µH. A 4.7 µH for both L1 and L2 is chosen to give a small size while maintaining low resistance in a widely available value. If an inductor other than the device listed in (Table 2) is used, it must be able to handle the peak operating current. The required peak current in L1 occurs at VIN(MIN), VOUT(MAX), and IOUT(MAX). This was discussed in Section 4, but is shown again as:

$$IL1(PEAK) = \frac{VOUT(MAX) \times ILED(MAX)}{VIN(MIN) \times efficiency} + \frac{VIN(MIN) \times D}{2 \times fsw \times L} \quad (13)$$

For example, given VOUT(MAX) = 12.3 V, ILED(MAX) = 0.5 A, VIN(MIN) = 5 V, efficiency = 0.8, L = 3.76 µH (L(nom) – 20%), f_{SW} = 1.12MHz (fsw(nom) – 20%), the maximum peak operating current in L1 would be 1.99 A.

For L2, the peak operating current occurs at maximum VIN, max VOUT, and max ILED this is given by:

$$IL2(PEAK\_CCM) = ILED(MAX) + \frac{VIN(MAX) \times D}{2 \times fsw \times L} \quad (14)$$

In this configuration with, VOUT(MAX) = 12.3 V, ILED(MAX) = 0.5 A, VIN(MAX) = 18 V, efficiency = 0.8, D = 0.46, the peak operating current for L2 would be 1.48A. Ideally, L2 could be sized smaller than L1.

6.2 Coupled Inductor Selection

In place of two discrete inductors, a coupled inductor can be used. A coupled inductor provides the following:

- Smaller form factor due to the shared core between L1 and L2
- Reduced input current ripple at the switching frequency. This is due to leakage inductance in series with the primary side inductance causing the current ripple to become steered to the lower impedance secondary winding (see *Section 6.2.1*, *Section 14* #5, #4)
- reduction of both switch and diode peak currents due to mutual inductance effectively reducing the total ripple currents in (L1 + L2) by a factor of 2 (see *Section 14* #6).

The major drawback however, is the limited availability of a suitable coupled inductor and the tendency for these devices to have a taller profile then discrete inductors with the same current rating. In Table 2, an LPD5030-472 was evaluated, see (Figure 12) and (Figure 9).

The rating of the coupled inductor must take into account total current in both windings. This would place a limit on the maximum output power which the circuit could deliver. Assuming continuous conduction mode, the total current in both windings is the sum of both inductors average currents + 1/2 the total current ripple for both. This is given again as:

$$IL(SUM) = IL1(PEAK) + IL2(PEAK) = \frac{VOUT(MAX) \times IOUT(MAX)}{VIN(MIN) \times efficiency} + IOUT(MAX) + \frac{VIN(MIN) \times D}{2 \times L1 \times fsw} \quad (15)$$

Based on the LPD5030-472 which has a maximum current of 2.2 A (both windings combined), VOUT(MAX) = 12.3 V, VIN(MIN) = 5 V, estimated efficiency = 0.8, L = 3.76µH (L nom – 20%), and f_{SW} = 1.12 MHz ($f_{SW\_NOMINAL}$ – 20%), the IOUT(MAX) would be estimated at 430 mA maximum. Slightly less current capability than the dual inductor topology.

6.2.1 Current Steering Effect

The following plots show the difference in input current ripple between two discrete inductors and a coupled inductor. The green trace is the current into the input side inductance. The coupled inductor shows approximately a 200-mA peak to peak current where the dual inductor topology shows approximately 620 mA. The advantage to lower input current ripple is that it can allow for a smaller input capacitance.

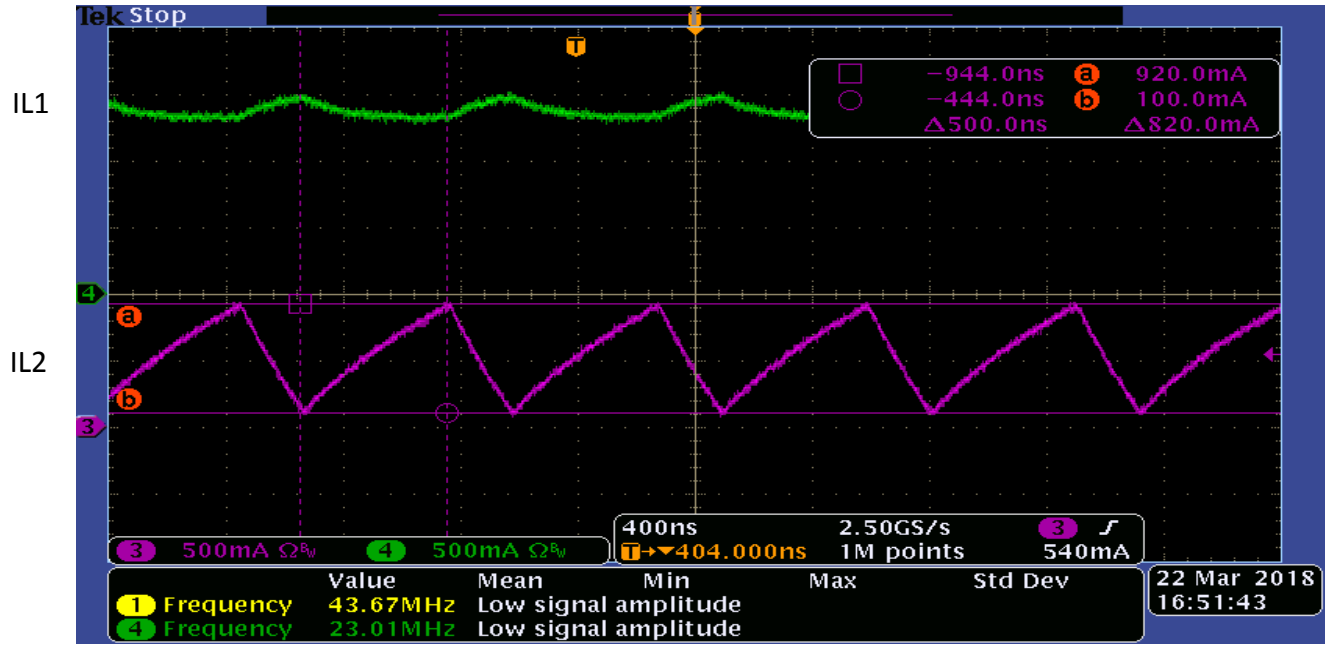

Figure 4. Coupled Inductor

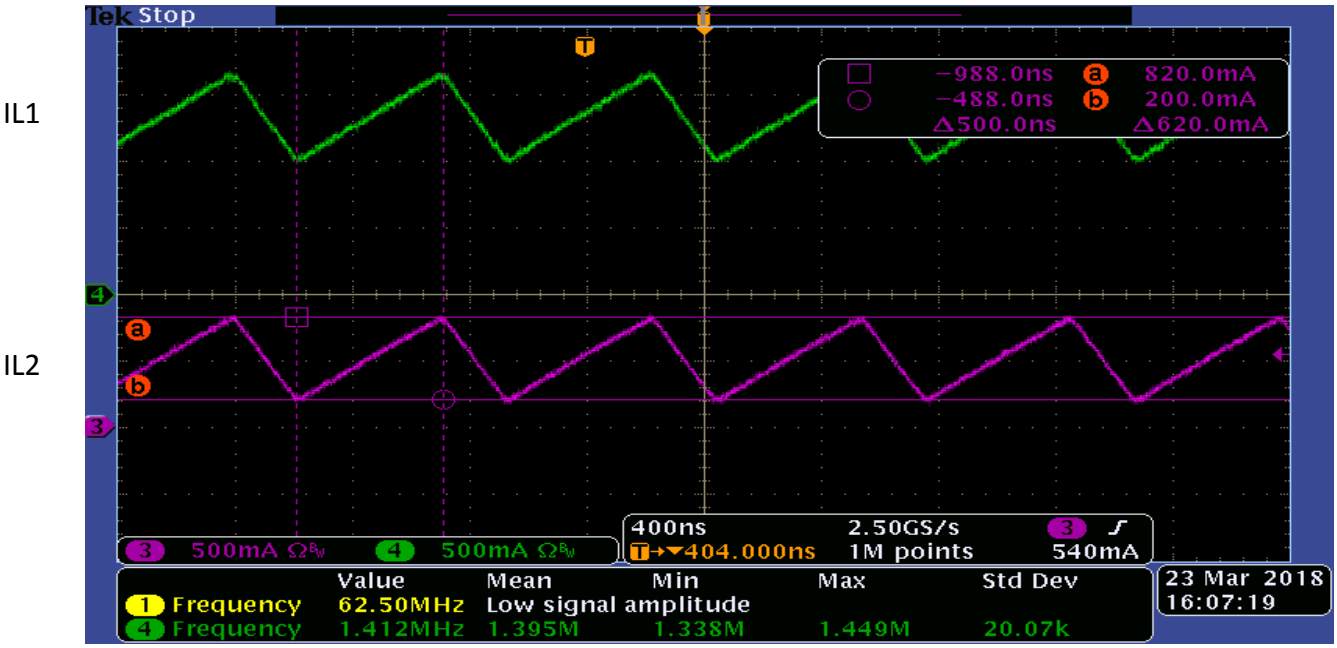

Figure 5. Dual Inductors

6.2.2 Coupled Inductor Orientation

When configured with a coupled inductor, the dot orientation must be connected properly. The dot orientation on the coupled inductor indicates the phase relationship between primary and secondary windings. The dot on the primary will have the same phase as the dot on the secondary. In the case of the SEPIC, when the primary dot side is positive with respect to the primary non-dotted side, the secondary dotted side is also positive with respect to the secondary non-dotted side.

For example, Figure 6 shows the properly connected coupled inductor SEPIC with the primary side dot on the VIN side and the secondary side dot on the GND side. During the switch on time, L1's polarity has #1 = VIN, #2 = GND. This forces the secondary dot side #4 positive with respect to pin #3, which due to the 1:1 turns ratio, makes #3 = –VIN. This is important in coupled inductor SEPIC's because the current flow in L1 and L2 must be simultaneous in order to store energy in L2 during the switch on-time. The other important thing to note is that the primary side of the coupled inductor must be connected to L1 (#1 = VIN). Otherwise, the current steering effect is pushed to the secondary and result in all the current ripple appearing on the primary side.

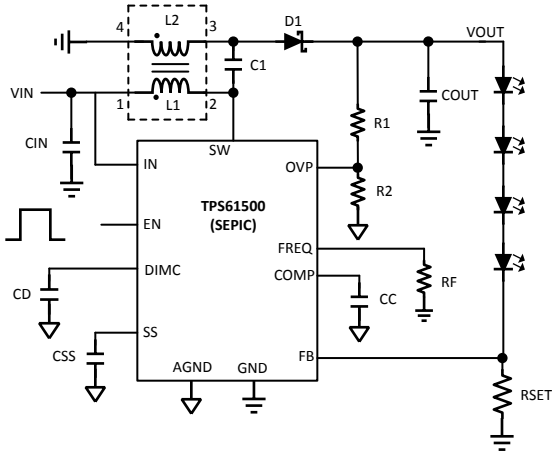

Figure 6. TPS61500 With Properly Oriented Coupled Inductor

7 Schottky Diode Selection

The Schottky diode must be selected for these criteria:

- The reverse voltage rating must be greater than [VOUT(MAX) + VIN(MAX)].
- The average current rating must be > ILED(MAX)
- The peak current rating must be > the sum of the maximum peak current of IL1 and IL2.
- The diode junction capacitance, reverse current, and forward voltage should be chosen as low as possible in order to optimize efficiency.

7.1 Maximum Reverse Voltage

The voltage across the series capacitor C1 is held at VIN. During the on time, when SW is pulled to GND, L2's switching node will be forced to -VIN. this causes the Schottky diode to become reverse biased with a maximum voltage of (VOUT_MAX + VIN_MAX) across the reverse biased junction. Under worse case conditions this could result in (12.3 V + 18 V = 30.3 V) across the Schottky diode.

7.2 Current Rating

A Schottky diode is typically rated with a maximum average current and either a repetitive peak current or a non-repetitive peak current rating. The average diode current in the SEPIC is IOUT. The maximum peak current occurs during the switch off time when the current through L1 and L2 sum together through the diode. This occurs at minimum VIN and maximum VOUT and is given as:

$$IDIODE(PEAK) = IL1(PEAK) + IL2(PEAK) = \frac{VOUT(MAX) \times IOUT(MAX)}{VIN(MIN) \times efficiency} + IOUT(MAX) + \frac{VIN(MIN) \times D}{L1 \times fsw} \quad (16)$$

Where D is given in Equation 16. This is the same equation as determining the peak NMOS current. Typically the diode can be chosen to handle only the maximum average current. However, because the power dissipation is relatively high in the diode the diode temperature rise will be significant. This can have large effects on the diode's reverse current. Therefore, the selected diode is chosen so it can handle a maximum average current of 3 A.

7.3 Junction Capacitance, Forward Voltage, and Reverse Current

7.3.1 Capacitance

Schottky Diodes junction capacitance is the effective capacitance across the diodes reverse biased junction. This effective capacitance must be charged each switching cycle as the diode goes from the on state (SEPIC off-time) to the reverse biased state (SEPIC on-time). The loss associated with this capacitance is approximately:

$$P(diode\_capacitance) = \frac{(VOUT + VIN)^2}{2} \times CD \times fsw \quad (17)$$

CD is the estimated diode capacitance (found in the diode datasheet). For example, at VOUT = 12.3 V, VIN = 12 V, the diodes capacitance for the listed diode in Table 2 is approximately 360pF. This results in approximately 154 mW of loss. As a % of the total efficiency loss this would be (P(diode_capacitance)/(Input Power)). At ILED = 500 mA, VOUT = 12.3 V the efficiency is 89%, and the input power is (6.91 W). At this operating point the Schottky diode capacitance is accounting for around 2.2% of the efficiency loss. Because this is a constant loss across load, at ILED = 100 mA, where the output power is much lower, the diode capacitance would be estimated to account for around 10% of the efficiency loss.

7.4 Diode Forward Voltage

The diode forward voltage is the on state voltage drop across the Schottky during the SEPIC off-time. The forward voltage drop would be measured at the average peak diode current (IIN + IOUT). This can be approximated as:

$$I(diode) = IOUT \times \left(1 + \frac{VOUT}{VIN \times efficiency}\right) \quad (18)$$

The diode power loss would then be found using the average diode current (IOUT):

$$P(diode\_vf) = VF(@Idiode) \times IOUT \quad (19)$$

For example, at VOUT = 12.3 V, IOUT = 500 mA, VIN = 12 V, efficiency = 89%, the average peak diode current is 1.08 A. From the MBRA340 datasheet this results in a VF of 0.25 V (assuming T_J = 100°C). Which results in a power loss estimate of 125 mW.

7.5 Reverse Current

The last main parameter to look for in Schottky diode selection is reverse current. Schottky diodes can have a relatively high reverse leakage current (IR) when operating in reverse bias. IR has a strong dependence on temperature (typically around 10× increase for every 25°C rise in temp). The power loss due to the reverse current can be approximated as:

$$P(diode\_ir) = VIN \times efficiency \times IR \quad (20)$$

IR would be selected at the reverse voltage of (VOUT + VIN). In the selected diode, the reverse current at (VOUT = 12 V and VIN = 12V) is approximately 2 mA (T_J = 100°C) which gives a P(diode_ir) loss of approximately 21mW. For this particular diode, IR is low enough to not be an issue. For diodes selected with much higher IR, (and in smaller footprints that might result in higher self heating), IR can drastically increase as the Schottky power dissipation increases (higher: Pdiode_capacitance, Pdiode_vf, Pdiode_ir), results in more self heating, which in turn results in higher IR. This can potentially lead to the point of thermal runaway. For SEPIC type converters, the Schottky must be sized appropriately to limit self heating to the recommended safe operating range. Diode self heating has a strong dependency on diode package, and PCB layout.

8 Output Capacitor Selection

The output capacitor has two functions. First, it supplies the output current during the SEPIC on time, when the Schottky is reverse biased. Secondly, it contributes to the complex pole in the SEPIC power stage gain and phase (AMOD). In this application the output capacitor is designed to be a nominal 10 µF, 50 V, 1206 case size X5R device. This device was used in the stability analysis and the measured transient responses. Because the output capacitor will affect the feedback loop gain and phase, it is necessary to use a device similar to the one listed in Table 2.

9 Series Capacitor Selection

The series capacitor (C1) is assumed to be fixed at VIN with negligible voltage ripple. However, during the SEPIC on-time, C1 will be charging L2 (average current is IOUT). This will cause C1 to discharge. Therefore C1 needs to be sized large enough such that during the switch on-time, when C1 is supplying L2's inductor current, the voltage across C1 is relatively constant (5% ripple voltage is a good target). The worst loading condition on C1 occurs at max LED current, and min VIN (max on-time).

C1 also needs to be verified at the maximum VIN where the capacitance degradation due to DC bias is the highest. Minimum C1 can be determined by:

$$CF > \frac{ILED(MAX) \times VOUT(MAX)}{(VIN \times efficiency + VOUT(MAX)) \times fsw \times VIN \times 5\%} \quad (21)$$

For this application, min C1 at VIN = 5 V is 1.3 µF and at VIN = 18 V, it is 0.21 µF. Table 2 shows the selected C1 effective capacitance at 5 V, 12 V, and 18 V.

10 Input Capacitor (CIN and CBYP)

The input capacitor is chosen to be a 10 µF, 50 V, 1206 device (same as COUT). In a SEPIC, CIN is not as critical as COUT or C1 because of the continuous inductor current at the input. CIN is there only to filter the inductor current ripple of L1. However, the layout of CIN must limit the trace inductance between the CIN+ and the input to L1, as well as the inductance between CIN– and GND. This requires that CIN be placed as close to L1 as possible and as close to the junction of COUT– and the TPS61500's PGND pin as possible.

11 Compensation Capacitor (CC)

The compensation capacitor has been designed to be a 15-nH ceramic capacitor (dual inductor toplogy) or a 33-nH (coupled inductor topology) with a tolerance of ±10% and a temperature tolerance of ±15%. The COMP output will regulate to 1.25 V, thus making the DC rating of COMP not critical. However, to minimize any DC bias shift associated with ceramic capacitors, a 25-V device was used.

12 Compensation

The COMP pin on the TPS61500 is the output of the error amplifier and provides for compensating the feedback loop of the device. The uncompensated SEPIC can have a complex loop gain consisting of right half plane zeroes and complex poles, which will lead to instability if the loop is not designed correctly (see Section 14 #2). The criteria for loop compensation will be to ensure the crossover frequency (f_C) of the loop is at least 10X lower than the lowest right half plane zero, and that there is at least 60 degrees of phase margin at min and max VIN.

First we can calculate the right half plane zerop (RHPZ) as:

$$f_{RHPZ} = \frac{VOUT(MAX) \times (1-D)^2}{2\pi \times L1 \times IOUT(MAX) \times D^2} = \frac{(VIN \times efficiency)^2}{2\pi \times L1 \times IOUT(MAX) \times VOUT(MAX)} \quad (22)$$

Next, we can measure the uncompensated loop gain, and by inspection, determine if our target f_C at 1/10 × f_{RHPZ} will provide the 60 degress of phase margin for the full VIN range.

12.1 Measuring the Uncompensated Loop

To begin with, the total loop gain (G_{LOOP}) of the SEPIC consists of:

$$G_{LOOP} = A_{MOD} \times A_{FB} \times A_{COMP} \quad (23)$$

AMOD is the power stage gain of the SEPIC, AFB is the divided down output voltage (VFB/VOUT) and ACOMP is the gain of the compensator (gm × Z_O). Z_O is the effective impedance at the COMP pin.

In order to measure A_{MOD}, we need to reduce A_{COMP} to unity. This can be done by making Z_O equal to 1/gm. From the datasheet, gm is given as 340 µmho (typical), thus making R_{ZO} = 1/340 µmho = 2.94 kOhms. A high value capacitor CP = 10 µF is placed in series with R_{ZO} to eliminate any DC loading on COMP. This places a pole zero pair at very low frequencies, and gives the error amplifier a unity gain at all frequencies of interest. The uncompensated loop gain and phase margin (A_{MOD} × A_{FB}) is shown in Figure 7.

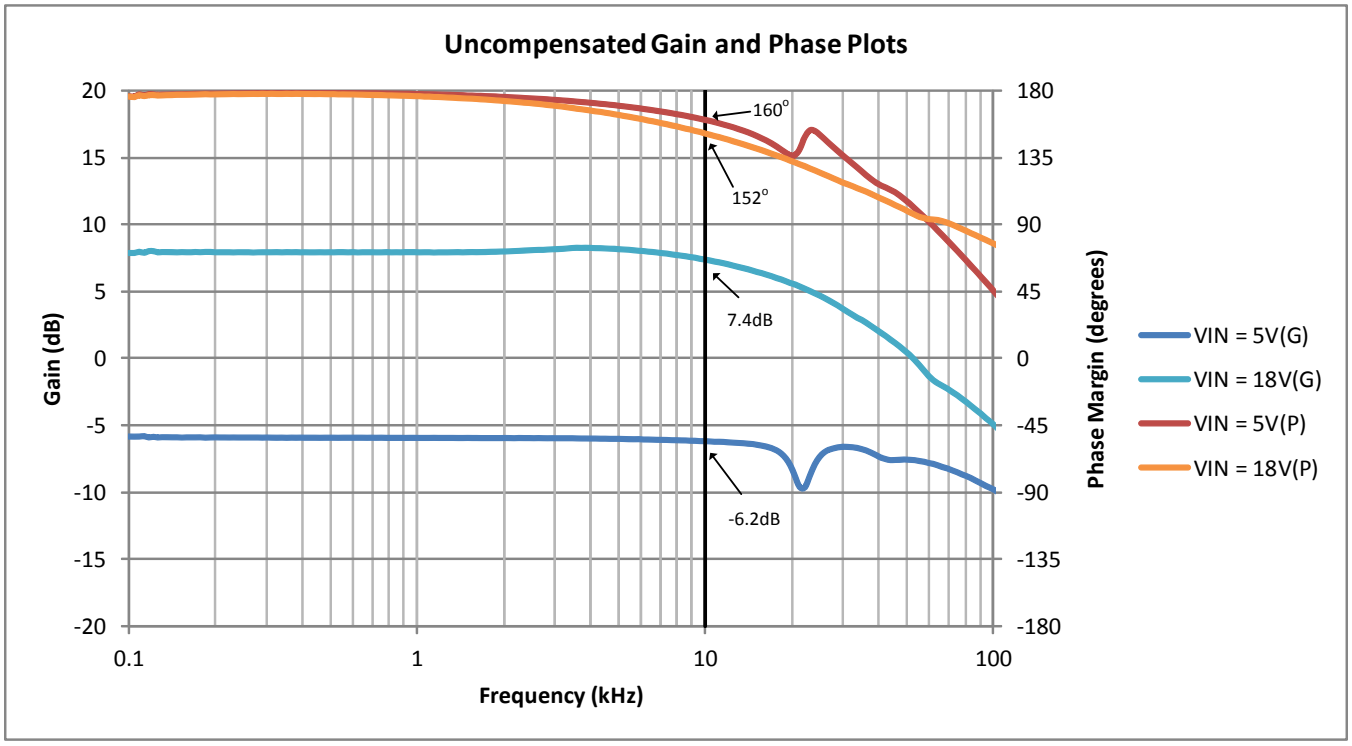

Figure 7. AMOD x AFB

Using an estimated efficiency of 85%, the right half plane zero frequency occurs at 96.6 kHz for VIN = 5 V and 1.23 MHz for VIN = 18 V. The goal of compensating this loop will be to ensure a > 60° phase margin at 0dB for both VIN = 18V and VIN = 5V. The crossover frequency will be targeted for 10 kHz (f_{RHPZ}/10). Inspection of the uncompensated gain and phase plots shows a gain and phase of –6.2 dB/160° for VIN = 5 V and 7.4 dB/152° for VIN = 18 V (both at f = 10 kHz). Attempting to make the crossover frequency be 10 kHz at VIN = 5 V might result in phase margin issues for VIN at 18 V, so we can choose f_C = 10 kHz based on VIN = 18 V.

12.2 Compensating the Loop

Compensation capacitor (CC) is then chosen to offset the uncompensated gain (A_{MOD} × A_{FB}) at f_C in order to achieve unity gain. This is given as:

$$CC = \frac{gm \times A_{MOD} \times A_{FB}}{2\pi \times f_C} \quad (24)$$

gm is listed in the TPS61500 (440µmhO(max)), AMOD × AFB is 7.4 dB (2.34 V/V) and found from Figure 7. CC is calculated as 16.4 nF. For the coupled inductor design, AMOD × AFB were also measured (not shown). Using the same procedure from above, CC was chosen for the coupled inductor configuration as 33 nF. The compensated loop gain and phase plots for the dual inductors and the coupled inductor are shown in Figure 8 and Figure 9. The crossover frequency at VIN = 18 V for the dual inductor configuration was measured at 8.8 kHz (1.7 kHz for VIN = 5 V). This is lower than expected due to the more typical value of gm and the 15 nF chosen for CC.

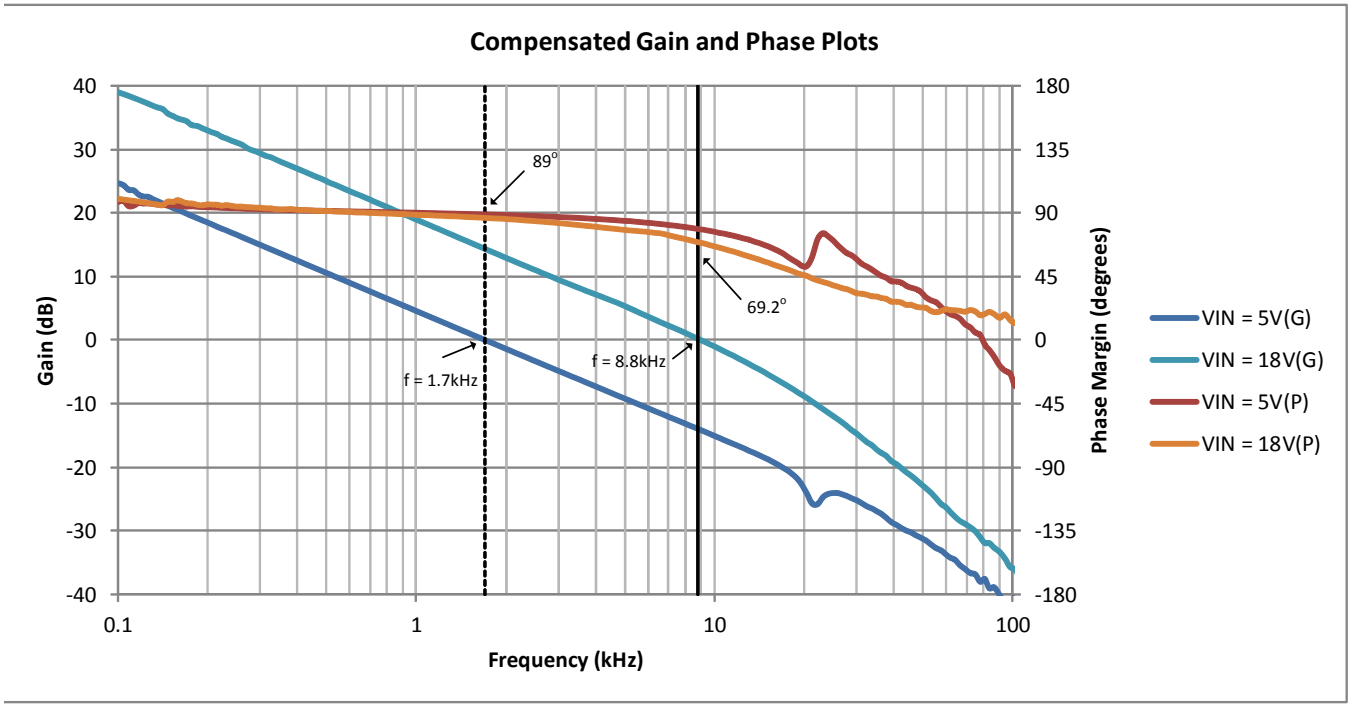

Figure 8. AMOD × AFB × ACOMP (Discrete Inductors)

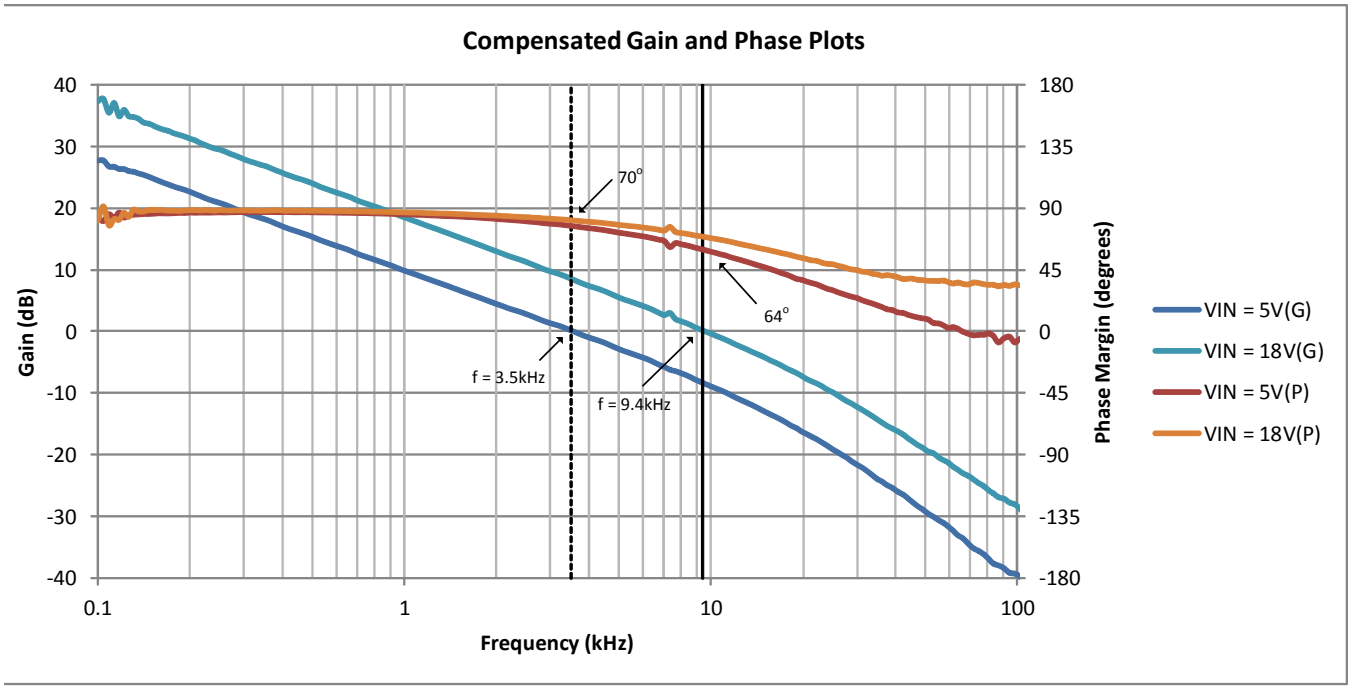

Figure 9. AMOD × AFB × ACOMP (Coupled Inductors)

13 Measured Results

Measured efficiency, start-up, and line transients are shown below using the circuit of Figure 10. Coupled inductor efficiency is also included as a comparison against the dual inductor measurement.

13.1 Evaluation Schematic

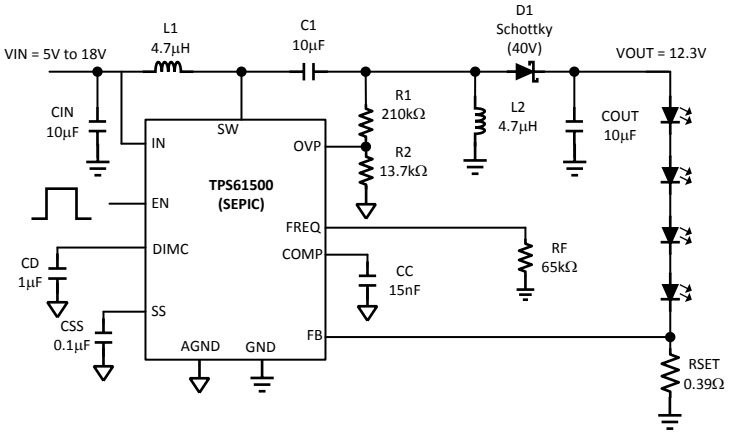

Figure 10. Evaluation Schematic (Dual Inductors)

Table 2. Materials List

Device	Function	Value	Manufacturer	Part Number	Size	Ratings/Spec's	Notes
L1	Input Power Inductor	4.7µH	Cyntec	HBLE041H-4R7MS	4mm × 4mm × 1.8mm	ISAT = 2.7A (min)	RDC = 70mΩ
L2	Output Power Inductor	4.7µH	Cyntec	HBLE041H-4R7MS	4mm × 4mm × 1.8mm	ISAT = 2.7A (min)	RDC = 70mΩ
L1//L2	Coupled Inductor	4.7µH	Coiltronics	LPD5030-472MR	4.8mm × 4.8mm × 2.9mm	ISAT = 2.2A (sum of both windings)	RDC = 111mΩ (each winding)
CIN	Input Bypass Capacitor	10µF	TDK	C3216X5R1H106KT	1206 (3.2mm × 1.6mm × 1.6mm)	50V, ±10%	DC Bias Degradation (from nominal)
							-8% at 5V
							-42% at 12V
COUT	Output Bypass Capacitor	10µF					-62% at 18V
C1	Series Coupling Capacitor	10µF	TDK	C3216X5R1H106KT	1206 (3.2mm × 1.6mm × 1.6mm)	50V, ±10%	DC Bias Degradation (from nominal)
							-8% at 5V (9.2µF)
							-42% at 12V (5.8µF)
							-62% at 18V (3.8µF)
D1	Rectifying Diode	Schottky	On-Semi	MBRA340	4.32mm × 2.6mm × 2.1mm	40V, 3A (ave)	
RFB	Sets the maximum LED current	0.39Ω	Panasonic	ERJ-8RQFR39V	1206 (3.1mm × 1.6mm × 0.55mm)	1/4 watt, 1%	

Table 2. Materials List (continued)

Device	Function		Value	Manufacturer	Part Number	Size	Ratings/Spec's	Notes
CC	Compensation Capacitor	Dual Inductor	15nH	TDK	CGA2B2X5R1E153KT	0402 (1mm × 0.5mm × 0.5mm)	25V, ±10%	25V rating is to ensure no DC bias shift
		Coupled Inductor	47nH	TDK	C1005X8R1E473K050BC			
RF	Frequency Setting Resistor		65kΩ	various		0603 (1.2mm × 0.8mm × 0.5mm)	1%	
CD	PWM input filter capacitor		1µF	various		0603 (1.2mm × 0.8mm × 0.8mm)	X5R, 20%	25V rating ensures no DC bias shift
CSS	Soft-Start Capacitor		0.1µF	various		0603 (1.2mm × 0.8mm × 0.8mm)	X5R, 20%	25V rating ensures no DC bias shift
R1	Over Voltage Protection Resistor Divider		210kΩ	various		0603 (1.2mm × 0.8mm × 0.5mm)	1%	sets OVP at 20V
R2			13.7kΩ	various		0603 (1.2mm × 0.8mm × 0.5mm)	1%	

13.2 Efficiency

With the given components, the measured efficiency of the circuit is shown in Figure 11.

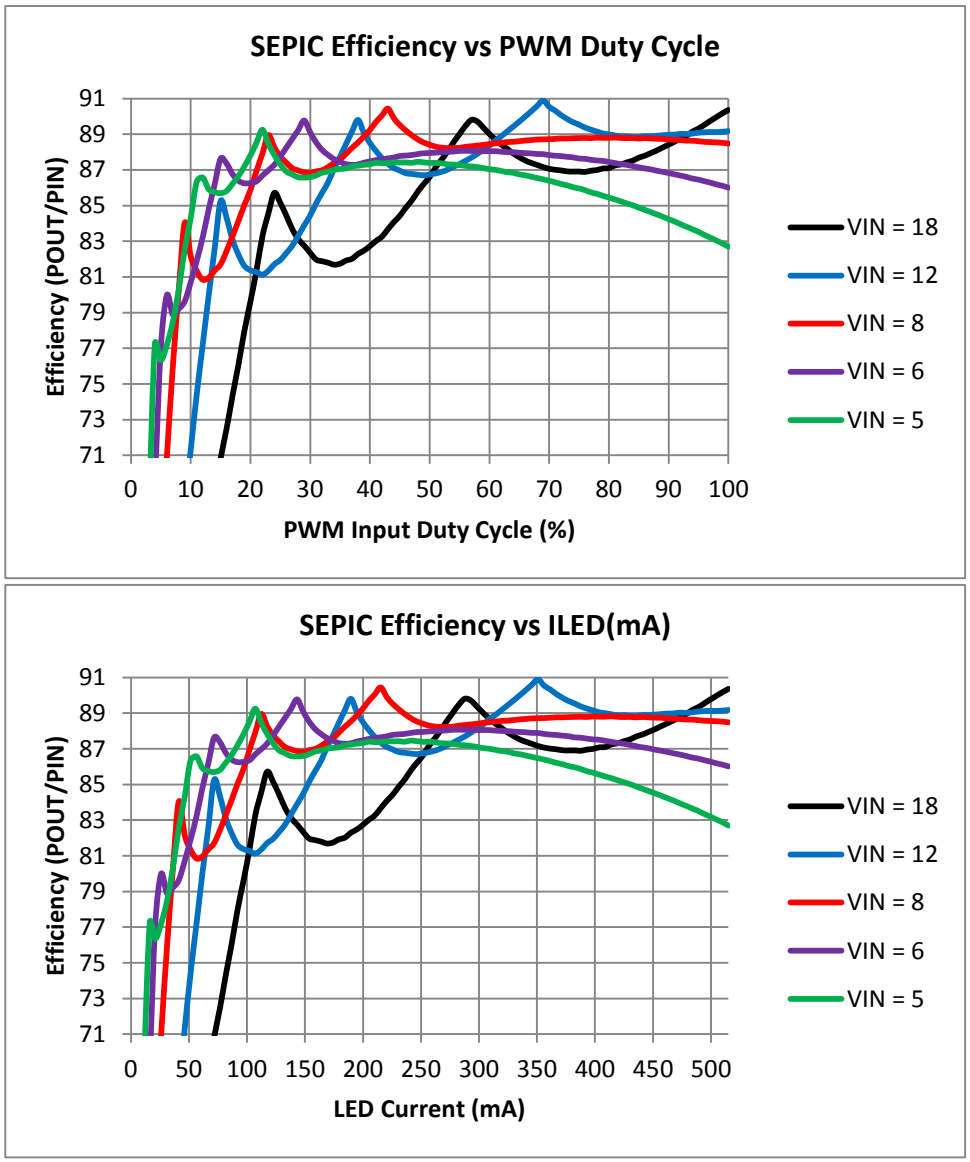

Figure 11. Measured Efficiency With Dual Inductors

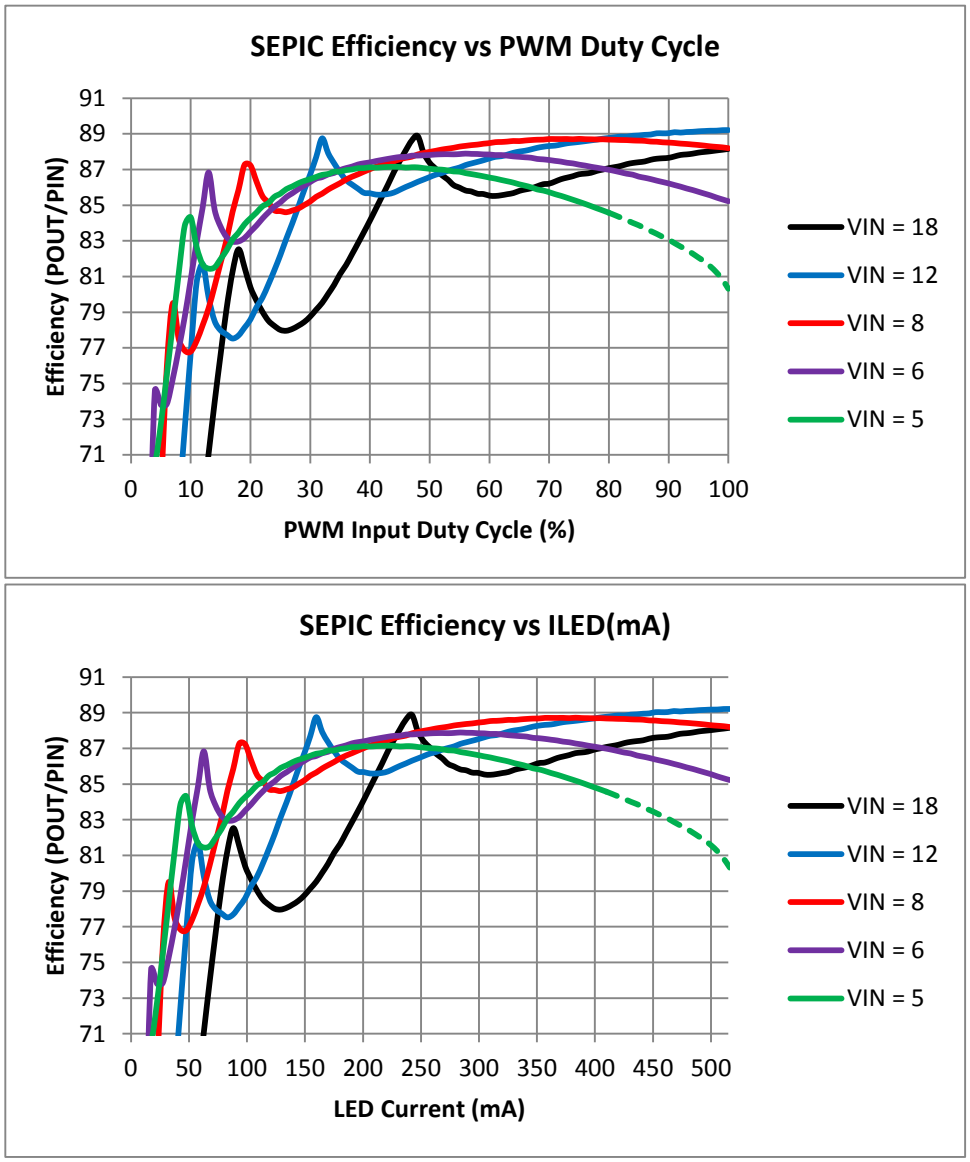

Figure 12. Measured Efficiency With Coupled Inductors

13.3 Start-Up

Typical start-up is shown in Figure 13, with CSS = 0.1 µF.

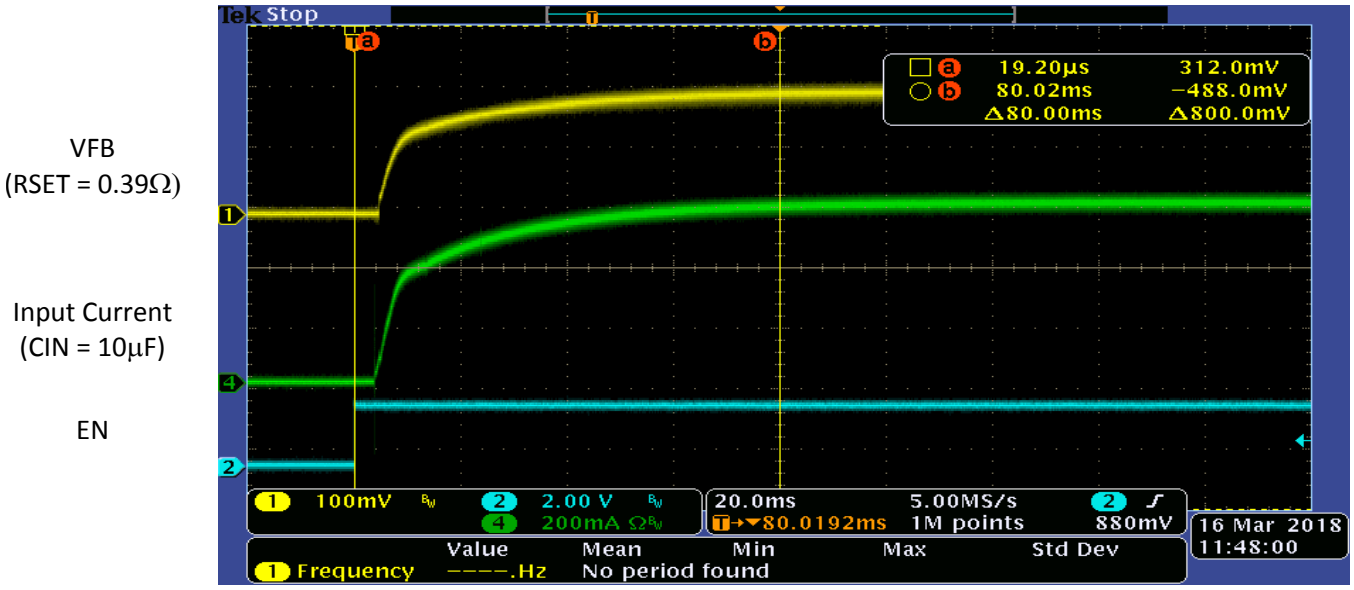

Figure 13. Typical Start-Up (ILED = 515 mA, VOUT = 12.3 V, VIN = 12 V)

13.4 Line Step Response

Line step response across the buck/boost region is shown in Figure 14.

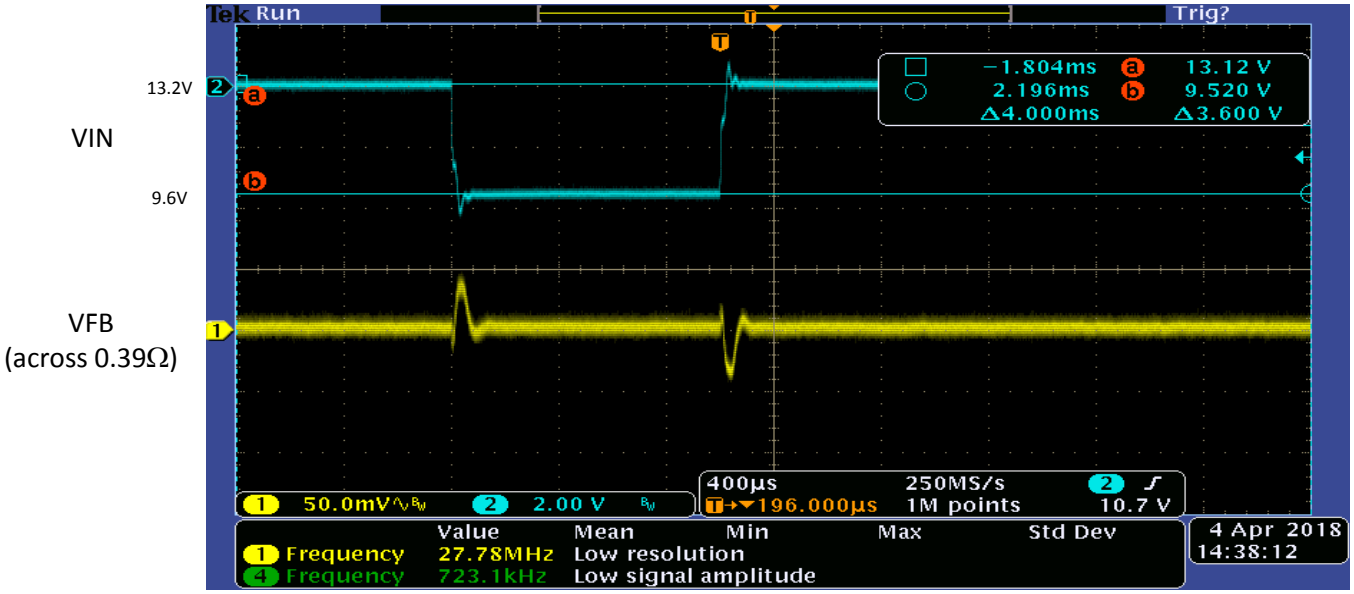

Figure 14. Line Step (13.2 V to 9.6 V), VOUT = 12.3 V, ILED = 500 mA

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5. LLoyd Dixon, High Power Factor Preregulator Using the SEPIC Converter (Unitrode Seminar/Texas Instruments SLUP103)
6. Elena Niculescu/Dorina-Mioara Purcaru/M.C. Niculescu, A Steady State Analysis of PWM SEPIC Converter (Proceedings of the 10th WSEAS International Conference on CIRCUITS, Vouliagmeni, Athens, Greece, July 10-12, 2006 (pp 217-222))

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