Application Report
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TPS65987DDH Power Path Performance and Protection

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ABSTRACT

There are many non-compliant PD (Power Delivery) devices available in the market that do not correctly follow the USB PD specification. These devices could severely damage systems by pulling too much current, shorting VBUS to ground, or by having 20 V on VBUS on initial plug in. The TPS65987DDH protects against all of these non-compliant devices while still being able to operate with them. This document describes the functionality of the overcurrent protection (OCP) mechanism of the TPS65987DDH device and how to program it using the *Application Customization Tool*. This guide defines the peak current and provides steps on how to set the threshold of OCP on the TPS65987DDH device as well as configuring the various protection settings.

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1 Introduction

Through the introduction of USB Power Delivery (PD) the capabilities of each USB Type-C port was greatly expanded. Each USB Type-C port can now support bidirectional power up to 100 W. This allows for devices to be charged from multiple different ports. When supporting complex USB Type-C and PD power architectures, it is crucial to have adequate protection circuitry to prevent reverse current, overcurrent, overvoltage, or undervoltage. Texas Instruments TPS65987DDH PD controllers have integrated high voltage power paths with full protection built in.

1.1 Related Documents

- TPS65987DDH Dual Port USB Type-C & USB PD Controller, data sheet
- TPS65987DDH Host Interface Technical Reference Manual

2 Typical Power Path Applications

On the TPS65988DH, the two internal power paths are commonly used as the power source paths for each of the Type-C ports. Per the USB Power Delivery specification, it is mandatory to have power path protection on the power source path. The TPS65988DH integrates this protection on the internal power paths which makes setting up this application simple. If the application requires both source and sink power paths for each port, the TPS65988DH supports the control of two external PFET power paths. It is recommended to add external reverse current protection for the external power paths.

The TPS65987DDH is a single port Type-C and PD controller that contains two internal power paths. Applications using the TPS65987DDH can easily use the two internal power paths to cover both source and sink use cases. No external protection circuitry is required when using both power paths on the TPS65987DDH.

3 Overcurrent Protection (OCP) and Overcurrent Clamping (OCC)

3.1 FW OCP vs HW OCP

The TPS65987DDH implements overcurrent protection through both firmware (FW) and hardware (HW). This dynamic overcurrent protection allows the TPS65987DDH to safely protect the system while still being able to pass through large inrush currents seen by some non-compliant PD devices available in the market.

When initially connecting a device to a TPS65987DDH, the TPS65987DDH will enable the configured source power path to output 5 V. When 5 V is on VBUS, the TPS65987DDH will implement both overcurrent clamping as explained in Section 3.2.1 and also the hardware overcurrent protection as highlighted in Section 3.3. The overcurrent clamping is implemented for 5 V power contracts as the 5 V rail is typically shared by numerous devices in the system. The overcurrent clamping at 5 V will prevent the 5 V rail from dropping too low when a large current is applied on VBUS and browning out other devices in the system. The overcurrent clamp trip point is configurable through the Application Customization GUI tool as highlighted in Section 3.2.1. If a current greater than 10 A is seen on VBUS during a 5 V contract, the hardware OCP will open the VBUS FET to protect the system.

When negotiating a high voltage contract on VBUS (VBUS > 5 V), the TPS65987DDH will dynamically adjust the hardware OCP trip point from 10 A to 20 A while the VBUS voltage is transitioning from 5 V to the negotiated high voltage level. This mechanism is implemented as there are many PD devices available in the market that will draw a very large amount of inrush current when the VBUS voltage transitions. After the voltage transition is complete, the hardware overcurrent protection trip point will return to 10 A. During a high voltage contract, the TPS65987DDH will implement overcurrent protection through firmware. The FW OCP is a running average of the current through the internal FET during the last 10 ms. If the average current going through the FET during the last 10 ms of operation is greater than the PDO current setting highlighted in Section 3.2.1, the TPS65987DDH will open the FET.

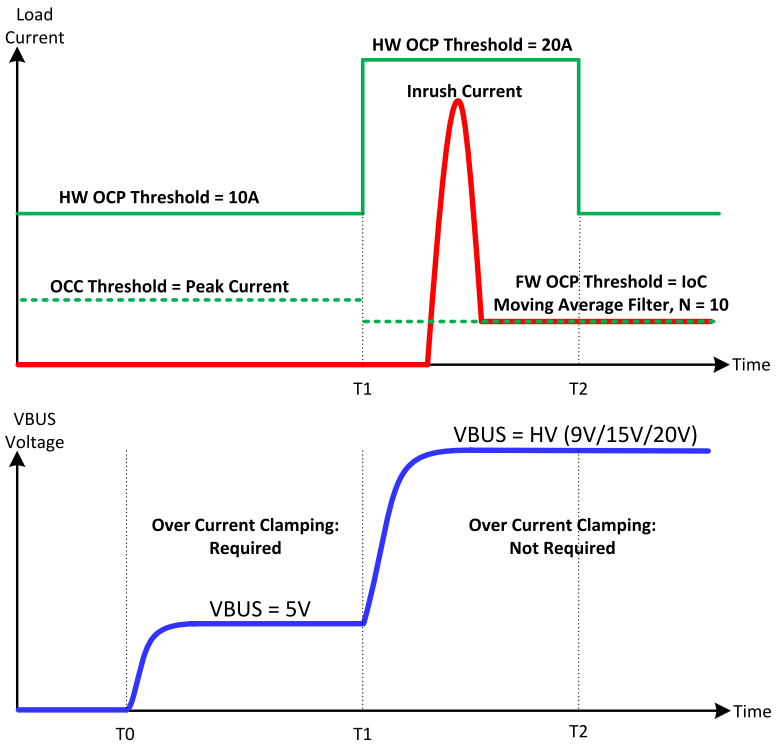


Figure 1. FW OCP vs HW OCP

Figure 1 highlights how the FW and HW OCP work together to protect the system from various overcurrent conditions. The blue line represents the VBUS voltage, the red line represents the VBUS current and the green line shows the HW OCP Trip point setting. When 5 V is on VBUS, you can see that the HW OCP is set to 10 A and the overcurrent clamping is implemented and set to the peak current PDO setting highlighted in Section 3.2.1. When the voltage on VBUS begins to transition to a high voltage contract, the HW OCP trip point is changed from 10 A to 20 A to allow for large inrush spikes to pass through. These inrush spikes are seen with non-compliant PD devices that are available in the market today. Once the voltage on VBUS has settled, the HW OCP trip point will return to the 10 A setting. The timing between T1 (Voltage begins to rise) and T2 (HW OCP setting returns to 10 A) is roughly 100 ms. It can also be seen in Figure 28 that the FW OCP running average filter is implemented for high voltage VBUS contracts (VBUS > 5 V). This will check the current on VBUS for the last 10 ms and if the average current is over the PDO Setting highlighted in Section 3.2.1, the TPS65987DDH will open the FET.

The following sections will highlight the differences with HW OCP and FW OCP as well as show examples of OCC.

3.2 FW OCP

3.2.1 Overcurrent Clamping (OCC) and “Soft Short” Protection

When the TPS65987DDH is sourcing 5 V on VBUS, the TPS65987DDH integrates overcurrent clamping into the power paths. In most customer systems, the 5 V rail is shared by many devices and cannot risk browning out due to an overcurrent event on VBUS. The overcurrent clamp point is programmable through the configuration tool. During an overcurrent clamping protection event, the TPS65987DDH will clamp the current on VBUS at the programmed value by regulating the gate of an internal FET to increase the Rds On. It will then open the power path once a deglitch timer of 640 µS has reached 0 and the current still exceeds the overcurrent clamp point. The 640 µS countdown serves as an overcurrent clamp deglitch to ensure the overcurrent clamp protection is not too sensitive.

The TPS65987DDH clamps current on implicit Type-C contracts and also PD contracts. With an implicit Type-C contract, the overcurrent clamp point is configured in the Port Control register (0×29). Setting the "Type-C Current" field adjusts the pull-up resistance on the CC line to determine the allowed current with a default Type-C connection. The strongest pull-up allows for 3000 mA, the medium pull-up allows for 1500 mA, and the weakest pull-up allows for 900 mA.

Figure 2. 3000 mA Type-C Current Setting

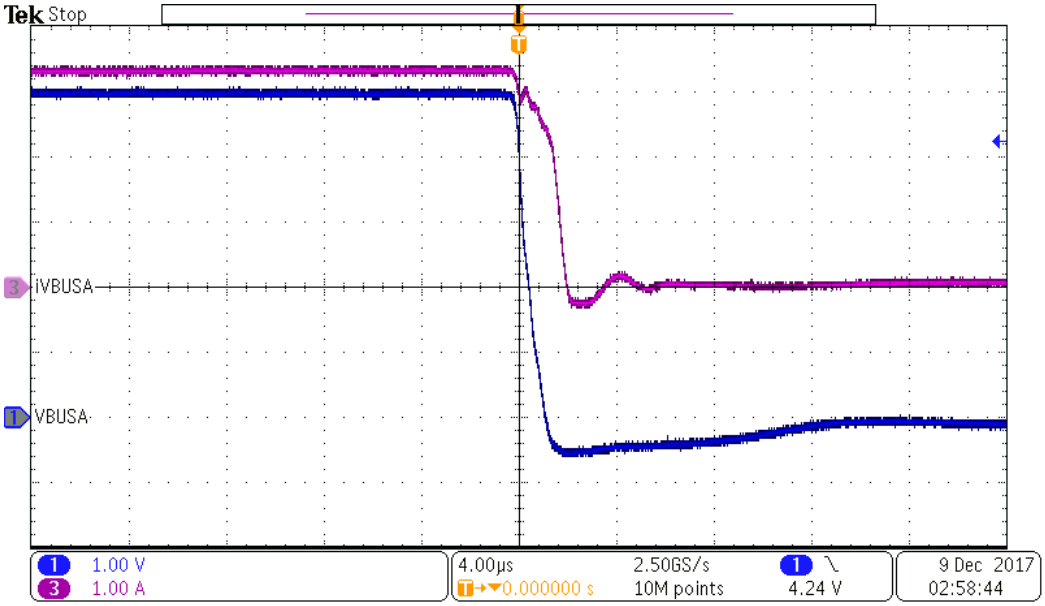


Figure 2 highlights the overcurrent clamp point with a default Type-C connection and the strongest pull-up setting to allow for 3000 mA. As seen, the power path opens just after the current exceeds 3000 mA for over 640 µS. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7.

Figure 3. 1500 mA Type-C Current Setting

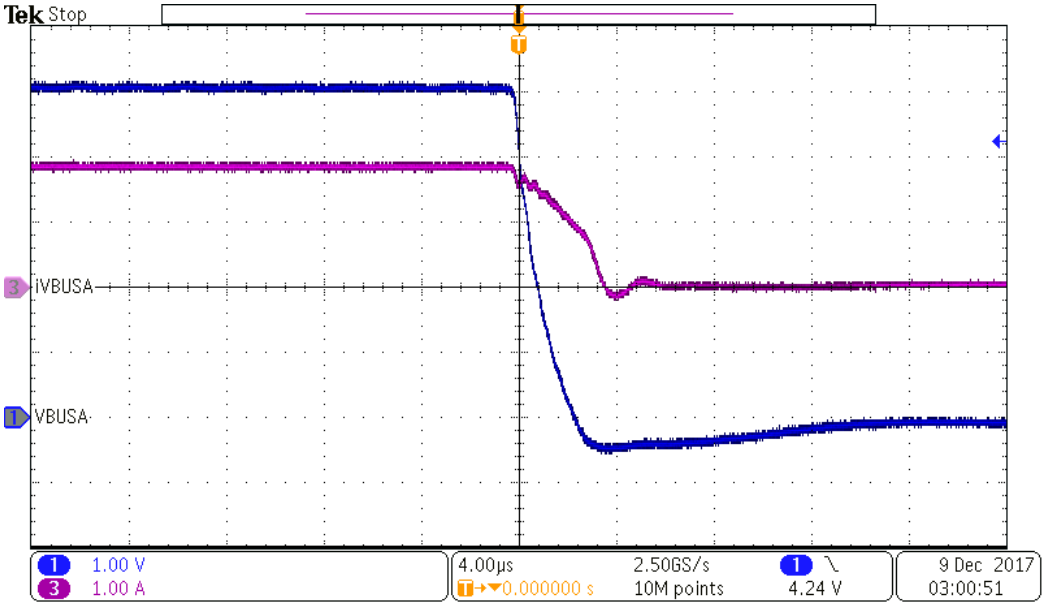


Figure 3 highlights the overcurrent clamp point with a default Type-C connection and the strongest pull-up setting to allow for 1500 mA. As seen, the power path opens just after the current exceeds 1500 mA for over 640 µS. Once the FET has opened, the TPS65987DDH enters the error recovery state as described in Section 7.

Figure 4. 900 mA Type-C Current Setting

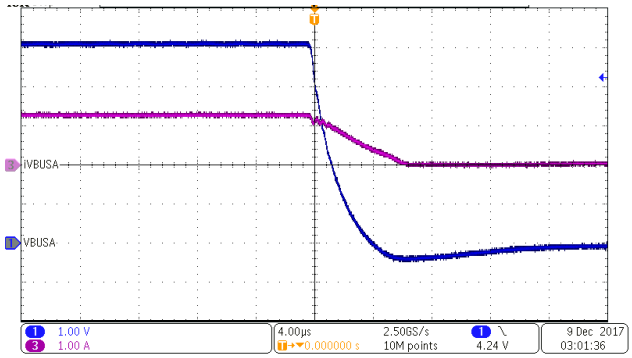


Figure 4 highlights the overcurrent clamp point with a default Type-C connection and the strongest pull-up setting to allow for 900 mA. As seen, the power path opens just after the current exceeds 900 mA for over 640 µS.

Adjusting the overcurrent clamp point for a PD contract allows for more flexibility and for larger current levels. In Type-C Power Delivery (PD), the Power Source is responsible for providing overcurrent protection. If the Power Source has a Source Capability of 5 V at 3 A and the Sink requests only 5 V at 1 A, it is the responsibility of the power source to clamp the current at 1 A.

The overcurrent clamp point for a PD contract can be adjusted in the Transmit Source Capabilities register (0×32) in the Application Customization Tool. The maximum current field can be set between 0 and 10.23 A with 10 mA increments. The peak current percentage field in the Transmit Source Capabilities can be used to increase the OCP trip point. For example, if you set a 5 V and 3 A Source Capability with 200% peak current, the overcurrent clamp point will be set around 6 A. The settings for changing the overcurrent clamp point are highlighted in Figure 5. Section 3.2.2 describes how the internal firmware sets the actual overcurrent clamp point based on GUI setting.

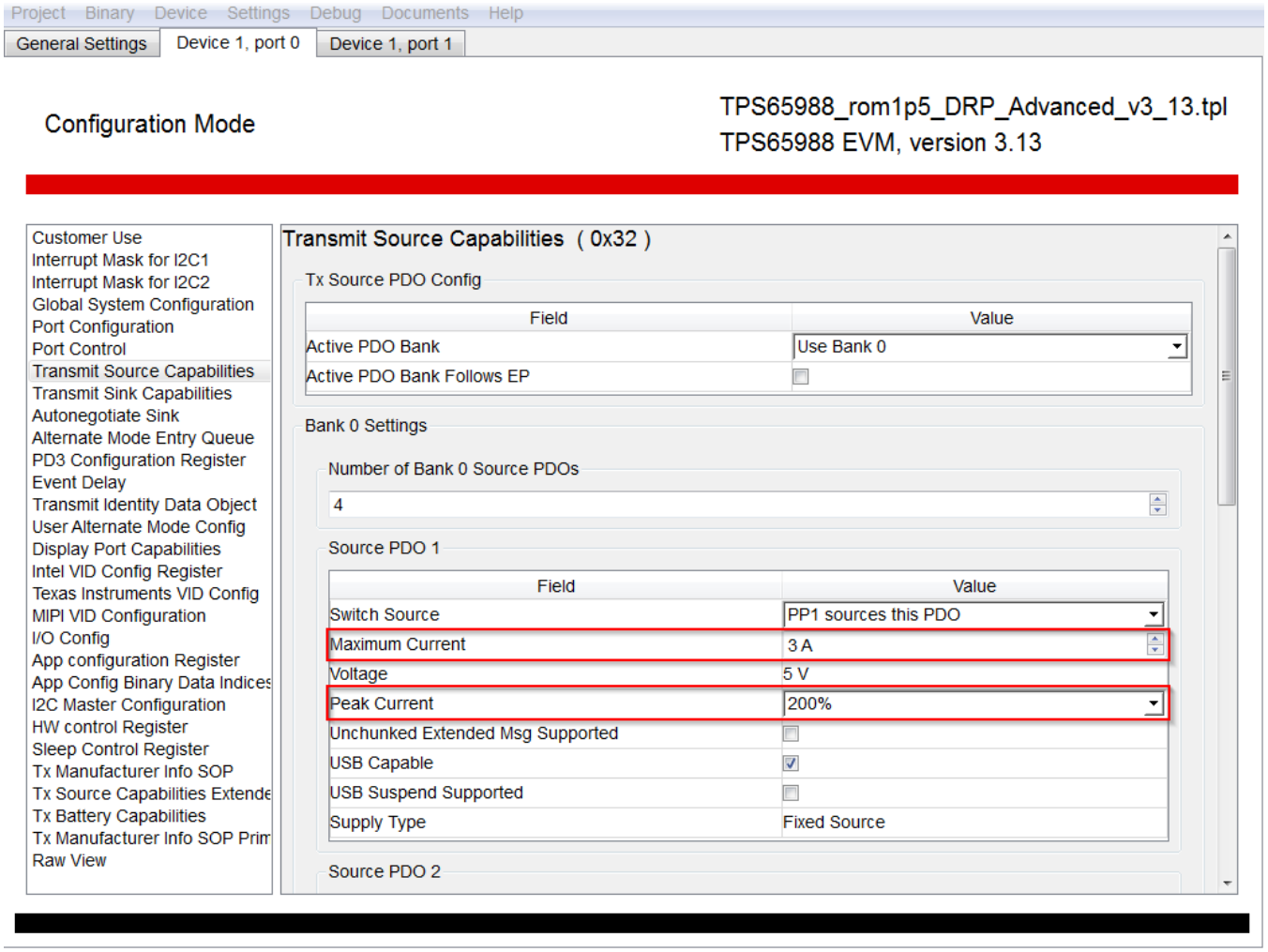


Figure 5. Overcurrent Clamp Trip Point Setting in Configuration Tool

Figure 6. 5 V 1 A OCP

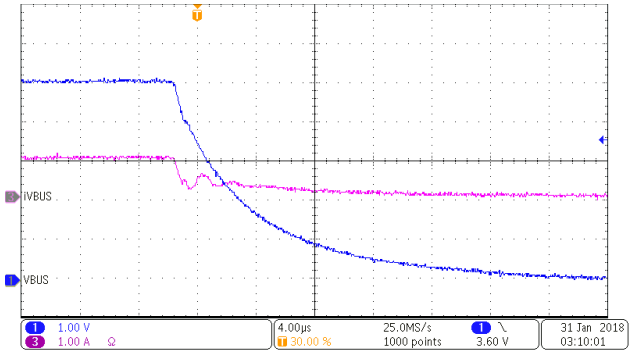
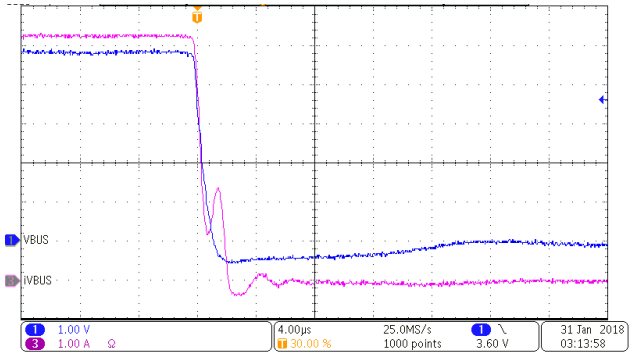


Figure 6 highlights the overcurrent clamp behavior with a 5 V 1 A PD contract. As seen in the scope capture, the current on VBUS trips after the current was above 1 A for more than 640 µS. Once the overcurrent clamp timeout reaches 0 to ensure the overcurrent clamp condition, the power path will open and VBUS will discharge to 0 V. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7.

Figure 7. 5 V 3 A PD Contract with 200% Peak Current



As explained earlier in this section, setting a 5 V at 3 A source capability with 200% peak current will set the overcurrent clamp point at 6 A. Figure 7 highlights the results of the 200% peak current setting. As seen, the overcurrent clamp opens the switch after more than 6 A of current was present on VBUS for more than 640 µs.

The VBUS FET in the TPS65987DDH will try to maintain a constant current across it from PPHV to VBUS when a soft short occurs. A soft short is when a load is present on VBUS that is below the 10 A hard short limit. When a soft short is present, the TPS65987DDH will start the 640 µs overcurrent clamp timeout before opening the FET. During this 640 µs, the TPS65987DDH will try to maintain a constant current across the FET. To do this, it will drop the voltage on VBUS slightly by increasing the Rds On of the internal FET.

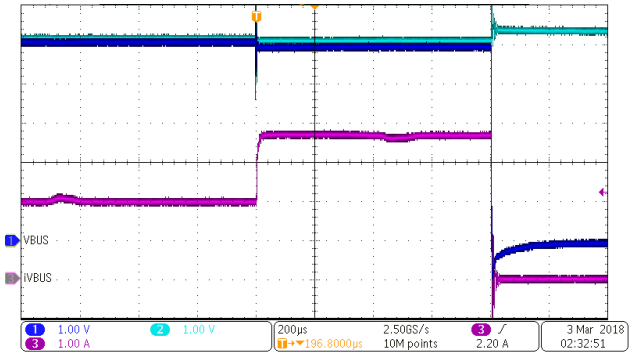


Figure 8. 5 V and 3 A PD Contract 3.75 A Soft Short Behavior

Figure 8 highlights the behavior of the TPS65987DDH when there is a 3.75 A load going through the internal FET when it is configured for a 5 V and 3 A PDO. It is observed that the voltage on VBUS drops slightly while the soft short condition is present. As soon as the 640 µs timer has hit 0, the VBUS FET opens and it is observed that both VBUS and the current through the FET go to 0. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7. This test case has an initial load of 2 A present which was then stepped to 3.75 A.

NOTE: Overcurrent Clamping is only implemented when the TPS65987DDH is sourcing 5 V on VBUS

3.2.2 How Overcurrent Clamp Setting in GUI Relates to Overcurrent Clamp Setting in the

TPS65987DDH

The data sheet for the TPS65987DDH contains a graph with “Overcurrent Clamp Firmware Selectable Settings” for I_{OCC} as shown below in Table 1. When using the Application Customization Tool to program the overcurrent clamp point, the internal firmware will select one of these programmable settings as the overcurrent clamp point. For example, when setting the overcurrent clamp point to 3 A with 100% Peak current, the internal firmware will select the setting with the minimum trip point of 3.060 A and maximum of 3.74 A. With that, the TPS65987DDH would clamp current at a minimum of 3.060 A and a maximum of 3.74 A when set for a 3 A PDO with 100% peak current. However, if setting the overcurrent clamp point in the Configuration Tool to 3.10 A, the internal FW would have to select the setting with a minimum of 3.30 A and maximum of 4.033 A as we cannot clamp the current before the selected setting. This means that the overcurrent clamp point for a 3.10 A PDO with 100% peak current would be between 3.30 A and 4.033 A.

Likewise, setting a PDO in the configuration tool to 3 A with 200% peak current would equate to a 6 A setting. The internal firmware in that case would select the I_{OCC} programmable setting to be the one with the minimum setting of 6.180 A and the maximum setting of 7.553 A. That means the overcurrent clamp point would be between 6.180 A and 7.553 A for a PDO set to 3 A with 200% peak current

Table 1. I_{occ} Programmable Settings for Overcurrent Clamp Point

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCC}	Overcurrent Clamp Firmware Selectable Settings		1.140	1.267	1.393	A
			1.380	1.533	1.687	A
			1.620	1.800	1.980	A
			1.860	2.067	2.273	A
			2.100	2.333	2.567	A
			2.34	2.600	2.860	A
			2.580	2.867	3.153	A
			2.820	3.133	3.447	A
			3.060	3.400	3.74	A
			3.300	3.667	4.033	A
			3.540	3.933	4.327	A
			3.780	4.200	4.620	A
			4.020	4.467	4.913	A
			4.260	4.733	5.207	A
			4.500	5.00	5.500	A
			4.740	5.267	5.793	A
			4.980	5.533	6.087	A
			5.220	5.800	6.380	A
			5..460	6.067	6.673	A
			5.697	6.330	6.963	A

3.3 Hardware Overcurrent Protection (HW OCP)

In the USB PD specification, the power source is required to implement overcurrent protection. An overcurrent event can be caused by many things such as a device pulling too much current from VBUS, or VBUS accidentally getting shorted to ground. Protection against these events is integrated in the TPS65987DDH. All of the power path testing was completed with the TPS65987DEVM. To test the overcurrent protection of the TPS65987DDH, the standard PD contracts (5 V, 9 V, 15 V, and 20 V) were negotiated and VBUS was shorted directly to ground through a cable. The TPS65987DEVM uses the LM3489 variable DC/DC regulator to control the voltage at PPHV.

Figure 9. Overcurrent Protection Test Setup

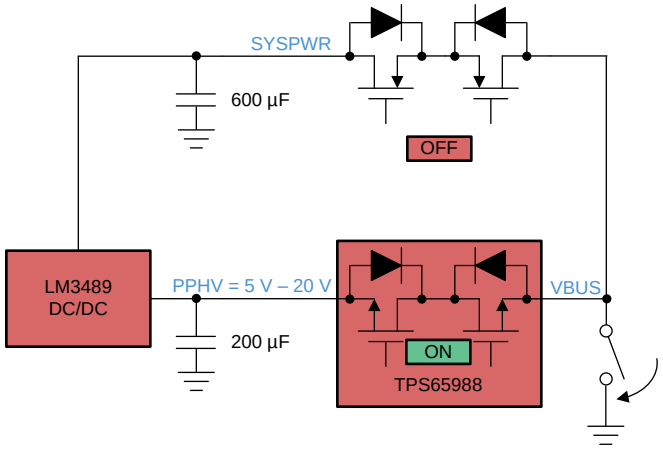
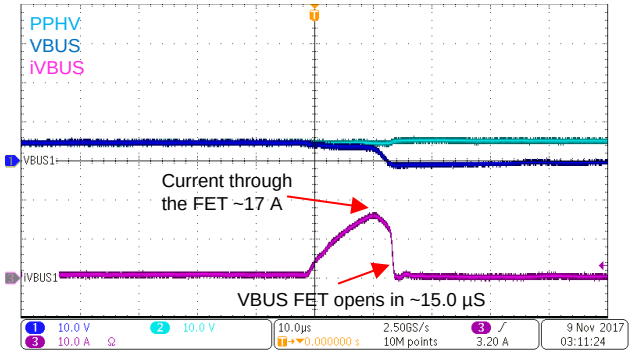


Figure 9 highlights the test setup used when completing the overcurrent protection testing. C1 is the capacitance on the output of the DC/DC that is supplying PPHV. When a PD contract is established, the internal FET will close and pass 5 V from the DC/DC to VBUS. When a short is applied on VBUS, the FET inside the 88 should open as quickly as possible to not let the DC/DC voltage drop too low and brownout the system. Typical operating voltage for devices powered by a 5 V rail range from 4.5 to 5.5 V. So ideally, the voltage at the output of the DC/DC which is PPHV in this case, should not drop below approximately 4.5 V in the event of a VBUS short to ground. Adding capacitance at C1 will help mitigate the effects of a fast transient that could be caused by a VBUS short to ground.

The overcurrent trip point is set dynamically in the TPS65987DDH and the setting of this value is optimized through the internal firmware. The measurements shown above are with the overcurrent protection trip point set at 30 A to highlight the performance of the internal FET and overcurrent protection circuit reaction time. Typically, the overcurrent protection point is set at 10 A. However, when a high voltage PD contract is negotiated and VBUS begins to transition from 5 V to the negotiated high voltage, the overcurrent protection point will change from 10 A to 20 A during the voltage transition and return to 10 A once the voltage has settled. There are many non-compliant devices available in the market today that draw a very large amount of inrush current during this voltage transition. By dynamically changing the overcurrent protection point during a voltage transition, we can pass through the large inrush drawn by the PD consumer without breaking the connection. The overcurrent protection point is changed to 2A when we receive the “Request” message in PD traffic and returns to 10 A 100 ms after the request message.

3.3.1 HW OCP with VBUS = 5 V

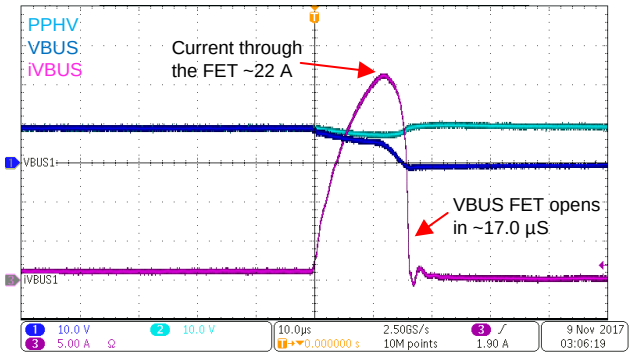
Figure 10. Overcurrent Protection with VBUS = 5 V



A smaller C1 capacitance of 120 µF is present on the TPS65987DEVM. A larger capacitance prevents the fast transient from affecting the DC/DC output too much. The voltage at PPHV only drops to 4.6 V here. The Internal VBUS FET is able to open in less than 15 µS during the event of a VBUS short to ground as seen in Figure 10. The faster this timing is, the better it will protect the system. Typical external FET paths will take longer than 150 µS to open during a hard short. This can allow significant damage to the system as the PPHV voltage will tank with a VBUS short to ground. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7.

3.3.2 HW OCP With VBUS = 9 V

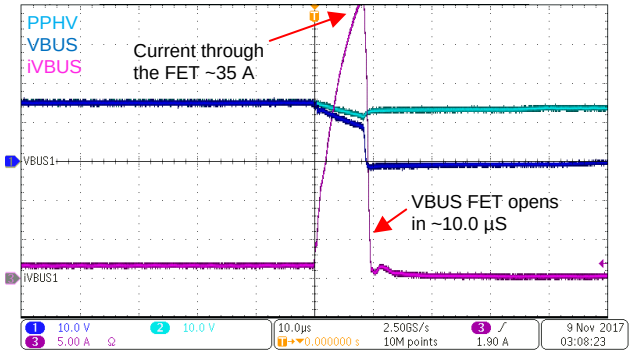
Figure 11. Overcurrent Protection with VBUS = 9 V



As the voltage on VBUS increases, the current seen on the VBUS power path during a hard short increases. Figure 11 highlights the performance of the overcurrent protection when VBUS is 9 V. The power path is able to open within 17 µs and the current through the power path is roughly 22 A. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7.

3.3.3 HW OCP With VBUS = 15 V

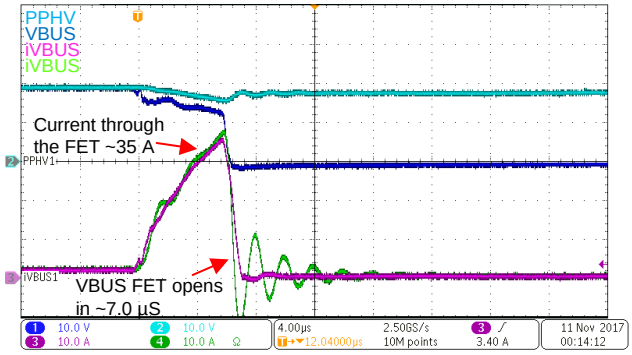
Figure 12. Overcurrent Protection with VBUS = 15 V



When VBUS is 15 V, the current spike on VBUS is exceeding 30 A. However, the TPS65987DDH is able to open the VBUS FET within 10 µs. The TPS65987DDH has a hardware interrupt set to open the power path once the current exceeds 30 A. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7.

3.3.4 HW OCP With VBUS = 20 V

Figure 13. Overcurrent Protection with VBUS = 20 V



A VBUS short to GND at 20 V is a tricky short to protect against. In Figure 13, the time scale on the oscilloscope was decreased to better observe the current spike and timing to open the power path. With a 20 V short, the current increases very rapidly, the analog circuitry catches it when it exceeds 30 A and immediately opens the power path. This all happens in less than 7 µs and the system remains protected from the short to ground. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7.

4 Reverse Current Protection

When designing a complex power architecture with the intention of supporting multiple different source and sink paths. It is crucial to ensure that each power path is protected from reverse currents. In this example, a two port notebook is being emulated, using two TPS65987DEVMs configured as TPS65987DDH.

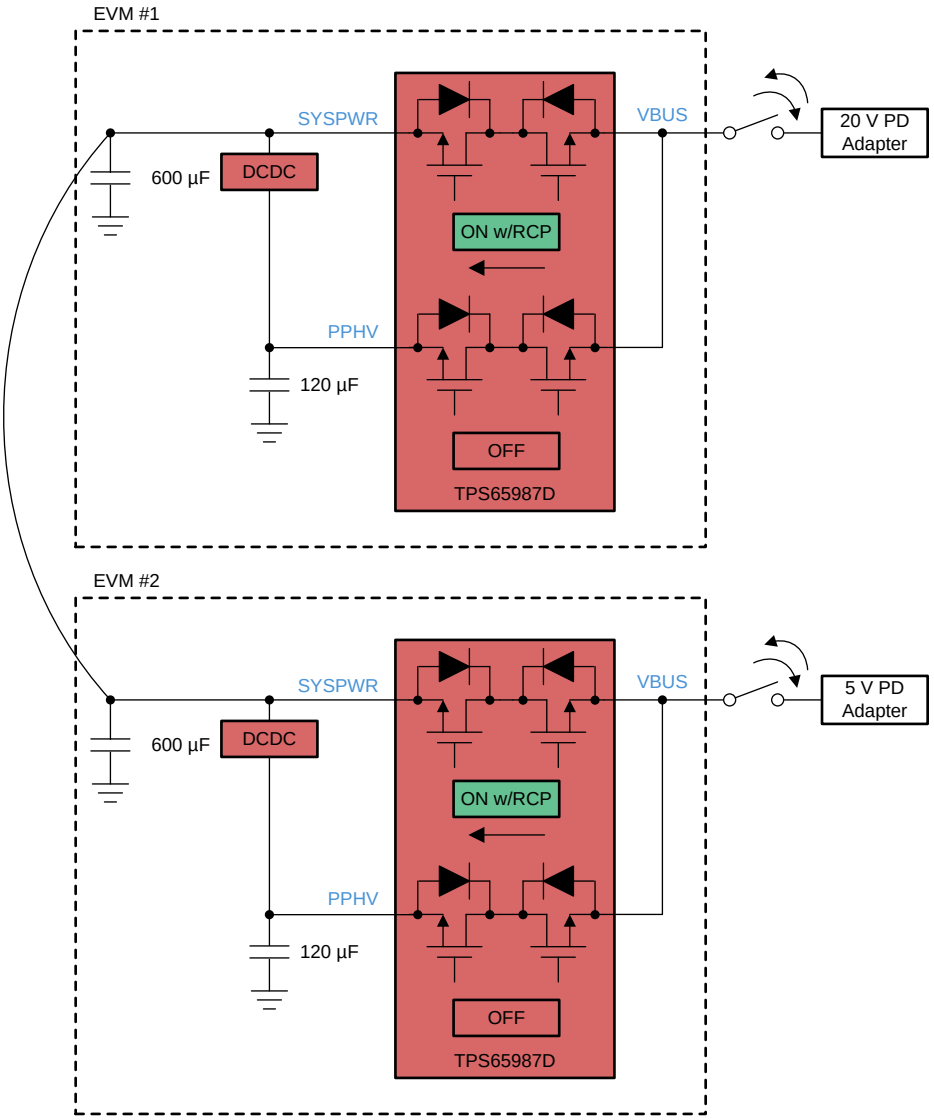


Figure 14. Reverse Current Protection Test Setup

In two port systems, what is connected to port 1 should have no transverse effects on port 2. In the diagram above, both power paths are closing onto the same SYSPWR rail. When a 5 V adapter is plugged into port 2 and a 20 V adapter is plugged into port 1, port 2 will have to enable reverse current protection. In this scenario, the SYSPWR voltage is higher than the VBUS voltage offered by the 5 V PD adapter connected in port 2. With no RCP, the 5 V PD adapter would be back fed with 20 V, causing damage to it and potentially to the system. The TPS65987DDH has internal back-to-back VBUS FETs, in this RCP event, port 2 VBUS FET will enable one of the back-to-back FETs and disable the other one as a “Blocking” FET. This will prevent any current being back fed into the 5 V PD adapter from the SYSPWR rail. If the 5 V Adapter is connected into port 2 and the 20 V adapter is connected into port 1, the port 2 FET will be in RCP. If someone disconnects the 20 V PD adapter on port 2, the port 1 FET will have to come out of RCP once the SYSPWR rail drops to 5 V to start supplying power to SYSPWR. The TPS65987DDH can do this fast enough to not let SYSPWR rail drop below 5 V. This is known as “Fast Recovery RCP”

Figure 15. Reverse Current Protection Test Results

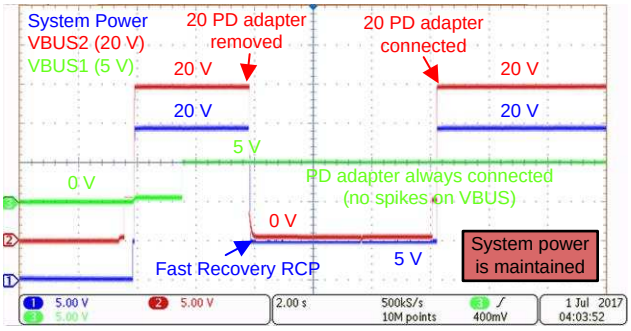


Figure 15 highlights the results of the RCP testing. Initially, a 20 V PD adapter is connected to port 1. When only the 20 V PD adapter is present, the SYSPWR rail will go to 20 V. Afterwards, a 5 V PD adapter is connected to the port 2 while the 20 V PD adapter is still present on port 1. In this case, the 20 V PD adapter on port 1 will be supplying SYSPWR and the port 2 will be held off in RCP as it has a lower power contract negotiated.

Once the 20 V PD adapter is removed from port 1 with the 5 V adapter still present on port 2, the SYSPWR rail will drop to 5 V as that is now the highest power available. When SYSPWR is dropping after the 20 V PD adapter is removed, the TPS65987DDH monitors the system side voltage and waits until SYSPWR has reached 5 V before enabling the power path with the 5 V PD adapter. This prevents any potential for reverse current damage to the 5 V PD adapter and the system.

With the 5 V PD adapter is still connected on port 2, the 20 V PD adapter is reinserted in port 1. The PD Controller for port 1 will enable the sink path and the SYSPWR will rise to 20 V. While this is occurring, the PD Controller for port 2 is monitoring the system side voltage, once it observes the system voltage rise above 5 V, it will immediately enable the RCP circuitry to protect the 5 V PD adapter from any reverse currents.

Figure 16. RCP 0 to 5 V Zoomed in Transition

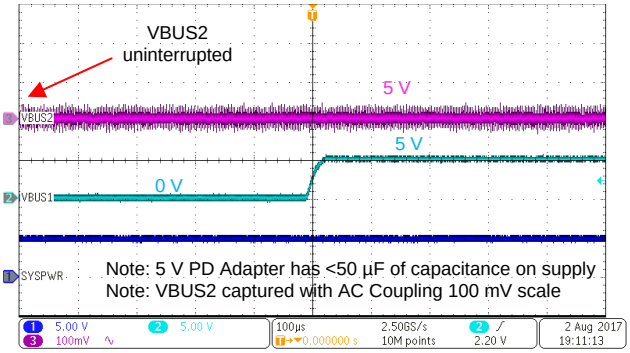


Figure 16 shows a zoomed in plot where there is initially a 5 V PD adapter connected on port 2 and a second 5 V PD adapter is added onto port 1. In this case, the port 1 5 V PD adapter is held off in RCP. The scope capture highlights that the voltage on VBUS 2 is unaffected by the PD adapter connected on VBUS 1. Please note that the voltage scale for VBUS 2 is 100 mV per division.

Figure 17. RCP 5 V to 20 V Zoomed in Transition

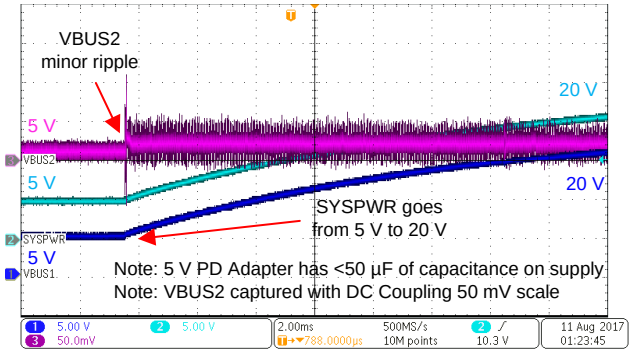
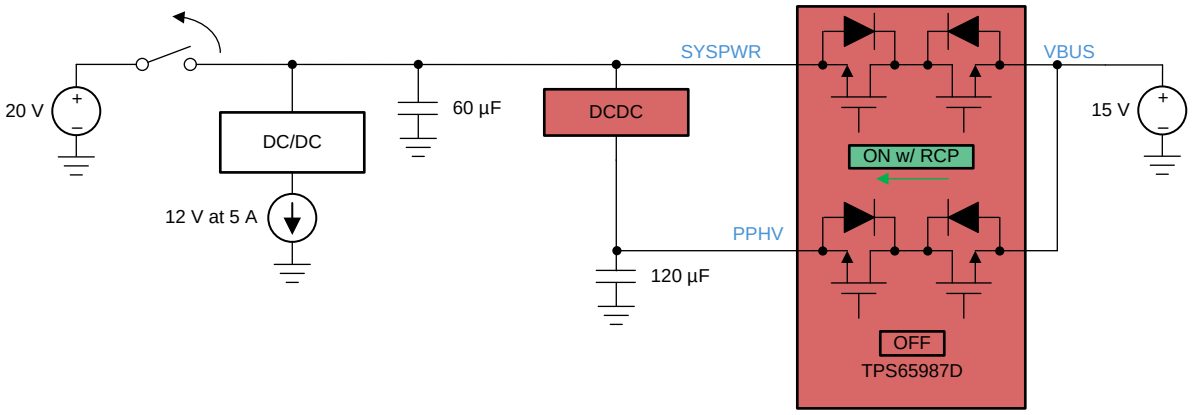


Figure 17 shows a zoomed in plot where there is initially a 5 V PD adapter connected on port 2 and a 20 V
PD adapter is then connected into port 1. The voltage on VBUS1 is transitioning from 5 V to 20 V here after the PD Controller has completed negotiating the higher voltage contract. Initially VBUS2 is carrying the system load and there is very little ripple on the 5 V supply. Once the PD adapter on port 1 (VBUS1) exceeds 5 V, the VBUS2 quickly enables RCP. The small spike seen in the scope capture is caused by the sudden disconnect of the system load when the power path is blocked by RCP. The System Power Rail is now being supplied by the VBUS1 20 V PD adapter and SYSPWR rises in parallel with VBUS1. Please note the 50 mV per division scale on VBUS2.

4.1 Fast Recovery RCP with System Loading

As previously highlighted in Section 4, the TPS65987DDH uses fast recovery RCP to keep the system alive when VBUS voltage changes. In a real world system, there will always be a load on the system power rail. When VBUS is the only source of power for the system power rail, the device will rely on the TPS65987DDH's fast recovery RCP feature to keep the system alive when the VBUS voltage changes. A real world example of this would be a laptop with no battery connected.

Figure 18. Fast Recovery RCP with System Loading Test Setup



As seen in Figure 18, a DC/DC converter was attached to SYSPWR to ensure the load was a constant power load and not a constant current load. Most end equipment will draw a constant power from their system power rail through a DC/DC to ensure that the other IC's in the system receive a constant voltage. This dynamic load better simulates the conditions in an end equipment. The amount of capacitance on the system power rail is only 60 µF. Generally, systems will have a minimum of 100 µF on the system power rail to better handle voltage transitions. The following experiment highlights a worst case scenario. Originally, an external 20 V supply is powering SYSPWR while a 15 V PD adapter is held off in RCP. When the 20 V supply gets removed, the 15 V PD adapter will need to come out of RCP when the SYSPWR rail is dissipated to 15 V to start supplying the DC/DC.

Figure 19. Fast Recovery RCP with System Load Test Results

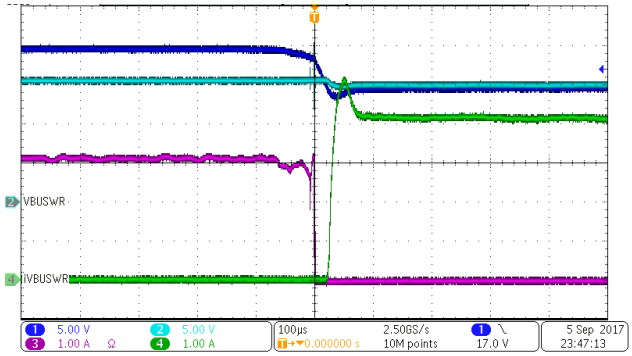


Figure 19 highlights the results of the Fast Recovery RCP test with a constant power System load. Initially, the system load is carried by the external 20 V power supply that is connected to the SYSPWR node of the TPS65987DEVM. The external DC/DC is being loaded with 5 A through a constant resistant load. With the DC/DC outputting 12 V, the load on the SYSPWR rail is 60 W. In the scope capture, it can be observed that initially, SYSPWR (dark blue) is at 20 V and the current on SYSPWR (Magenta) is roughly 3 A. Once the external 20 V supply is removed from SYSPWR, the 15 V PD adapter on VBUS comes out of RCP and begins to supply SYSPWR. The scope capture highlights that the current swaps to VBUS and SYSPWR drops to 15 V to match VBUS. Here, SYSPWR is roughly 15 V and the current on SYSPWR is roughly 4 A and the power drawn remains constant.

5 Over-Voltage Protection (OVP)

The TPS65987DDH also integrates overvoltage protection (OVP) on both the internal and external power paths. The TPS65987DDH monitors the VBUS voltage actively during run-time and will open the FET when the voltage exceeds the expected maximum. The OVP trip point is configurable through the application customization tool and can be set to trip at 5%, 10%, or 15% of the expected maximum voltage of the negotiated PD contract. The OVP trip point can also be set to a hard coded value by selecting “Disconnect VBUS if voltage exceeds OVPTripPoint” in the Overvoltage Protection Usage field of the Port Configuration register (0×28). This Overvoltage Trip Point is also configurable in the Port Configuration register.

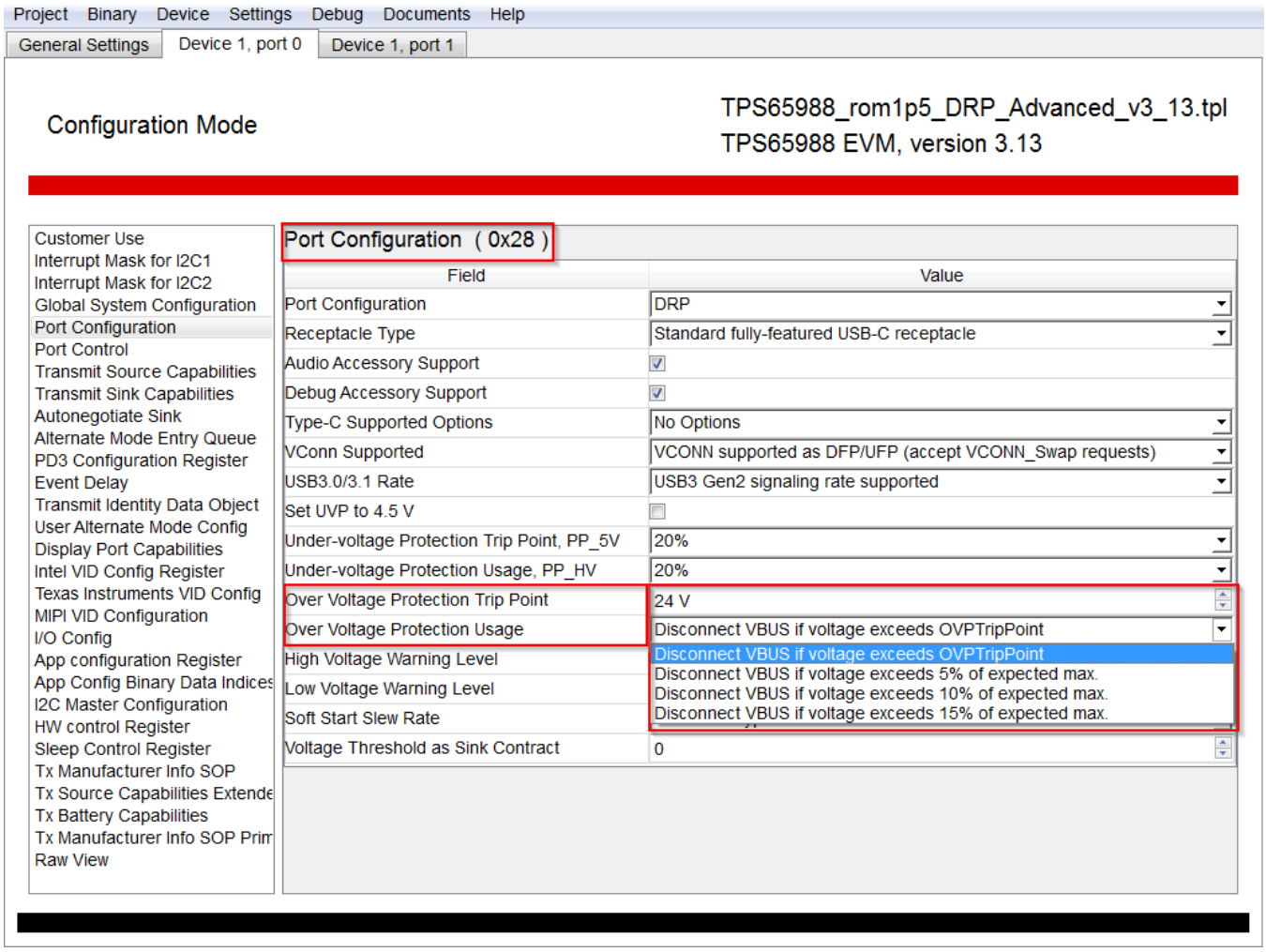


Figure 20. Overvoltage Protection Configuration Registers

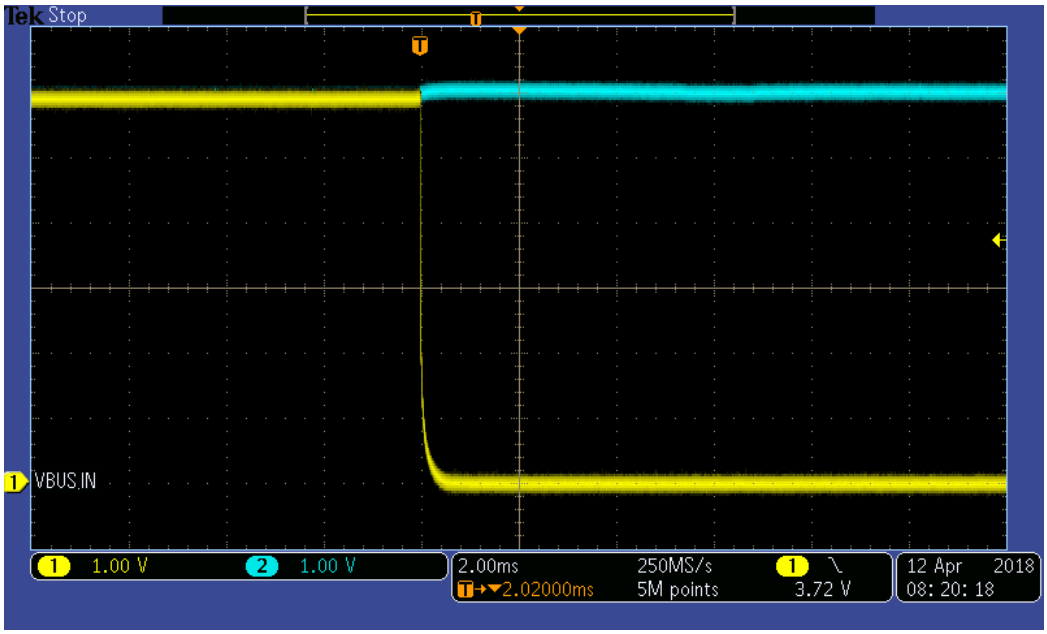


Figure 21. 5 V 5% OVP Trip Point

Figure 21 highlights the response of the OVP circuit with a 5 V PD contract. In this test, the OVP was set to “Disconnect VBUS if voltage exceeds 5% of expected max. With a 5 V contract, the expected max is 5 V + 5% = 5.25 V. After the FET opens, the TPS65987DDH will enter an Error Recovery state as described in Section 7.

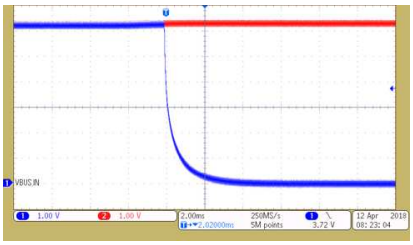


Figure 22. 5 V 10% OVP Trip Point

Figure 22 highlights the response of the OVP circuit with a 5 V PD contract. In this test, the OVP was set to “Disconnect VBUS if voltage exceeds 10% of expected max. After the FET opens, the TPS65987DDH will enter an Error Recovery state as described in Section 7.

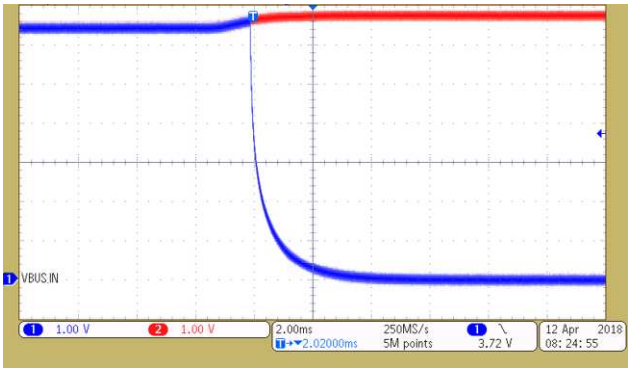


Figure 23. 5V 15% OVP Trip Point

Figure 23 highlights the response of the OVP circuit with a 5 V PD contract. In this test, the OVP was set to “Disconnect VBUS if voltage exceeds 15% of expected max. After the FET opens, the TPS65987DDH will enter an Error Recovery state as described in Section 7.

Setting the “Over Voltage Protection Usage” field to “Disconnect VBUS is voltage exceeds OVPTripPoint” is not a recommended configuration when sourcing 5 V. This setting allows you to select an OVP Trip Point manually that would be applied to any PD source voltage. In this case, if you set the OVP Trip Point to 24 V, you will not open VBUS until the voltage exceeds 24 V. This would even be applied when sourcing 5 V.

The recommended configuration is to set this field to “Disconnect VBUS if voltage exceeds 5% of expected max”. With this setting, the internal firmware will adjust the OVP Trip Point internally based on the source or sink voltage.

5.1 VBUS Ramp On Open Switches

This test will highlight what will happen if a non-compliant PD adapter is connected to the TPS65987DDH. For example, if a PD adapter that has 20 V on VBUS is connected, or a PD adapter has VBUS ramping to 20 V outside of the PD Spec. We should see that I(VBUS) will be very small and only enough to charge the VBUS caps that are present on the PCB. The SYSPWR rail and PPHV should be unaffected as both internal and external FET paths will not enable in this non-compliant event.

Figure 24. VBUS Ramp On Open Switches Test Setup

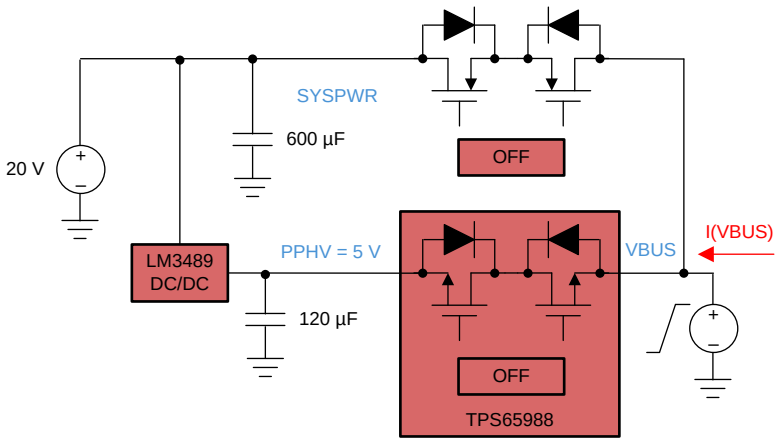
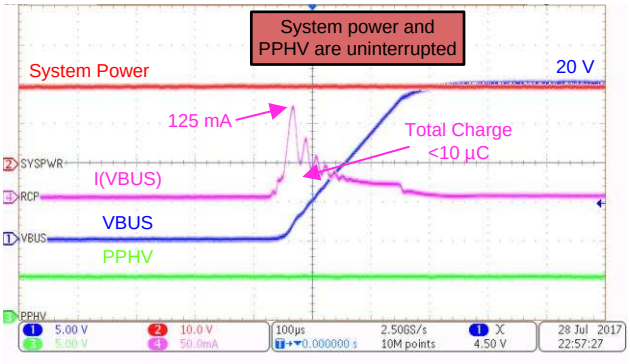


Figure 25. VBUS Ramp On Open Switches Test Results



From the results in Figure 25, the current on VBUS is marginal. When calculating the total charge from the current spike, it is noticed that it is only enough to charge the capacitance present on VBUS. Also, the System Power rail is unaffected by the non-compliant 20 V source on VBUS as the power path remains off. When the power path is off, the blocking diode in the back-to-back FET will isolate the system from any non-compliant behavior on VBUS.

6 Undervoltage Protection (UVP)

The TPS65987DDH integrates undervoltage protection (UVP) for the internal power paths on the VBUS side of the FETs. The UVP trip point is configurable through the configuration tool and is set to a percentage of the nominal voltage. For example, if the VBUS contract is at 20 V with the UVP set at 20%, the UVP is expected to trip around 14.8 V. This is assuming that the minimum expected voltage on VBUS is 18.5 V with a 20 V contract per the USB PD3.0 specification. With a 5% setting, it would be expected that the UVP trips around 17.575 V. With the 50% setting, the UVP should trip around 9.25 V with a 20 V source contract. When operating as a sink, the UVP settings will trip slightly lower to compensate for potential cable losses. Under voltage protection is typically used to disconnect VBUS if the voltage gets too low. When the VBUS FET is enabled as a sink, some devices that are powered by that rail could brown out. The same could happen when operating as a source and the systems 5 V rail dips too low.

Figure 26. VBUS UVP 20 V Source 5%

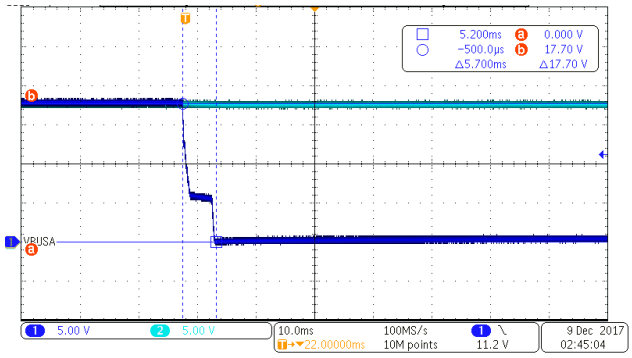


Figure 26 highlights the test results of UVP when setting the TPS65987DDH as a 20 V source with UVP set to 5%. As explained in the previous paragraph, it is expected to trip UVP around 17.575 V with this setting. The scope capture highlights the UVP tripping at 17.7 V with the 5% setting when sourcing 20 V. The internal ADC that is measuring will have a small percentage of error due to the nature of data converters. More details on the internal ADC can be found in the TPS65987DDH datasheet. The TPS65987DDH trips the UVP at the expected point. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7.

Figure 27. VBUS UVP 20 V Source 20%

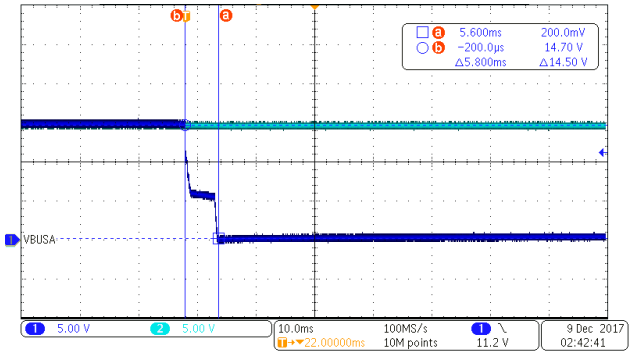


Figure 27 highlights the test results of UVP when setting the TPS65987DDH as a 20 V source with UVP set to 20%. As explained in the previous paragraph, it is expected to trip UVP around 14.8 V with this setting. The scope capture highlights the UVP tripping at 14.7 V with the 20% setting when sourcing 20 V. The TPS65987DDH trips the UVP at the expected point. Once the FET has opened, the TPS65987DDH enters the Error Recovery state as described in Section 7.

Figure 28. VBUS UVP 20 V Source 50%

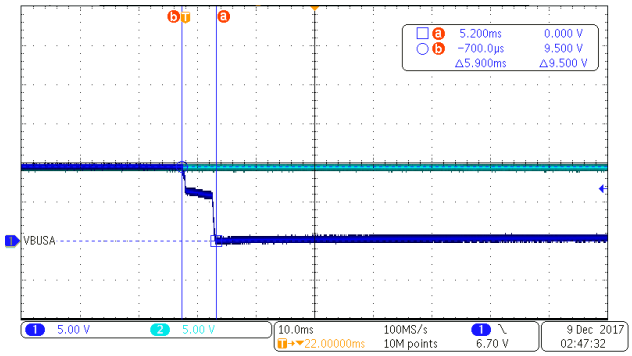


Figure 28 highlights the test results of UVP when setting the TPS65987DDH as a 20 V source with UVP set to 50%. As explained in the previous paragraph, it is expected to trip UVP around 9.25 V with this setting. The scope capture highlights the UVP tripping at 9.5 V with the 50% setting when sourcing 20 V. The TPS65987DDH trips the UVP at the expected point.

The same logic applies to the 5 V UVP trip point. For 5 V contracts, VSafe5Vmin is 4.75 V from the PD spec. With this, 5% UVP should trip around 4.51 V, 20% should trip around 3.8, and 50% should trip around 2.38 V.

7 Error Recovery

When there is a protection event on VBUS such as opening the FET after the overcurrent clamp timeout has reached 0 or opening the FET after an overcurrent protection event, the TPS65987DDH will enter the Error Recovery state as defined in the USB Type-C specification. When the TPS65987DDH enters an Error Recovery state it removes the termination present from the CC1 and CC2 pins for at least 25 mS. During this 25 mS timing, the CC lines shall present a high-impedance to ground as defined in the USB Type-C Spec. After the timeout for Error Recovery has completed, the TPS65987DDH will return to an Unnattached.SNK state or an Unnattached.SRC state depending on the configuration of the port. Error Recovery state can be interpreted as a disconnect and reconnect.

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