Powering the NXP i.MX 8M Mini and Nano with the TPS6521825 and LP873347 PMICs

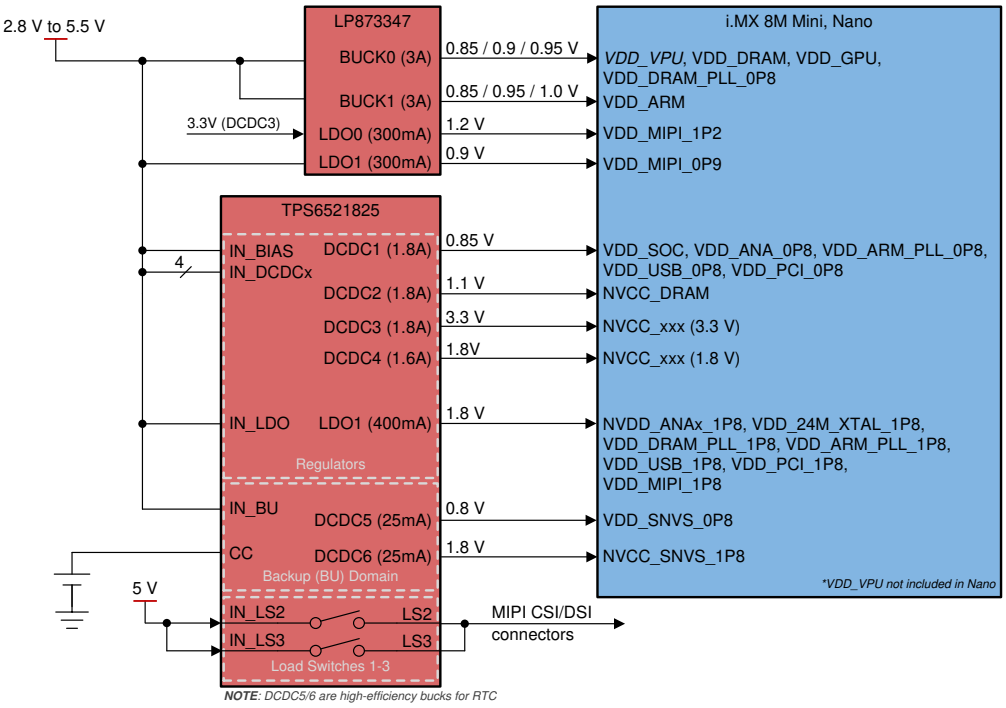

Figure 1. System Power Block Diagram

Can PMICs Be Changed?

Using a multi-rail power management IC (PMIC) for an applications processor is common, but typically the vendor recommends the PMIC that must be used for each processor. Even if the suggested PMIC is not ideal for the needs of the processor, often the complexity makes it difficult to swap out the PMIC for another solution. The purpose of this tech note is to show that the TPS6521825 and LP873347 PMICs can provide power for the i.MX 8M Mini and i.MX 8M Nano processor.

Why the TPS6521825 and LP873347?

The TPS6521825 and LP873347 devices have an input range from 2.8 to 5.5 V, making this solution appropriate for applications powered from a 3.3-V or 5-V DC supply or a Li-Ion battery. The LP873347 device has two step-down converters that provide the dynamic (0.85-V to 1.0-V) power rails required for the ARM® and VPU/GPU/DRAM cores while two 300-mA LDOs provide power for MIPI. The TPS6521825 device has four step-down converters that generate another 0.85-V rail for the SoC core, the 1.2 V (or 1.35-V) rail required for DDR4 (or DDR3L) memory, a 3.3-V rail required for I/Os, and a 1.8-V rail for additional I/Os. A low-dropout (LDO) regulator provides 1.8 V for the processor analog domain at up to 400-mA. The TPS6521825 automatically sequences these rails in the correct power-up sequence for the i.MX 8M Mini and Nano processor.

How Do Designers Make the Switch?

The TPS6521825 output voltages and sequencing order are determined by an EEPROM-backed register map, which are pre-programmed to work with the LP873347 to power the i.MX 8M Mini and Nano processor. To order pre-programmed samples of the TPS6521825RSLR and LP873347RHDR for the NXP i.MX 8M Mini and Nano processor that match this tech note, visit the TPS6521825 product folder and the LP8733 product folder.

Table 1. i.MX 8M Mini, Nano Power Requirements

TPS6521825 and LP873347 PMICs				i.MX 8M Mini, Nano processor		
POWER-UP SEQUENCE	POWER SUPPLY (OUTPUT)	OUTPUT CURRENT [mA]	OUTPUT VOLTAGE [V]	POWER SUPPLY (INPUT)	VOLTAGE RATING [V]	MAX CURRENT [mA]
4	LP873347 Buck0	3000	0.85 / 0.9[(1)] / 0.95	VDD_VPU[(2)], VDD_GPU, VDD_DRAM, VDD_DRAM_PLL_0P8	0.805 (min), 0.9 (max) / 0.855 (min), 0.95 (max) / 0.9 (min), 1.0 (max)	2500
5	LP873347 Buck1	3000	0.85 / 0.95[(1)] / 1.0	VDD_ARM	0.805 (min), 0.95 (max) / 0.9 (min), 1.0 (max) / 0.95 (min), 1.05 (max)	2200
10	LP873347 LDO0	300	1.2	VDD_MIPI_1P2	Minimum: 1.14 Maximum: 1.26	4
4	LP873347 LDO1	300	0.9	VDD_MIPI_0P9	Minimum: 0.855 Maximum: 1.0	256
3	TPS6521825 DCDC1	1800	0.85	VDD_SOC, VDD_ANA_0P8, Misc_0P8	Minimum: 0.805 Maximum: 0.9	1050
8	TPS6521825 DCDC2	1800	1.1[(1)]	NVCC_DRAM	Minimum: 1.14 Maximum: 1.26	≈1500[(3)]
9	TPS6521825 DCDC3	1800	3.3	NVCC_xxx (3.3 V)	Minimum: 3.0 Maximum: 3.6	IO Current
7	TPS6521825 DCDC4	1600	1.8	NVCC_xxx (1.8 V)	Minimum: 1.71 Maximum: 1.89	IO Current
6	TPS6521825 LDO1	400	1.8	VDD_ANAx_1P8, Misc_1P8	Minimum: 0.78 Maximum: 0.9	366
2	TPS6521825 DCDC5	25	0.8[(4)]	VDD_SNVS_0P8	Minimum: 0.76 Maximum: 0.9	10
1	TPS6521825 DCDC6	25	1.8	NVCC_SNVS_1P8	Minimum: 1.62 Maximum: 1.98	3
N/A	TPS6521825 LS2/LS3	1820	5	MIPI CSI, MIPI DSI, other 5-V peripherals	N/A	≈900[(3)]

(1) This is the default value recommended for this design at power-up. VDD_VPU_GPU_DRAM and VDD_ARM require DVFS. NVCC_DRAM also supports DDR4 (1.2 V) and DDR3L (1.35 V), which would require reprogramming the EEPROM register of the TPS6521825 device for DCDC2.
(2) VDD_VPU is not included in the i.MX 8M Nano. All other rails are still present.
(3) The maximum current for this rail is not listed in the i.MX 8M Mini data sheet.
(4) To generate 0.8 V for VDD_SNVS, a resistor divider is used to lower the output voltage of DCDC5.

Table 2. Adjacent Tech Notes

Processor	Title
i.MX 6Solo and 6DualLite	Powering the NXP i.MX 6Solo, 6DualLite with the TPS6521815 PMIC
i.MX 7Solo and 7Dual	Powering the NXP i.MX 7 Processor with the TPS6521815 PMIC

References

Texas Instruments, *TPS6521825 Power Management IC (PMIC) for NXP i.MX 8M Mini* Data Sheet

Texas Instruments, *LP8733xx Dual High-Current Buck Converter and Dual Linear Regulator* Data Sheet

Texas Instruments, *Integrated Power Supply Reference Design for NXP i.MX 8M Mini Processor* Design Guide

NXP Semiconductors, *i.MX 8M Mini Applications Processor Datasheet for Industrial Products* (IMX8MMIEC), Rev. 0.2, 04/2019

NXP Semiconductors, *i.MX 8M Nano Applications Processor Datasheet for Industrial Products* (IMX8MNIEC), Rev. 0, 10/2019

0.1 Trademarks

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2019) to A Revision	Page
• Updated part number from LP8733D to LP873347	1

Changes from A Revision (October 2019) to B Revision	Page
• Updated part number from TPS65218D0 to TPS6521825	1
• Updated Block Diagram based on completed design	1
• Updated i.MX 8M Mini Power Requirements Table based on completed design	2

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