Application Report
SLVAEB4–August 2019

TPS25831-Q1 and TPS25833-Q1 Thermal Management

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ABSTRACT

In automotive application systems, thermal performance is critical to a successful design. Power densities can be very high, especially in head units, media hubs, and multiple-port applications. This application note discusses how to deal with this thermal issue using the TPS25831-Q1 and TPS25833-Q1 in automotive USB port applications.

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1 Introduction

The TPS25831-Q1 and TPS25833-Q1 is a USB type-C and BC1.2 charge port converter. This device includes a synchronous DC/DC converter with cable droop compensation and NTC input for intelligent thermal management. The TPS25831-Q1 and TPS25833-Q1 can be designed in dual type-C and dual type-A port applications. Space and PCB size are typically very limited in head units and USB media hubs. In a dual type-C port hub application, the total power consumption can be up to 30 W. In some special cases, the hub needs to sustain an 85°C ambient temperature with no drop in available output current. In such cases, a robust thermal design is especially critical.

2 PCB Design in the TPS25831-Q1 and TPS25833-Q1

2.1 PCB Layout Consideration

The following are several key factors you need to consider during PCB layout for high power density applications.

1. Landing pad: The landing pad on the top of the PCB must be the same size, or larger, than the exposed pad of the component. The component must be soldered to the pad with reasonable coverage to ensure good heat conduction from the component to the PCB. See the *PowerPAD™ Thermally Enhanced Package Application Report* for more information on soldering. The outermost portions of the landing pad must be free from the solder mask as these are the most important areas for spreading heat into the PCB.
2. Spreading plane: There must be at least one Cu spreading plane in the PCB. This plane conducts the heat away from the small area of the component to a larger area in the PCB where the heat is then dissipated through convection and radiation into the surrounding environment. As such, the plane must have sufficient thickness and area to provide adequate heat sinking for the component. Electrically, the plane is normally held at ground for exposed pad packages. As illustrated in Figure 1, the spreading plane can be located on the top layer and directly connected to the landing pad. This is often the case for packages such as TSSOP or SON. The spreading planes can also be located on buried layers and connected to the vias. Buried spreading planes are commonly used with packages such as QFN or QFP. Figure 1 lists and illustrates a short summary of the main factors.

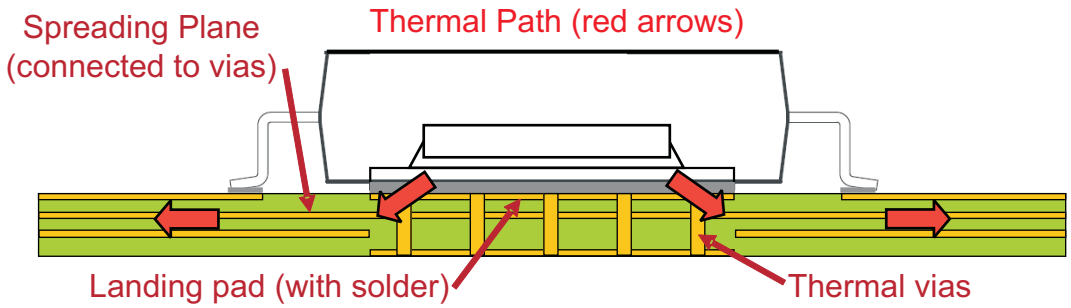

Figure 1. PCB Thermal Path

3. Vias: When a buried spreading plane is employed, the landing pad must be connected by an array of vias to the buried plane to ensure good heat conduction from the exposed pad. Details of via designs can be found in the *PowerPAD™ Thermally Enhanced Package Application Report*. A landing pad with insufficient vias to buried power and ground planes does not conduct sufficient heat from the package into the PCB spreading planes, and can result in high temperatures.

The spreading plane is of particular importance to the thermal performance of exposed pad packages and must be one of the primary considerations in PCB design. For adequate thermal management, it must have a sufficient area. The larger the spreading plane, the cooler the devices run, so it must be as large as possible beyond the minimum area. Perform thermal analysis to ensure the plane meets the minimum area required to keep the junction temperature below the absolute maximum temperature. Figure 2 shows an example of a graph that illustrates the impact of the spreading plane area on junction temperature for an example device and PCB stackups. The area of the spreading plane (assumed to be continuous, having no breaks) is shown on the x-axis, and the resulting temperature is shown on the y-axis. Note that below a certain size, the temperature rises dramatically as there is little copper area available to cool the component. Similarly, for a copper area larger than a certain size, the impact on the temperature diminishes significantly as the heat is sufficiently spread out.

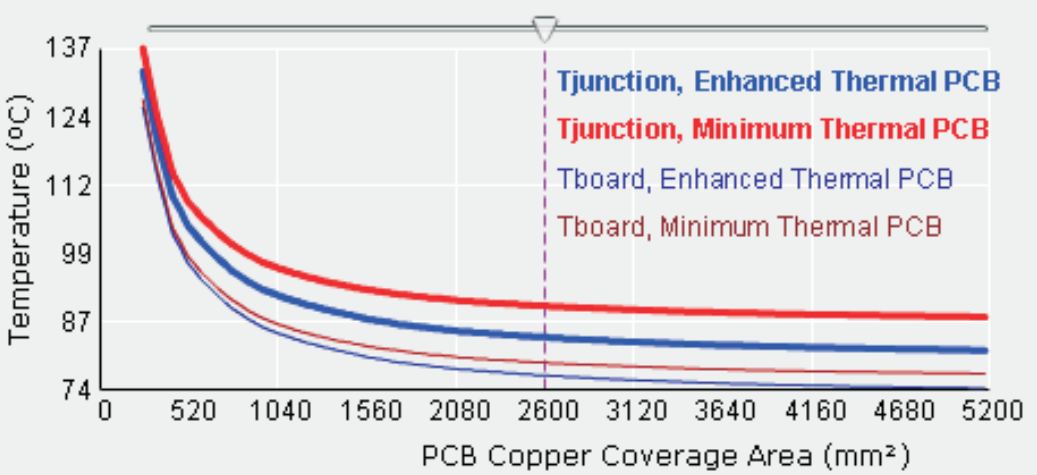

Figure 2. Example Graph Showing Junction Temperature as a Function of Spreading Plane Area for the TPS25831-Q1 Device at 0.5 W with 65°C Ambient Temperature

2.2 TPS25831-Q1 and TPS25833-Q1 PCB Layout Recommendation

The TPS25831-Q1 and TPS25833-Q1 packages are 5-mm × 5-mm VQFN(32), which has a large thermal pad to provide low thermal resistance from junction to the board. Figure 3 and Figure 4 show the PCB layout of the PMP40542 30-mm × 30-mm reference design. This design uses two TPS25833-Q1 devices in a dual type-C USB port application. The PMP40542 uses a 4-layer PCB with 2 oz Cu on the top and bottom layer and 1 oz Cu for the inner layers. The landing pads for U1 and U2 each have 16 vias to provide good thermal conduction from the device to the top layer and two internal signal layers. The top layer and two middle signal layers work as the main spreading plane to provide heat sinking for the two TPS25833-Q1 devices. There are about 50 spreading plane vias in total to ensure good heat conduction from the device cases to the outer layer.

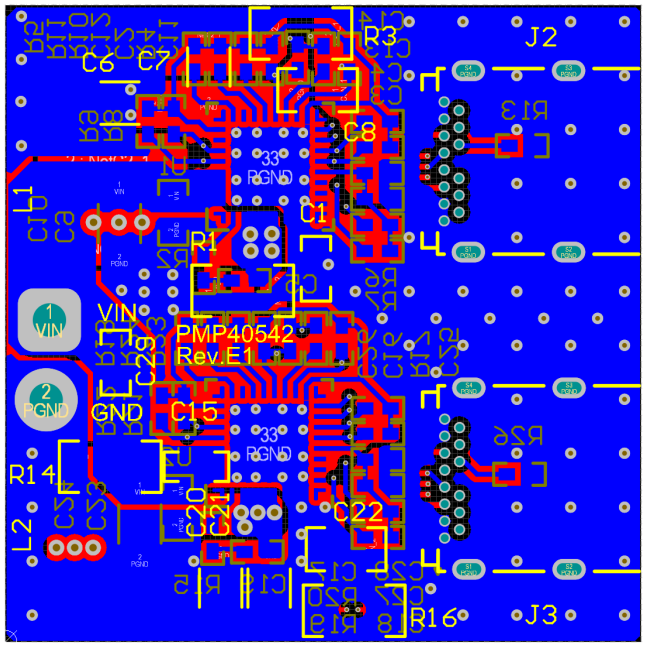

Figure 3. PMP40542 Bottom View

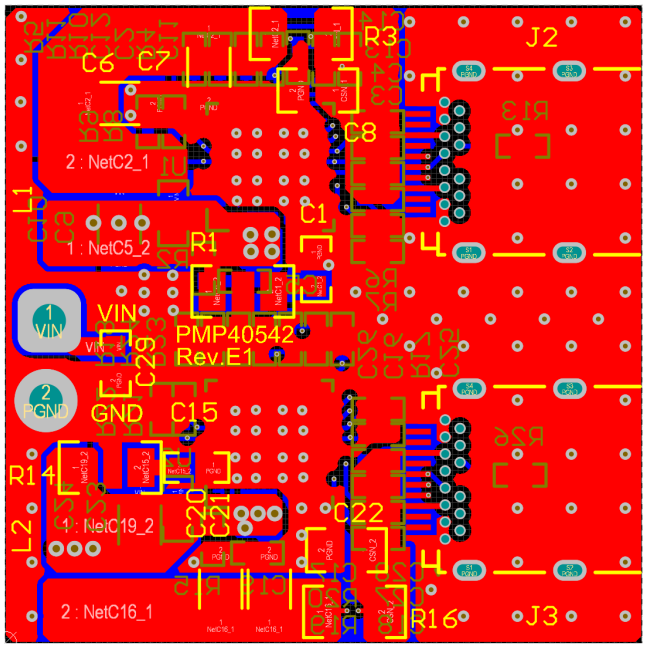

Figure 4. PMP40542 Top View

3 Size of PCB Impact the Thermal

The PMP40542 and PMP40543 are two functionally similar, but physically and thermally different reference designs that clearly show the impact of board design on thermal performance.

Figure 5 shows the PMP40542, dual type-C port solution schematic. Figure 6 shows the PMP40542 PCB (30-mm × 30-mm) and thermal performance. The case temperature rises about 50°C in a 12 V input and 6 A full load current condition.

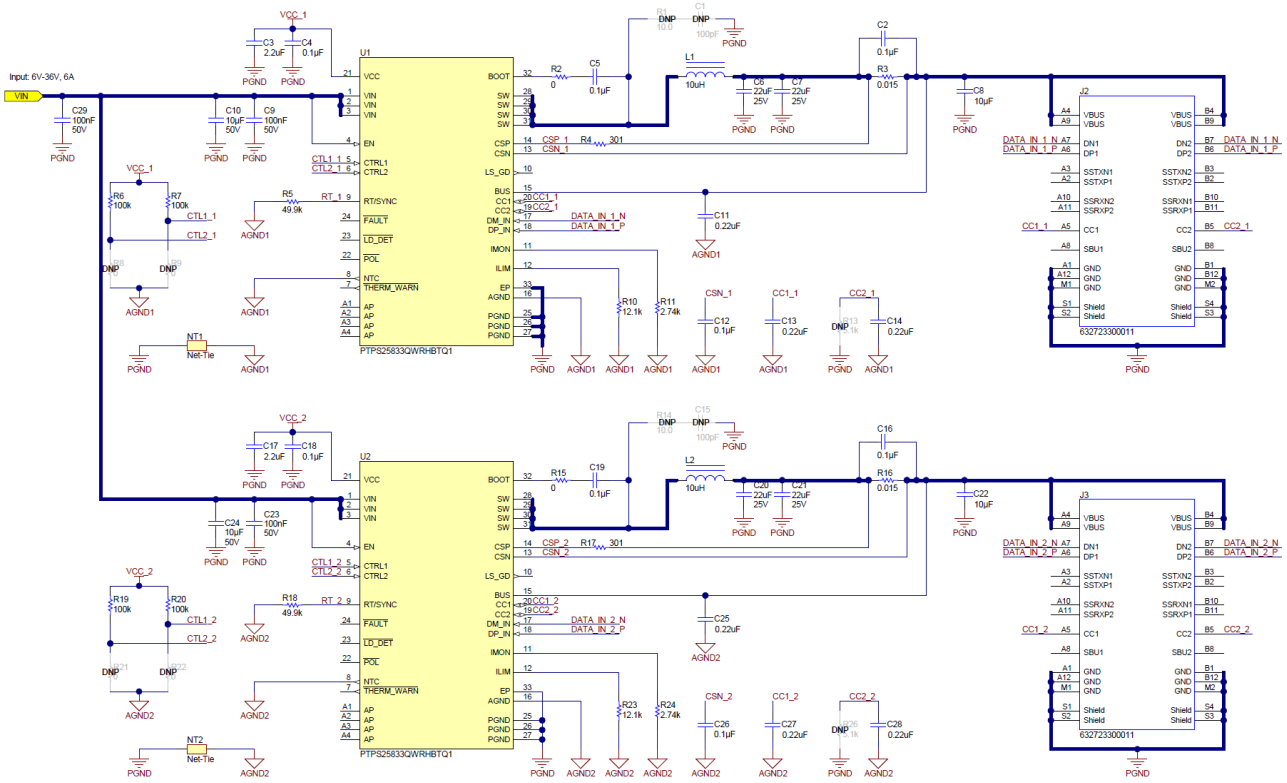

Figure 5. Dual Type-C Port Application

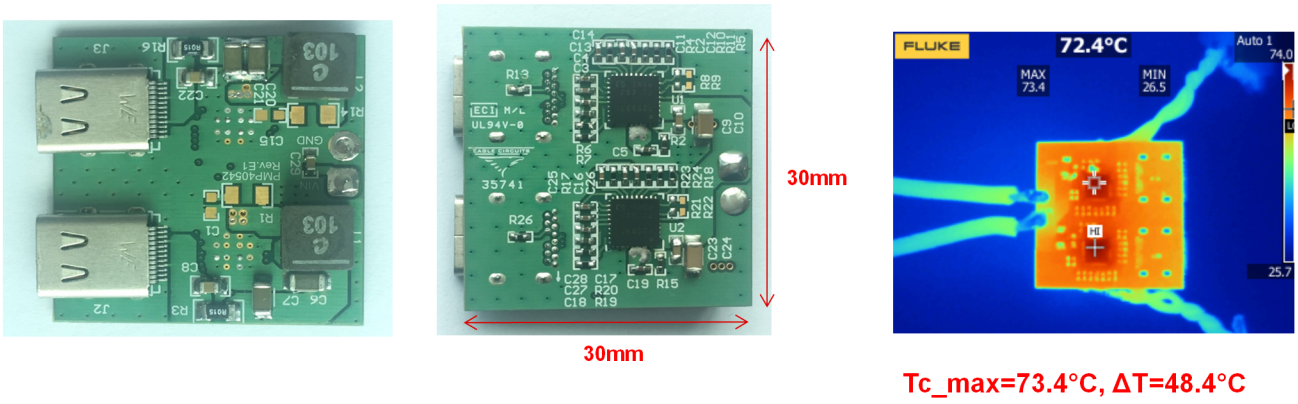

Figure 6. Dual Type-C Port PCB View and Thermal Performance

Figure 7 shows the PMP40543 schematic and Figure 8 shows the PMP40543 PCB (45-mm × 45-mm) and thermal performance. The case temperature rises about 37°C in a 12 V input and 6 A loading current condition.

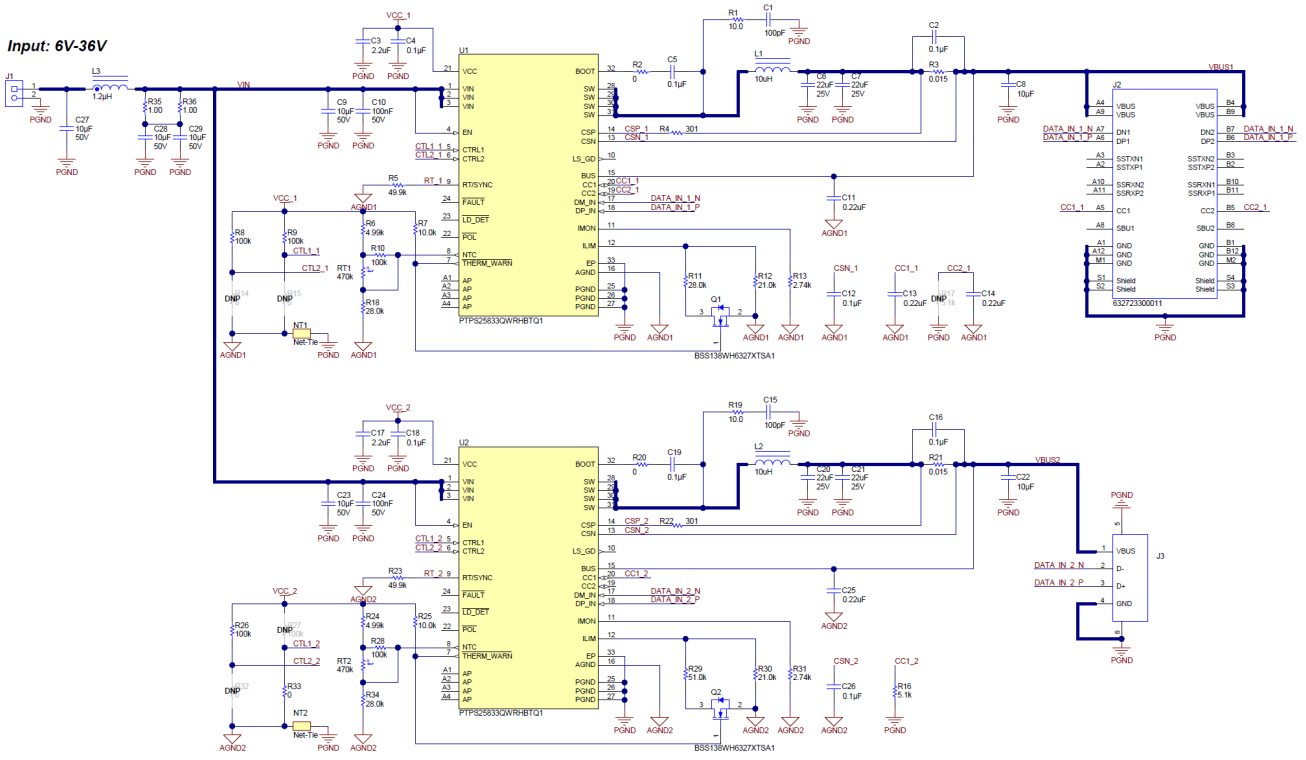

Figure 7. Type A And Type-C Dual Port Application Schematic

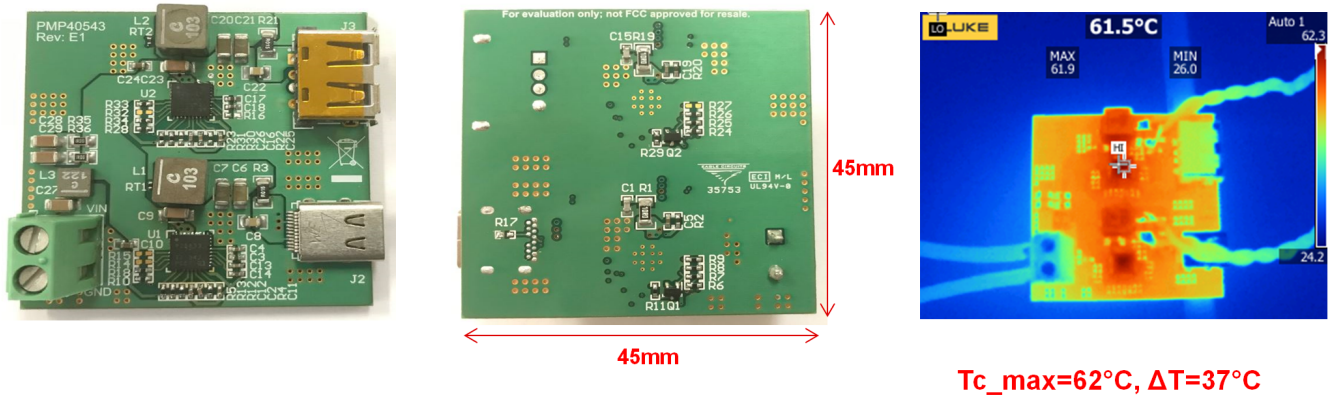

Figure 8. Type-A And Type-C Dual Port PCB And Thermal

Both reference design boards use 2 oz Cu for top and bottom layers and 1 oz Cu for the internal layers. Even though the loading is same, the TPS25833-Q1 case temperature in the PMP40543 (45-mm × 45-mm) is about 11 degrees lower than the PMP40542 (30-mm × 30-mm). Both EVMs work well in full loading current condition without any reduction in output current at 85°C ambiance temperature. The TPS25833 shows good thermal performance in these two dual-port reference designs.

Table 1 shows the TPS25833-Q1 case temperature in 28°C and 85°C ambiance temperatures.

Table 1. TPS25833-Q1 Case Temperatures

	Ta = 28°C	Ta = 85°C
Loading	6 A	6 A
PMP40542 (30-mm × 30-mm), T_case	72.6°C	126°C
PMP40543 (45-mm × 45-mm), T_case	63.5°C	117.5°C

4 Thermal Management with NTC (TPS2581-Q1 and TPS25833-Q1)

4.1 Thermal Sensing with NTC (TPS2581-Q1 and TPS25833-Q1)

The NTC input pin allows for user-programmable load shedding during high temperature operation. Without load shedding the device provides full output current during high temperature operation and eventually shuts off all current when the internal OSD level is reached. Smart thermal management allows the design to program a thermal threshold which, when crossed, uses the CC pins to reduce the advertised available current from 3A to 1.5 A. This reduces device internal power dissipation up to 50%, which helps avoid thermal shutdown and the poor consumer experience that goes with a charge port that does not charge. The NTC input pin threshold is ratiometric with V_{CC}. The external resistor divider setting V_{NTC}, must be connected to the TPS25831-Q1 V_{CC} pin to achieve accurate results (see Figure 9 and Figure 10). When $V_{NTC} = 0.5 \times V_{CC}$ (approximately 2.5 V typically), the TPS25831-Q1 performs two actions:

1. If operating with 3-A type-C advertisement, the CC1 and CC2 pin automatically reduces advertisement to the 1.5-A level.
2. The $\overline{\text{THERM\_WARN}}$ flag is asserted to provide an indication of the overtemperature condition. $\overline{\text{FAULT}}$ is NOT asserted at this time.

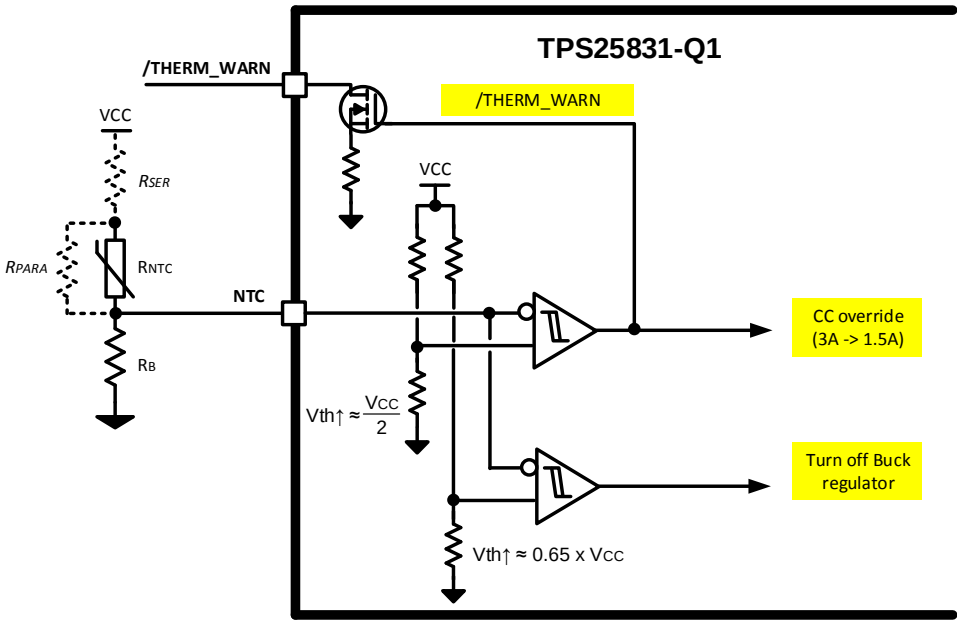

Figure 9. NTC Input Pin

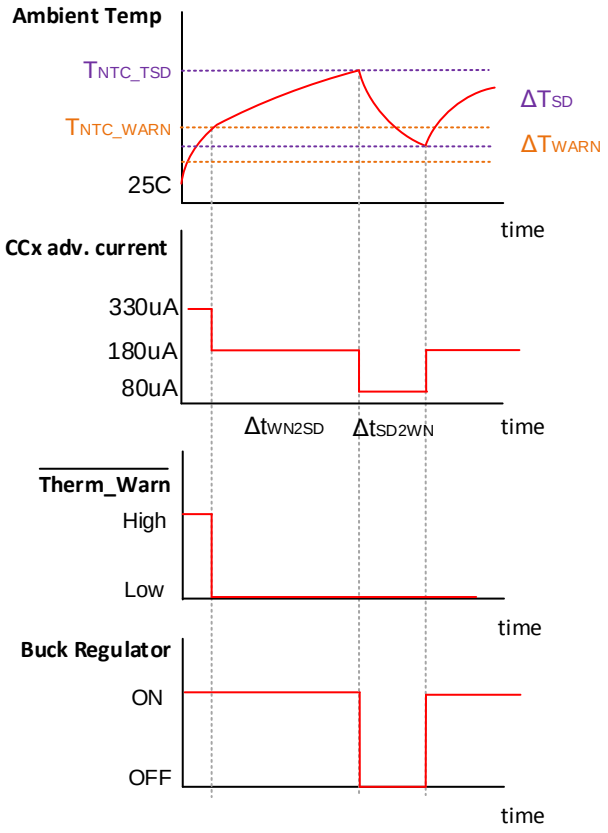

Figure 10. TPS25831-Q1 Behavior When Trigger NTC Threshold

If the overtemperature condition persists, causing $V_{NTC} = V_{CC} \times 0.65$ (3.25-V typical), the TPS25831-Q1 turns off the buck regulator and pulls the LS_GD pin low. The $\overline{\text{THERM\_WARN}}$ flag remains asserted; however, the $\overline{\text{FAULT}}$ pin is NOT asserted for this condition.

Tuning the V_{NTC} threshold levels of V_{WARN_HIGH} and V_{SD_HIGH} is achieved by adding R_{SER} or R_{PARA}, or both R_{SER} and R_{PARA} in conjunction with R_{NTC}.

4.2 Active Current Limit By TPS2581-Q1 and TPS25833-Q1

The TPS2581-Q1 and TPS25833-Q1 only changes the CC line broadcast when the NTC pin voltage touches the V_{WARN_HIGH} and V_{SD_HIGH} thermal protection threshold. These devices cannot automatically change the current limit threshold in the output USB port during thermal warning and thermal shutdown. The USB port charging current depends on the charging behavior of te attached device. In some cases, it needs to limit the port output current to avoid system thermal issues. You can use an external FET and the $\overline{\text{THERM\_WARN}}$ pin for the active current limit by the TPS2581-Q1 and TPS25833-Q1.

Figure 11 shows how to use the $\overline{\text{THERM\_WARN}}$ pin and a FET to change the current limit threshold in response to device thermal warning. In the type-C port design, the R_{11}, R_{11}, and Q_{12} can be configured to change the original current limit threshold from 3.3 A to 1.9 A when the V_{NTC} touches the V_{WARN_HIGH} threshold. In the type-A port design, the R_{29}, R_{30}, and Q_2 can be configured to change the original current limit threshold from 2.7 A to 1.9 A after thermal warning.

The following are NTC spec and resistor values used in the PMP40543.

- $R_{T1,T2}$ = 470 kΩ, β = 4700, $R_{NTC} = R_0 \times \exp \beta \times (1/T\text{-}1/T_0)$
- R_{10} and R_{28} = 100 kΩ
- R_6 and R_{24} = 4.98 kΩ
- R_{18} and R_{34} = 28 kΩ

The EVM thermal design target warns at 87°C and shuts down at 116°C.

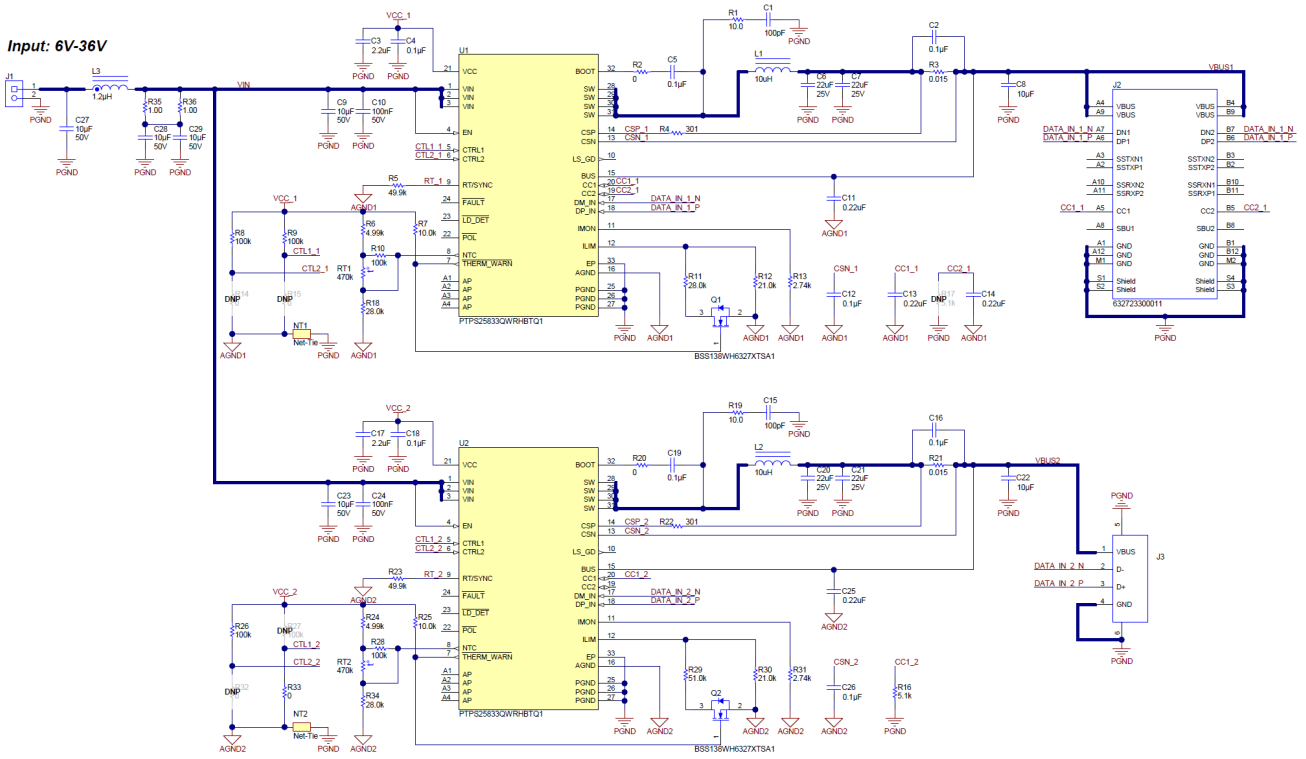

Figure 11. Active Current Limit With NTC Thermal Management

Figure 12 and Figure 13 show the PMP40543 test results. The test used an Apple iPAD® for the type-A port and Google type-C Pixel 2™ phone for the type-C port.

Figure 12 shows the active current limit in a J3 type-A receptacle port. The Apple iPAD original charging current is 2.4 A. When the V_{NTC} in U2 reaches 2.5 V, the $\overline{\text{THERM\_WARN}}$ pin asserts to turn off Q2 and cuts R29 from the circuit. The total resistance in U2 ILIM pin is now equal to R30. The current limit threshold in the J3 type-A port is changed from 2.7 A to 1.9 A accordingly. The iPAD charging current is limited to 1.9 A automatically.

Figure 13 shows the active current limit in the J2 type-C receptacle port. The charging current of the Google Pixel 2 is 2.3 A. When the V_{NTC} in U1 reaches 2.5 V, the $\overline{\text{THERM\_WARN}}$ pin asserts to turn off Q1 and cuts R11 out of the circuit. The total resistance from U1 ILIM pin to GND is now equal to R12 and the current limit threshold in the J2 type-C port drops from 3.3 A to 1.9 A, accordingly. At the same time, the CC line in the J2 type-C receptacle port broadcast current changes from 3 A to 1.5 A. The Google Pixel 2 detects the change in available current broadcast on the CC line and drops the charging current to 1.5 A, accordingly.

After the active current limit in J2 and J3 port, the device and system power dissipation is reduced and thermal issues have been mitigated. Test results show that the PMP40543 U1 and U2 case temperatures can dropped down to 93°C after the active current limit for thermal management. Compared to the 118°C temperature during full load, the system can cool down as much as 20°C.

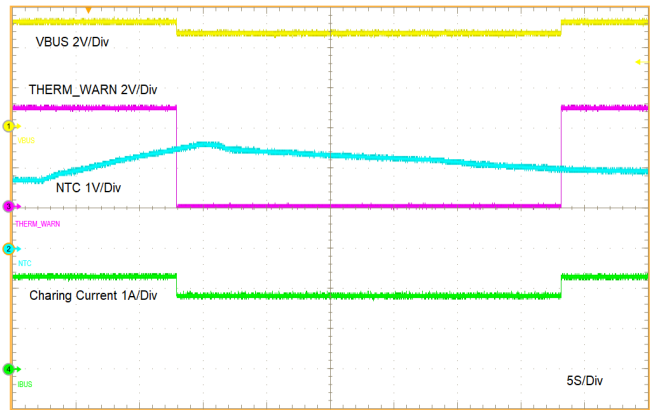

Figure 12. Active Current Limit In Type-A Port

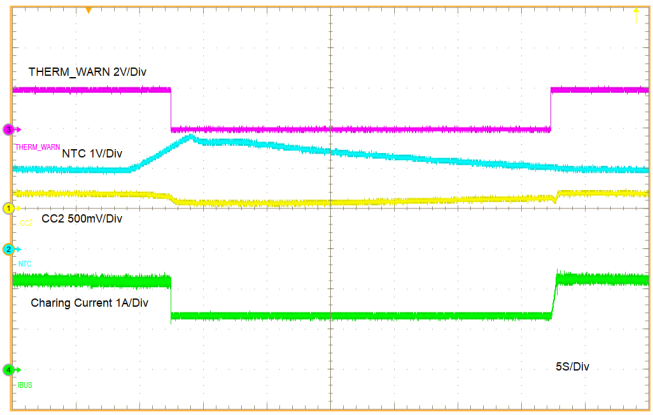

Figure 13. Active Current Limit In Type-C Port

5 References

- Texas Instruments, *PowerPAD™ Thermally Enhanced Package Application Report* (SLMA002)
- Texas Instruments, *TPS2583x-Q1 USB Type-C and BC1.2 5-V 3.5-A Output, 36-V Input Synchronous Step-Down DC/DC Regulator with Cable Compensation Data Sheet* (SLVSDP6)

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