Functional Safety Information

DRV8873-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for DRV8873H-Q1 (HTSSOP(24) package, HW variant) and DRV8873S-Q1 (HTSSOP(24) package, SPI variant) to aid in a functional safety system design. Information provided are:

-
- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

DRV8873-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

Figure 1-1 shows the functional block diagram for the HW variant of this device as a reference.

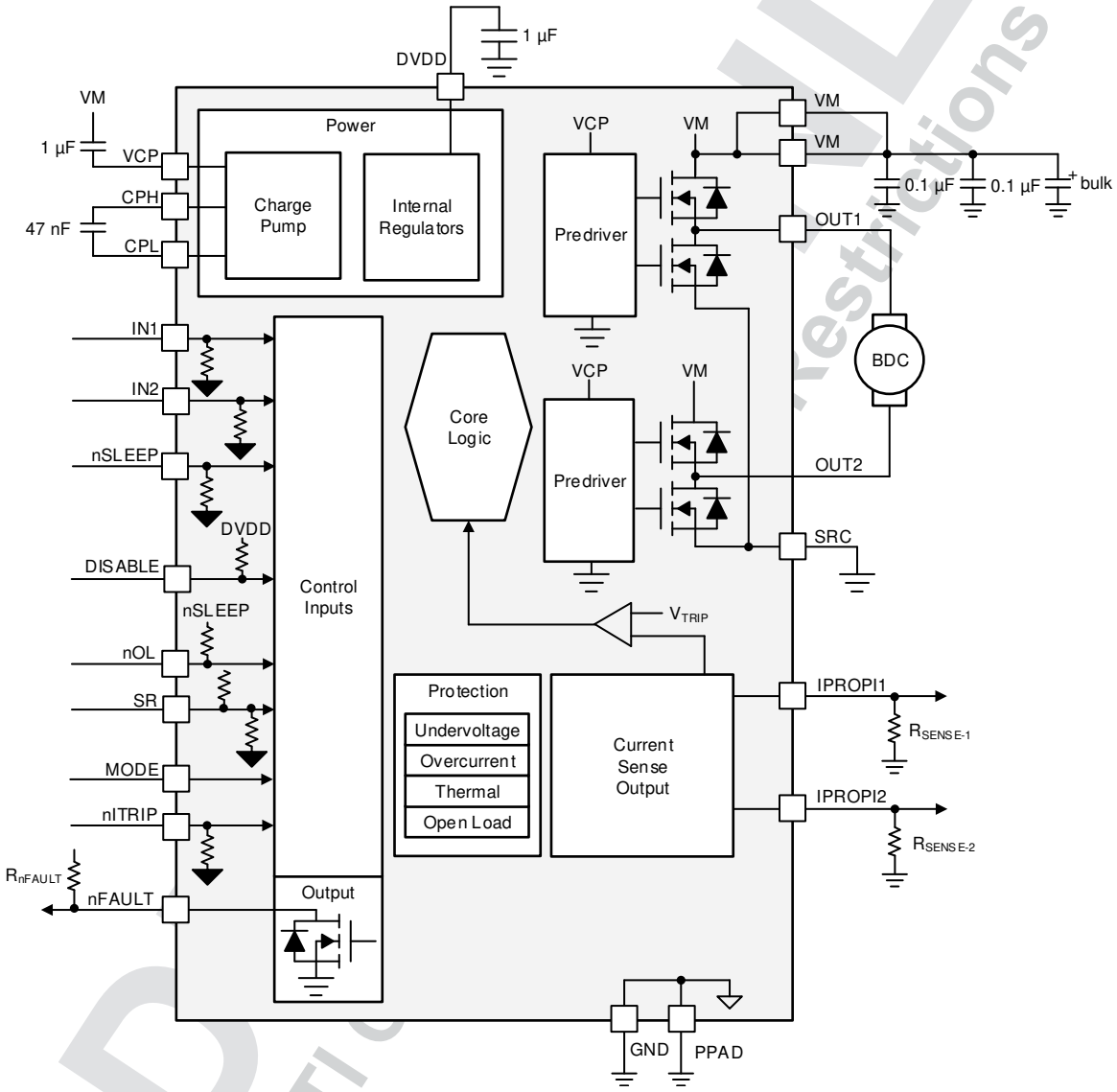

Figure 1-1. DRV8873H-Q1 Device Block Diagram - HW variant

Figure 1-2 shows the functional block diagram for the HW variant of this device as a reference.

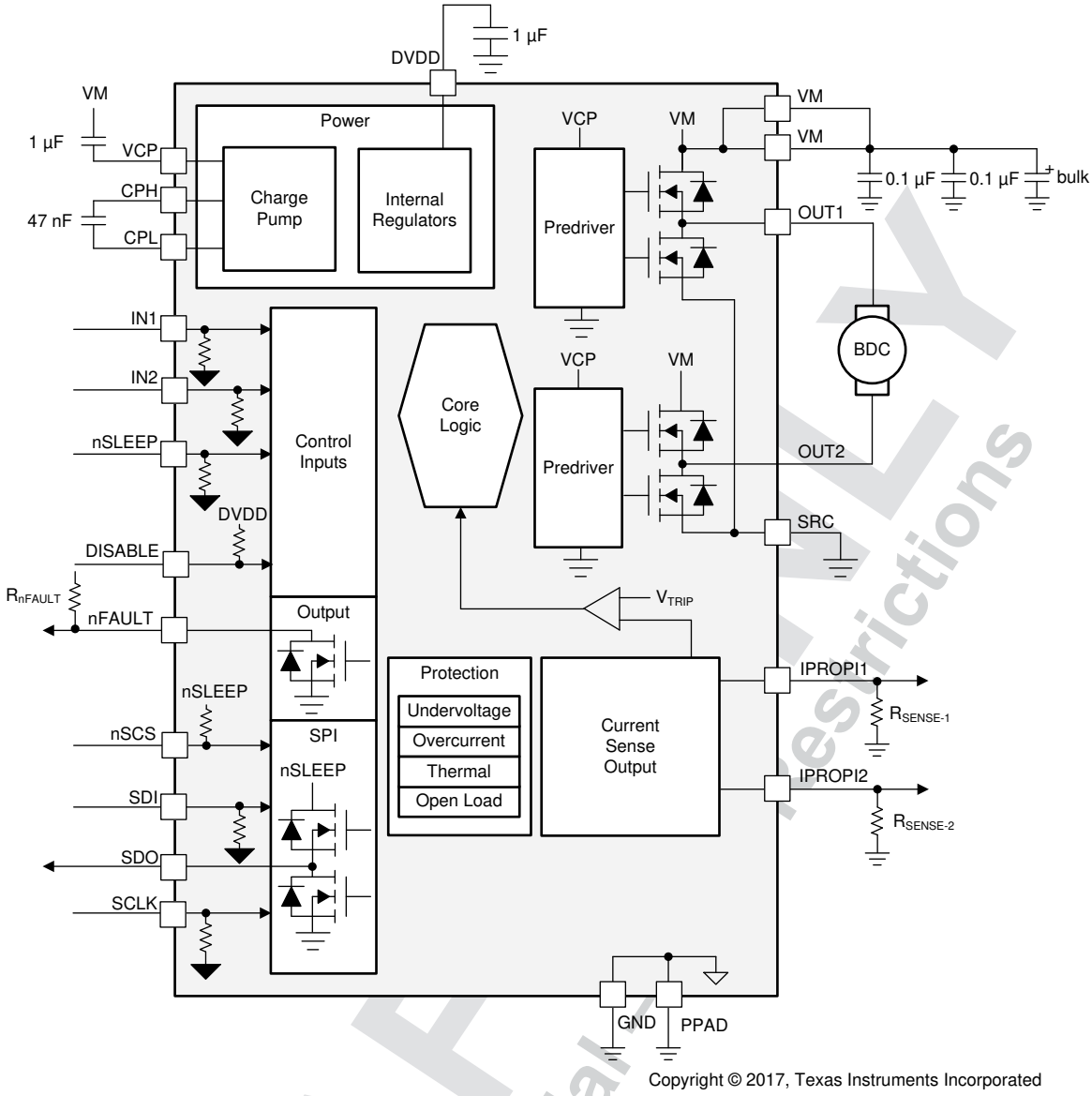

Figure 1-2. DRV8873S-Q1 Device Block Diagram - SPI variant

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV8873-Q1 (common for both variants) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	**24**
Die FIT Rate	**8**
Package FIT Rate	**16**

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: **1.15 W**
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	**CMOS, BICMOS Digital, analog / mixed**	**25 FIT**	**55°C**

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV8873-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTx is stuck LOW when commanded OFF	14%
OUTx is stuck OFF when commanded LOW	8%
OUTx ON resistance too high when commanded LOW	12%
Low side slew rate too fast or too slow	5%
OUTx is stuck HIGH when commanded OFF	14%
OUTx is stuck OFF when commanded HIGH	8%
OUTx ON resistance too high when commanded HIGH	17%
High side slew rate too fast or too slow	5%
Dead-time is too short	1%
Current sense feedback incorrect	3%
ITRIP current regulation incorrect	3%
Incorrect communication or fault indication	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the DRV8873-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 for HW variant, see Table 4-6 for SPI variant)
- Pin open-circuited (see Table 4-3 for HW variant, see Table 4-7 for SPI variant)
- Pin short-circuited to an adjacent pin (see Table 4-4 for HW variant, see Table 4-8 for SPI variant)
- Pin short-circuited to supply (see Table 4-5 for HW variant, see Table 4-9 for SPI variant)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 DRV8873H-Q1 (HW variant)

Figure 4-1 shows the DRV8873H-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the DRV8873-Q1 datasheet.

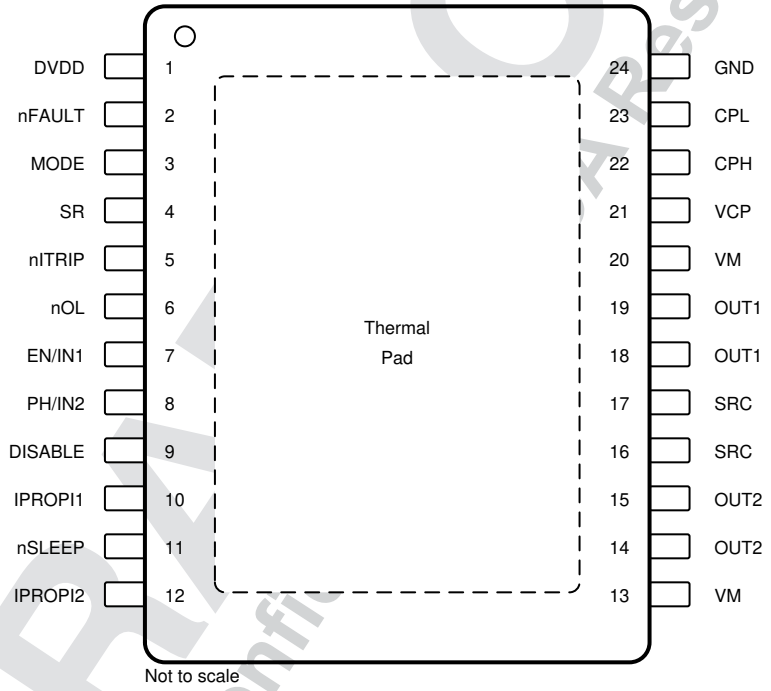

Figure 4-1. DRV8873H-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table of the datasheet.

Table 4-2. HW variant - Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DVDD	1	Device will not power on (OUTx remain HiZ) with higher current draw from VM	A
nFAULT	2	Device will always be signaling fault	B

Table 4-2. HW variant - Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE	3	Device Mode configuration may be misinterpreted	B
SR	4	Device SR configuration may be misinterpreted	B
nITRIP	5	Device nITRIP configuration may be misinterpreted	B
nOL	6	Device nOL configuration may be misinterpreted	B
EN/IN1	7	OUTx driver control will be lost	B
PH/IN2	8	OUTx driver control will be lost	B
DISABLE	9	OUTx driver control will be lost	B
IPROPI1	10	Current sensing capability will be lost	B
nSLEEP	11	Device will be in sleep state with OUTx HiZ	B
IPROPI2	12	Current sensing capability will be lost	B
VM	13	Device will not power up	B
OUT2	14	OUTx HiZ, with device signaling fault	B
OUT2	15	OUTx HiZ, with device signaling fault	B
SRC	16	Intended operation	D
SRC	17	Intended operation	D
OUT1	18	OUTx HiZ, with device signaling fault	B
OUT1	19	OUTx HiZ, with device signaling fault	B
VM	20	Device will not power up	B
VCP	21	Device will be damaged with higher current draw from VM	A
CPH	22	Device will be damaged with higher current draw from VM	A
CPL	23	Device will be damaged with higher current draw from VM	A
GND	24	Intended operation	D

Table 4-3. HW variant - Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DVDD	1	Internal regulator will become unstable	A
nFAULT	2	Fault signaling will be lost	B
MODE	3	Device Mode configuration may be misinterpreted	B
SR	4	Device SR configuration may be misinterpreted	B
nITRIP	5	Device nITRIP configuration may be misinterpreted	B
nOL	6	Device nOL configuration may be misinterpreted	B
EN/IN1	7	OUTx driver control will be lost	B
PH/IN2	8	OUTx driver control will be lost	B
DISABLE	9	OUTx driver control will be lost	B
IPROPI1	10	Current sensing capability will be lost	B
nSLEEP	11	Device will be in sleep state with OUTx HiZ	B
IPROPI2	12	Current sensing capability will be lost	B
VM	13	Device will not power up	B
OUT2	14	OUTx impedance will be higher - device will not be able to drive the load properly	B
OUT2	15	OUTx impedance will be higher - device will not be able to drive the load properly	B
SRC	16	OUTx impedance will be higher - device will not be able to drive the load properly	B
SRC	17	OUTx impedance will be higher - device will not be able to drive the load properly	B

Table 4-3. HW variant - Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	18	OUTx impedance will be higher - device will not be able to drive the load properly	B
OUT1	19	OUTx impedance will be higher - device will not be able to drive the load properly	B
VM	20	Device will not power up	B
VCP	21	OUTx HiZ, with device signaling fault	B
CPH	22	OUTx HiZ, with device signaling fault	B
CPL	23	OUTx HiZ, with device signaling fault	B
GND	24	Device will not power up	B

Table 4-4. HW variant - Pin FMA for Device Pins Shorted to Adjacent Pin

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DVDD	1	2	Device will reset whenever nFAULT is asserted low	B
nFAULT	2	3	Device Mode configuration may be misinterpreted	B
MODE	3	4	Device Mode and/or SR configuration may be misinterpreted	B
SR	4	5	Device SR and/or nITRIP configuration may be misinterpreted	B
nITRIP	5	6	Device nITRIP and/or nOL configuration may be misinterpreted	B
nOL	6	7	Device nOL configuration may be misinterpreted	B
EN/IN1	7	8	OUTx driver control will be lost	B
PH/IN2	8	9	OUTx driver control will be lost	B
DISABLE	9	10	OUTx driver control and load current sensing will be lost	B
IPROPI1	10	11	Current sensing capability will be lost	B
nSLEEP	11	12	Current sensing capability will be lost	B
IPROPI2	12	13	Device will be damaged with higher current draw from VM	A
VM	13	14	OUTx HiZ with device signaling fault	B
OUT2	14	15	Intended operation	D
OUT2	15	16	OUTx HiZ, with device signaling fault	B
SRC	16	17	Intended operation	D
SRC	17	18	OUTx HiZ, with device signaling fault	B
OUT1	18	19	Intended operation	D
OUT1	19	20	OUTx HiZ with device signaling fault	B
VM	20	21	OUTx HiZ with device signaling fault	B
VCP	21	22	Device will be damaged with higher current draw from VM	A
CPH	22	23	Device will be damaged with higher current draw from VM	A
CPL	23	24	Device will be damaged with higher current draw from VM	A

Table 4-5. HW variant - Pin FMA for Device Pins Shorted to VM (High Voltage Supply)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DVDD	1	Device will be damaged with higher current draw from VM	A
nFAULT	2	Device will be damaged with higher current draw from VM	A
MODE	3	Device will be damaged with higher current draw from VM	A
SR	4	Device will be damaged with higher current draw from VM	A
nITRIP	5	Device will be damaged with higher current draw from VM	A
nOL	6	Device will be damaged with higher current draw from VM	A
EN/IN1	7	Device will be damaged with higher current draw from VM	A

Table 4-5. HW variant - Pin FMA for Device Pins Shorted to VM (High Voltage Supply) (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PH/IN2	8	Device will be damaged with higher current draw from VM	A
DISABLE	9	Device will be damaged with higher current draw from VM	A
IPROPI1	10	Device will be damaged with higher current draw from VM	A
nSLEEP	11	Device will be damaged with higher current draw from VM	A
IPROPI2	12	Device will be damaged with higher current draw from VM	A
VM	13	Intended operation	D
OUT2	14	OUTx HiZ with device signaling fault	B
OUT2	15	OUTx HiZ with device signaling fault	B
SRC	16	Device will not power up	B
SRC	17	Device will not power up	B
OUT1	18	OUTx HiZ with device signaling fault	B
OUT1	19	OUTx HiZ with device signaling fault	B
VM	20	Intended operation	D
VCP	21	OUTx HiZ with device signaling fault	B
CPH	22	Device will be damaged with higher current draw from VM	A
CPL	23	Device will be damaged with higher current draw from VM	A
GND	24	Device will not power up	B

4.2 DRV8873S-Q1 (SPI variant)

Figure 4-2 shows the DRV8873S-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the DRV8873-Q1 datasheet.

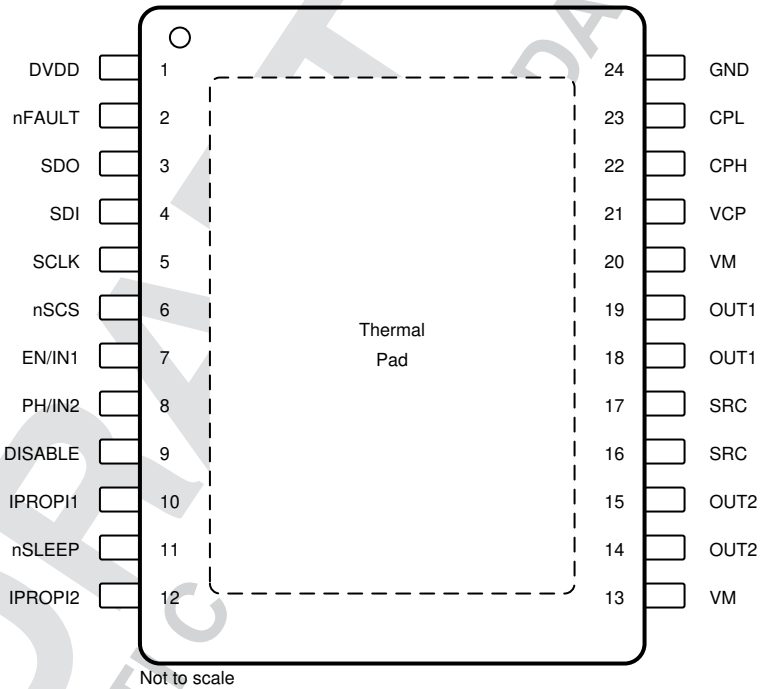

Figure 4-2. DRV8873S-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table of the datasheet.

Table 4-6. SPI variant - Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DVDD	1	Device will not power on (OUTx remain HiZ) with higher current draw from VM	A
nFAULT	2	Device will always be signaling fault	B
SDO	3	SPI read function will be non-functional	B
SDI	4	SPI read write functions will be non-functional	B
SCLK	5	SPI read write functions will be non-functional	B
nSCS	6	SPI read write functions will be non-functional	B
EN/IN1	7	OUTx driver control will be lost	B
PH/IN2	8	OUTx driver control will be lost	B
DISABLE	9	OUTx driver control will be lost	B
IPROPI1	10	Current sensing capability will be lost	B
nSLEEP	11	Device will be in sleep state with OUTx HiZ	B
IPROPI2	12	Current sensing capability will be lost	B
VM	13	Device will not power up	B
OUT2	14	OUTx HiZ, with device signaling fault	B
OUT2	15	OUTx HiZ, with device signaling fault	B
SRC	16	Intended operation	D
SRC	17	Intended operation	D
OUT1	18	OUTx HiZ, with device signaling fault	B
OUT1	19	OUTx HiZ, with device signaling fault	B
VM	20	Device will not power up	B
VCP	21	Device will be damaged with higher current draw from VM	A
CPH	22	Device will be damaged with higher current draw from VM	A
CPL	23	Device will be damaged with higher current draw from VM	A
GND	24	Intended operation	D

Table 4-7. SPI variant - Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DVDD	1	Internal regulator will become unstable	A
nFAULT	2	Fault signaling will be lost	B
SDO	3	SPI read function will be non-functional	B
SDI	4	SPI read write functions will be non-functional	B
SCLK	5	SPI read write functions will be non-functional	B
nSCS	6	SPI read write functions will be non-functional	B
EN/IN1	7	OUTx driver control will be lost	B
PH/IN2	8	OUTx driver control will be lost	B
DISABLE	9	OUTx driver control will be lost	B
IPROPI1	10	Current sensing capability will be lost	B
nSLEEP	11	Device will be in sleep state with OUTx HiZ	B
IPROPI2	12	Current sensing capability will be lost	B
VM	13	Device will not power up	B
OUT2	14	OUTx impedance will be higher - device will not be able to drive the load properly	B
OUT2	15	OUTx impedance will be higher - device will not be able to drive the load properly	B
SRC	16	OUTx impedance will be higher - device will not be able to drive the load properly	B

Table 4-7. SPI variant - Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SRC	17	OUTx impedance will be higher - device will not be able to drive the load properly	B
OUT1	18	OUTx impedance will be higher - device will not be able to drive the load properly	B
OUT1	19	OUTx impedance will be higher - device will not be able to drive the load properly	B
VM	20	Device will not power up	B
VCP	21	OUTx HiZ, with device signaling fault	B
CPH	22	OUTx HiZ, with device signaling fault	B
CPL	23	OUTx HiZ, with device signaling fault	B
GND	24	Device will not power up	B

Table 4-8. SPI variant - Pin FMA for Device Pins Shorted to Adjacent Pin

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DVDD	1	2	Device will reset whenever nFAULT is asserted low	B
nFAULT	2	3	SPI read write functions and fault signaling will not work	B
SDO	3	4	SPI read write functions will be non-functional	B
SDI	4	5	SPI read write functions will be non-functional	B
SCLK	5	6	SPI read write functions will be non-functional	B
nSCS	6	7	SPI read write functions will be non-functional	B
EN/IN1	7	8	OUTx driver control will be lost	B
PH/IN2	8	9	OUTx driver control will be lost	B
DISABLE	9	10	OUTx driver control and load current sensing will be lost	B
IPROPI1	10	11	Current sensing capability will be lost	B
nSLEEP	11	12	Current sensing capability will be lost	B
IPROPI2	12	13	Device will be damaged with higher current draw from VM	A
VM	13	14	OUTx HiZ with device signaling fault	B
OUT2	14	15	Intended operation	D
OUT2	15	16	OUTx HiZ, with device signaling fault	B
SRC	16	17	Intended operation	D
SRC	17	18	OUTx HiZ, with device signaling fault	B
OUT1	18	19	Intended operation	D
OUT1	19	20	OUTx HiZ with device signaling fault	B
VM	20	21	OUTx HiZ with device signaling fault	B
VCP	21	22	Device will be damaged with higher current draw from VM	A
CPH	22	23	Device will be damaged with higher current draw from VM	A
CPL	23	24	Device will be damaged with higher current draw from VM	A

Table 4-9. SPI variant - Pin FMA for Device Pins Shorted to VM (High Voltage Supply)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DVDD	1	Device will be damaged with higher current draw from VM	A
nFAULT	2	Device will be damaged with higher current draw from VM	A
SDO	3	Device will be damaged with higher current draw from VM	A
SDI	4	Device will be damaged with higher current draw from VM	A
SCLK	5	Device will be damaged with higher current draw from VM	A
nSCS	6	Device will be damaged with higher current draw from VM	A
EN/IN1	7	Device will be damaged with higher current draw from VM	A

Table 4-9. SPI variant - Pin FMA for Device Pins Shorted to VM (High Voltage Supply) (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PH/IN2	8	Device will be damaged with higher current draw from VM	A
DISABLE	9	Device will be damaged with higher current draw from VM	A
IPROPI1	10	Device will be damaged with higher current draw from VM	A
nSLEEP	11	Device will be damaged with higher current draw from VM	A
IPROPI2	12	Device will be damaged with higher current draw from VM	A
VM	13	Intended operation	D
OUT2	14	OUTx HiZ with device signaling fault	B
OUT2	15	OUTx HiZ with device signaling fault	B
SRC	16	Device will not power up	B
SRC	17	Device will not power up	B
OUT1	18	OUTx HiZ with device signaling fault	B
OUT1	19	OUTx HiZ with device signaling fault	B
VM	20	Intended operation	D
VCP	21	OUTx HiZ with device signaling fault	B
CPH	22	Device will be damaged with higher current draw from VM	A
CPL	23	Device will be damaged with higher current draw from VM	A
GND	24	Device will not power up	B

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