Application Brief

Driving Parallel MOSFETs Using the DRV3255-Q1

Today's automotive designs are paving the way for future 48-V electrification as the world strives for more efficient electric vehicles and reducing green house gases. 48-V drive-train components such as the Belt Starter Generator (BSG) and Motor Generators can demand very high-power delivery, some needing as high as 30 kW or higher. The DRV3255-Q1 is well suited for these applications as it is designed specifically with these needs in mind. One of the biggest challenges in these high-power half-bridge designs is optimization to avoid unnecessary PCB heating due to thermal loses in the external MOSFETs. One such optimization is to decrease the MOSFET drain-to-source resistance while in the ON state (known commonly as $R_{DS(on)}$). This document discusses some best practices for schematic and layout optimization with regards to high-power bridge designs with DRV3255-Q1. The same concept can be extended to other drivers with high source and sink current capabilities.

Theory

Increasing the current-conducting capability of a half-bridge circuit benefits from lower $R_{DS(on)}$ and therefore reduced power loss to heat. Designers often use multiple FETs in parallel since FETs placed in parallel will result in an effective reduction in $R_{DS(on)}$ that can still be driven by one gate output. From a theoretical standpoint these multiple FETs can be treated as a single component, as Figure 1 shows.

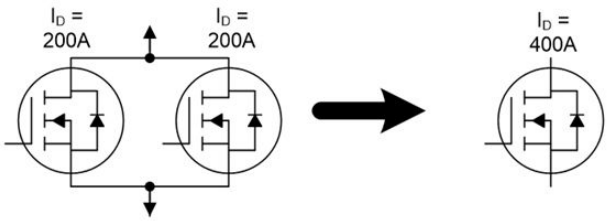

Figure 1. Parallel MOSFET Modeled as a Single FET

In reality, no two MOSFETs will ever be *exactly* identical. This means that ultimately, one MOSFET may turn on faster than the other and carry more current due to $R_{DS(on)}$ differences. Minimizing this difference is critical to system operation. When multiple MOSFETs are on and conducting normally, the MOSFET carrying the most current will experience the most heating, which will raise the $R_{DS(on)}$ compared to the other MOSFETs. This forms a negative feedback loop that should eventually balance the power dissipation between the MOSFETs. However, when the MOSFETs are conducting in reverse through the body diode (due to the motor being turned externally in generator mode, or an asynchronous PWM pattern), the opposite is true. The forward voltage of the body diode *decreases* with temperature, which can cause that MOSFET to then take more of the current flow. This positive feedback loop can cause thermal runaway and damage to the PCB or MOSFETs. For this reason it is important to keep the characteristics of the body diode and the expected reverse current flow in mind when choosing the MOSFET.

Schematic Considerations

When the first MOSFET turns on, it causes a rapid voltage swing at the source node as it starts to conduct. This voltage can couple through the parasitic gate-drain capacitance of the other MOSFET, and cause a voltage spike on the shared gate connection. This can cause oscillation on the gate node as the MOSFETs rapidly turn on and off, and ultimately damage the gate driver or MOSFETs. To dampen this coupling, each MOSFET should have an individual resistor placed between the gate and the shared connection to the gate driver. This will prevent the voltage pulse from coupling back into the input. Figure 2 shows the potential unwanted coupling path. Figure 3 shows the improved individual resistor schematic.

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Note that because the limiting resistor is now being placed in parallel for each MOSFET, the individual resistance must be increased to maintain the same equivalent resistance. For example, if an individual 10-Ω resistor was used on a single gate, each gate in a dual MOSFET configuration would need a 20-Ω resistor so that the equivalent resistance is still 20 || 20 = 10.

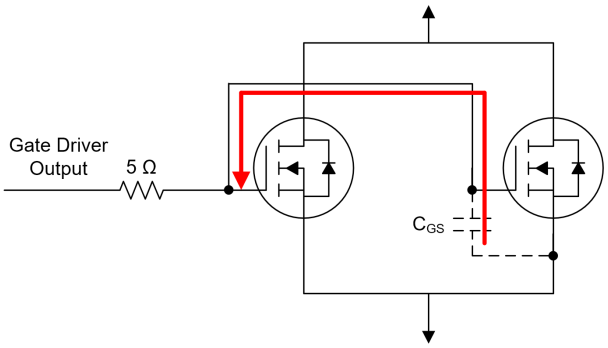

Figure 2. Single-Gate Resistor

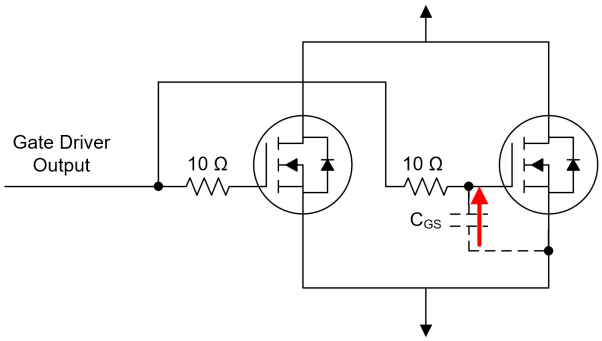

Figure 3. Individual per Gate Resistors

Layout Gate Considerations

The following guidelines are helpful for the best performance of the MOSFET gates:

- To switch the MOSFETs as simultaneously as possible and minimize power losses, try to **place MOSFETs in close proximity to each other.**
- Keep the gate traces unified until close to the MOSFETs. This will minimize the chance of external signal coupling affecting the MOSFETs differently
- **Keep the length of the individual gate traces reasonably close**, although precision length matching usually is not necessary.
- Placement of the individual gate resistors is not critical, but it is recommended to place them close to the MOSFETs, when possible, to limit the chance for signals to couple into or out of the MOSFET gates.

Figure 4 shows a bad gate layout example and Figure 5 shows a recommended gate layout example:

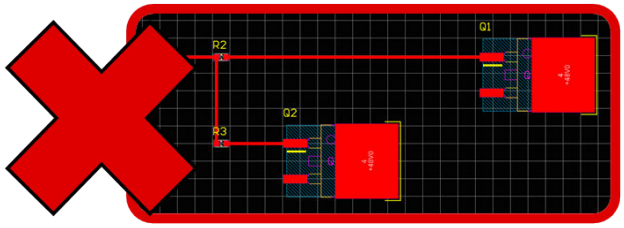

Figure 4. Example of bad Gate Layout

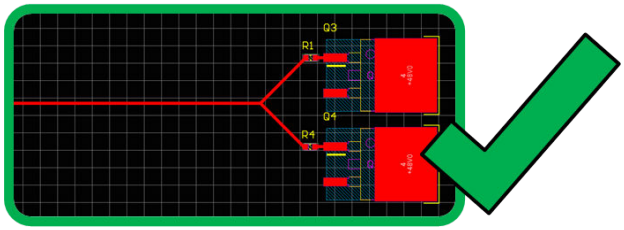

Figure 5. Example of Recommended Gate Layout

Layout Drain and Source Considerations

The following guidelines are helpful for best performance of the MOSFET Drain and Source connections:

- To switch the MOSFETs as simultaneously as possible and minimize power losses, try to **keep MOSFET drain and source connections as similar as possible**.
- Ensure that the source and drain connections for both MOSFETs have strong connections (polygon copper pours are *highly* recommended instead of traces) so that current flow is relatively even. If current flow through one of the MOSFETs is limited by the source or drain connection, it will cause the other MOSFET to take a disproportionate amount of the current, potentially causing thermal issues.
- Thermal relief of the pads is not advised as this reduces current carrying capability and increases thermal resistance which will reduce MOSFET heat sinking to the PCB.

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Figure 6 shows a bad drain and source layout example and Figure 7 shows a recommended drain and source layout example:

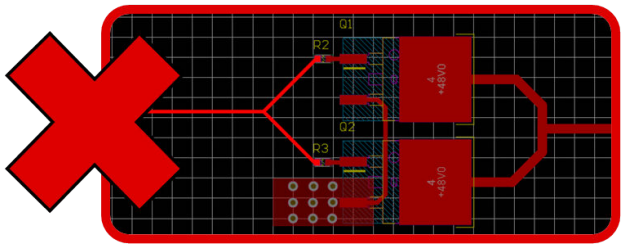

Figure 6. Example of bad Drain and Source Layout

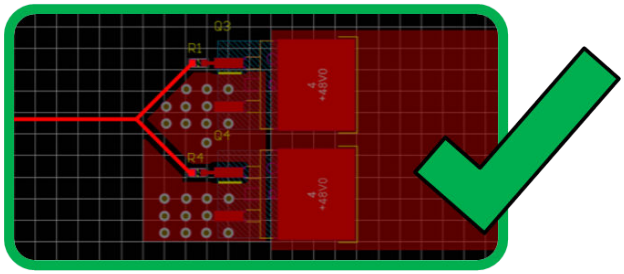

Figure 7. Example of Recommended Drain and Source Layout

Conclusions

This application brief discussed the use of two parallel MOSFETs in high-power applications. The same concept can be adapted to boards using three, four, or more parallel MOSFETs as long as the techniques in this brief are utilized.

A thermally efficient PCB will allow more system power to be delivered to the motor rather than wasting energy to heat generated by inefficiency of MOSFET $R_{DS(on)}$. Applying the techniques described in this document along with those shared in the *Best Practices for Board Layout of Motor Drivers Application Report* will ensure that your next design maintains efficiency while also adding robustness and reducing system power loss.

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