# **JU TEXAS INSTRUMENTS**

#### **ABSTRACT**

The purpose of this study is to characterize the Single-Event Effects (SEE) performance due to heavy-ion irradiation of the TPS7H3014-SP. Heavy-ions with LET $_{\sf EFF}$  of 75MeV $\cdot$ cm $^2$ /mg were used to irradiate production devices. Flux of ≈8 × 10<sup>4</sup> ions/cm<sup>2.</sup>s and fluence of ≈10<sup>7</sup> ions/cm<sup>2</sup> per run were used for the characterization. The results demonstrate the TPS7H3014-SP is SEL-free and SEB/SEGR-free at T = 125°C and T = 25°C, respectively. The TPS7H3014-SP was also tested for SET at T = 25°C, results demonstrate the device is SET-free.

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# **1 Introduction**

The TPS7H3014-SP is an integrated 3V to 14V, four channel radiation-hardness assured power-supply sequencer. The channel count can be incremented as needed for the application by connecting multiple ICs in a daisy-chain configuration. The device features sequence up and reverse sequence down control signals (UP and DOWN), SEQ-DONE and PWRGD flags to monitor the sequence and power status of the monitored power tree. Other features for the device include:

- A 599mV  $\pm$  1% threshold voltage
- $24\mu$ A  $\pm$  3% hysteresis current
- Common programmable (268µs to 23.37ms) delay timer – Valid during sequence up and down
- Time-to-regulation programmable timer (264µs to 23.63ms) to track rising voltage on  $SENSE<sub>x</sub>$
- Valid only during sequence up
- Open drain FAULT detection pin to monitor internally generated faults

The device is offered in a 14-pin ceramic package. General device information and test conditions are listed in Table 1-1. For more detailed technical specifications, user-guides, and application notes please go to [TPS7H3014-SP product page.](https://www.ti.com/product/TPS7H3014-SP)



#### **Table 1-1. Overview Information**

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# **2 Single-Event Effects (SEE)**

The primary concern for the TPS7H3014-SP is the robustness against the destructive single-event effects (DSEE): single-event latch-up (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR). In mixed technologies such as the BiCMOS process used on the TPS7H3014-SP, the CMOS circuitry introduces a potential for SEL susceptibility.

SEL can occur if excess current injection caused by the passage of an energetic ion is high enough to trigger the formation of a parasitic cross-coupled PNP and NPN bipolar structure (formed between the p-sub and n-well and n+ and p+ contacts) [[1](#page-20-0), [2](#page-20-0)]. The parasitic bipolar structure initiated by a single-event creates a high-conductance path (inducing a steady-state current that is typically orders-of-magnitude higher than the normal operating current) between power and ground that persists (is "latched") until power is removed, the device is reset, or until the device is destroyed by the high-current state. During the testing of the TPS7H3014 a total of three units were exposed under worst-case bias conditions for SEL. The TPS7H3014-SP did not exhibit any SEL with heavy-ions with LET<sub>EFF</sub> = 75MeV·cm<sup>2</sup> /mg at flux of ≈8 × 10<sup>4</sup> ions/cm<sup>2</sup> ·s, fluence of ≈10<sup>7</sup> ions/cm<sup>2</sup>, and a die temperature of 125°C.

The TPS7H3014-SP was evaluated for SEB/SEGR at a maximum voltage of 14V ( $V_{IN}$ ) in the waiting to sequence up (all outputs low) and waiting to sequence down (all outputs high) states. Because it has been shown that the MOSFET susceptibility to burnout decrement with temperature [\[5\]](#page-20-0), the device was evaluated while operating under room temperatures. The device was tested with no external thermal control device. During the SEB/SEGR testing, not a single current event was observed, demonstrating that the TPS7H3014-SP is SEB/SEGR-free up to LET<sub>EFF</sub> = 75MeV·cm<sup>2</sup>/mg at a flux of ≈8 × 10<sup>4</sup> ions/cm<sup>2.</sup>s, fluence of ≈10<sup>7</sup> ions/cm<sup>2</sup>, and a die temperature of ≈25°C.

The TPS7H3014-SP was tested under nominal input conditions for SET. During the testing of three devices, not a single transient was recorded, showing that the TPS7H3014-SP is both transient free and SEFI free. To see more details please refer to [Section 8](#page-17-0).



The forcing conditions for the different DSEE and SET testing are shown in Table 2-1.

### <span id="page-4-0"></span>**3 Device and Test Board Information**

The TPS7H3014-SP is packaged in a 22-pin CFP-HFT ceramic package as shown in Figure 3-1. The TPS7H3014-SP evaluation module was used to evaluate the performance and characteristics of the TPS7H3014-SP under heavy ion radiation. The TPS7H3014EVM-CVAL (Evaluation Module) is shown in Figure 3-2. The actual EVM BOM was modified from the original (or default). The board was configured to be dualsite rather than in daisy-chain. This means both samples on a given board were configured under the same conditions (or configuration). Three different configurations were used during the heavy-ions test campaign, the details are provided on [Figure 3-3](#page-5-0), [Figure 3-4](#page-5-0), and [Figure 3-5.](#page-6-0)



**Figure 3-1. Photograph of Delidded TPS7H3014-SP [Left] and Pinout Diagram [Right]**

Note: The package was delidded to reveal the die face for all heavy-ion testing.



**Figure 3-2. TPS7H3014-SP EVM Top View**

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<span id="page-6-0"></span>



**Figure 3-5. TPS7H3014-SP EVM for Worst-Case SET Testing**

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## **4 Irradiation Facility and Setup**

The heavy-ion species used for the SEE studies on this product were provided and delivered by the TAMU Cyclotron Radiation Effects Facility using a superconducting cyclotron and an advanced electron cyclotron resonance (ECR) ion source. At the fluxes used, ion beams had good flux stability and high irradiation uniformity over a 1in diameter circular cross-sectional area for the in-air station. Uniformity is achieved by magnetic defocusing. The flux of the beam is regulated over a broad range spanning several orders of magnitude. For these studies, ion flux of 1.62 × 10<sup>4</sup> to 9.53 × 10<sup>4</sup> ions/cm<sup>2.</sup>s were used to provide heavy-ion fluences of 1.00 ×  $10<sup>7</sup>$  ions/cm<sup>2</sup>.

For the experiments conducted on this report <sup>165</sup>Ho was used to obtain LET<sub>EFF</sub> of 75MeV·cm<sup>2</sup>/mg. The total kinetic energy for each of the ion was:

- $165$ Ho = 2.474GeV (15MeV/nucleon)
	- Ion uniformity for these experiments was between 91% and 95%

Figure 4-1 shows the TPS7H3014EVM-CVAL used for the data collection at the TAMU facility. Although not visible in this photo, the beam port has a 1-mil Aramica window to allow in-air testing while maintaining the vacuum within the accelerator with only minor ion energy loss. The in-air gap between the device and the ion beam port window was maintained at 40mm for all runs.



**Figure 4-1. Photograph of the TPS7H3014-SP EVM in Front of the Heavy-Ion Beam Exit Port at the Texas A&M Cyclotron**

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## **5 Depth, Range, and LET<sub>EFF</sub> Calculation**



#### **Figure 5-1. Generalized Cross-Section of the LBC7 Technology BEOL Stack on the TPS7H3014-SP [Left] and SEUSS 2020 Application Used to Determine Key Ion Parameters [Right]**

The TPS7H3014-SP is fabricated in the TI Linear BiCMOS 250nm process with a back-end-of-line (BEOL) stack consisting of four levels of standard thickness aluminum. The total stack height from the surface of the passivation to the silicon surface is 11.44μm based on nominal layer thickness as shown in Figure 5-1. Accounting for energy loss through the 1-mil thick Aramica beam port window, the 40mm air gap, and the BEOL stack over the TPS7H3014-SP, the effective LET (LET<sub>EFF</sub>) at the surface of the silicon substrate and the depth was determined with the SEUSS 2020 Software (provided by the Texas A&M Cyclotron Institute and based on the latest SRIM-2013 [\[7\]](#page-20-0) models). The results are shown in Table 5-1.



#### **Table 5-1. Ion LET<sub>FFF</sub>, Depth, and Range in Silicon**

# <span id="page-9-0"></span>**6 Test Setup and Procedures**

There were four input supplies used to provide power to the TPS7H3014-SP. The voltage values and the model of the used equipment per the SEE test type is presented in Table 6-1.





As discussed in [Section 3](#page-4-0) the TPS7H3014-SP was tested (or evaluated) under heavy-ions using three unique configurations.

- 1. For DSEE the device was tested under the configuration shown in [Figure 3-3](#page-5-0). We refer to this configuration as the loopback <sup>1</sup>. ENx was tied to SENSEx using a resistive divider with R<sub>TOP</sub> = 100kΩ and R<sub>BOTTOM</sub> = 21kΩ. Under this configuration the overdrive <sup>2</sup> voltage is 1V (typically).
- 2. For SET the device was tested with DLY\_TMR disabled (OPEN). Each SENSE<sub>X</sub> was connected to an external power supply via a resistive divider with  $R_{TOP} = 24.5kΩ$  and  $R_{BOTTOM} = 1.5kΩ$ . Under this configuration the external voltage was controlled to provide an overdrive voltage of ±20mV (typically). The device was tested under:
	- a. Waiting to Sequence UP State (with a  $-20$ mV by forcing  $V_{\text{OUTx}}$  to 6.27V).
	- b. Waiting to Sequence  $\overline{DOWN}$  State (with a +20mV by forcing  $V_{\text{OUTX}}$  to 6.19V).

Transients were monitored on EN1, EN4, and FAULT. The equipment used and the trigger details are summarized in Table 6-2. The device was tested for transients under the Waiting to Sequence UP and Waiting to Sequence DOWN *states*. This was done to ensure the device will not activate/deactivate any downstream device (typically a POL) connected to it.





[Figure 6-1](#page-10-0) shows a block diagram of the setup used for SEE testing of the TPS7H3014-SP.

All boards used for SEE testing were fully checked for functionality. Dry runs were also performed to ensure that the test system was stable under all bias and load conditions prior to being taken to the TAMU facility. During

<sup>&</sup>lt;sup>1</sup> In loopback mode ENx is connected to SENSEx via a resistive divider, for automatic sequence up and down.

 $2\text{ }$  The overdrive is referring to the difference between the steady-state voltage when the hysteresis current is active and the internal  $V_{TH-SSEN}$  reference voltage (599mV typically). For example, for an overdrive voltage of 1V the steady-state voltage is 1.599V when the  $I_{HYS}$  sensex is active.

<span id="page-10-0"></span>

the heavy-ion testing, the LabVIEW control program powered up the TPS7H3014-SP device and set the external sourcing and monitoring functions of the external equipment. After functionality and stability was confirmed, the beam shutter was opened to expose the device to the heavy-ion beam. The shutter remained open until the target fluence was achieved (determined by external detectors and counters). During irradiation, the NI scope cards continuously monitored the signals. When the output exceeded the pre-defined 20% edge trigger, a data capture was initiated. No sudden increases in current were observed (outside of normal fluctuations) on any of the test runs and indicated that no SEL or SEB/SEGR events occurred during any of the tests. Neither, a single transient was capture by the oscilloscope measuring the outputs indicting the device is SET-free.



**Figure 6-1. Block Diagram of the SEE Test Setup for the TPS7H3014-SP**



# <span id="page-11-0"></span>**7 Destructive Single-Event Effects (DSEE)**

### **7.1 Single-Event Latch-Up (SEL) Results**

During SEL characterization, the device was heated using a closed-loop PID controlled heat gun [MISTRAL 6 System (120V, 2400W)]. The DUT temperature was monitored prior to being irradiated with a FLIR IR-camera to ensure the junction temperature. The species used for SEL testing was <sup>165</sup>Ho. Incident angle was used which achieved an LET<sub>EFF</sub> of 75MeV·cm<sup>2</sup>/mg.

Three devices were tested under the loopback mode (for more details in loopback mode refer to [footnote 1\)](#page-9-0). In the loopback mode (used for DSEE) the overdrive voltage was selected to be 1V. This was done to avoid interpreting a transient as a functional interrupt. All devices were tested in the Waiting to Sequence DOWN *state*. Maximum recommend voltages were used for  $V_{IN}$ ,  $V_{PULL-UPx}$  and  $V_{UP}$ . For more configuration information please refer to [Table 6-1](#page-9-0).

Not a single functional interrupt was observed, neither a high current event on either of the power supplies of the TPS7H3014-SP. A total of three units were tested under the same conditions and configuration. This indicates the TPS7H3014-SP is SEL-free. The results for three runs across three devices are shown in Table 7-1. A typical  $V_{\text{IN}}$  current vs time plot during a SEL run is shown in [Figure 7-1.](#page-12-0) Typical  $V_{\text{PULL}}$  UP<sub>x</sub> current vs time plots during SEL runs are shown in [Figure 7-2](#page-12-0) and [Figure 7-3](#page-13-0).



#### **Table 7-1. Summary of TPS7H3014-SP SEL Test Condition and Results**

Using the MFTF method described in *[Single-Event Effects \(SEE\) Confidence Interval Calculations](https://www.ti.com/lit/pdf/slvk047)* application [report](https://www.ti.com/lit/pdf/slvk047) and combining (or summing) the fluence of the four runs @ 125°C (4 × 10<sup>7</sup>), the upper-bound crosssection (using a 95% confidence level) is calculated as:

 $\sigma_{\sf SEL}$  ≤ 1.23 × 10<sup>–7</sup>cm<sup>2</sup>/device for LET<sub>EFF</sub> = 75MeV·cm<sup>2</sup>/mg and T = 125°C.

<span id="page-12-0"></span>

**Figure 7-1. Current vs Time for IIn: Run #1 of the TPS7H3014-SP at T = 125°C**



Figure 7-2. Current vs Time for V<sub>PULL\_UP1</sub>: Run #1 of the TPS7H3014-SP at T = 125°C

<span id="page-13-0"></span>



Figure 7-3. Current vs Time for V<sub>PULL\_UP2</sub>: Run #1 of the TPS7H3014-SP at T = 125°C

<span id="page-14-0"></span>

#### **7.2 Single-Event Burnout (SEB) and Single-Event Gate Rupture (SEGR) Results**

During SEB/SEGR testing, the device was tested at room temperature. The same test conditions, in terms of biasing and voltage levels, apply for SEB/SEGR as was used during the SEL testing. In the case of the SEB/SEGR the device was tested in the following state machine states:

- Waiting to Sequence UP
	- $-$  All outputs are low (ENx = Low, SEQ DONE = LOW, and PWRGD = Low)
	- $-$  The device is waiting for a rising edge in UP to start the sequence up.
	- VUP = 0V (only difference from the SEL biasing)
- Waiting to Sequence DOWN
	- $-$  All outputs are high (ENx = High, SEQ DONE = High, and PWRGD = High)
	- The device is waiting for a falling edge in to start a sequence down.

For more configuration information, please refer to [Table 6-1.](#page-9-0)

The results for six runs across three devices for  $SEB<sub>X</sub>$  are shown in Table 7-2. Typical V<sub>IN</sub> current vs time plots for SEB/SEGR on and off runs are shown in [Figure 7-4](#page-15-0) and [Figure 7-5](#page-15-0). Typical V<sub>PULL UPx</sub> current vs time plots for SEB/SEGR on and off runs are shown in [Figure 7-6](#page-16-0) through [Figure 7-9](#page-17-0).

<b>RUN#</b>	UNIT#	<b>ION</b>	<b>LET<sub>EFF</sub></b> (MeV cm <sup>2</sup> /mg)	<b>FLUX</b> (ions $cm2/mg$ )	<b>FLUENCE</b> (NUMBER OF <b>IONS</b> )	<b>ON/OFF</b> <b>STATUS</b>	<b>SEB EVENT?</b>
4		165H <sub>O</sub>	75	$2.80 \times 10^{4}$	$1.00 \times 10^{7}$	On	No
5		165H <sub>O</sub>	75	$2.68 \times 10^{4}$	$1.00 \times 10^{7}$	Off	No
6	2	165H <sub>O</sub>	75	$4.90 \times 10^{4}$	$1.00 \times 10^{7}$	On	No
7	2	165H <sub>O</sub>	75	$2.60 \times 10^{4}$	$1.00 \times 10^{7}$	Off	No
8	3	165H <sub>O</sub>	75	$8.86 \times 10^{4}$	$1.00 \times 10^{7}$	On	No
9	3	165H <sub>O</sub>	75	$8.80 \times 10^{4}$	$1.00 \times 10^{7}$	Off	No

**Table 7-2. Summary of TPS7H3014-SP SEB/SEGR Test Condition and Results**

Using the MFTF method described in *[Single-Event Effects \(SEE\) Confidence Interval Calculations](https://www.ti.com/lit/pdf/https://www.ti.com/lit/pdf/slvk047)* application [report,](https://www.ti.com/lit/pdf/https://www.ti.com/lit/pdf/slvk047) the upper-bound cross-section (using a 95% confidence level) is calculated as:

 $\sigma_{\rm SEB}$  ≤ 6.15 × 10<sup>–8</sup>cm<sup>2</sup>/device for LET<sub>EFF</sub> = 75MeV·cm<sup>2</sup>/mg and T = 25°C.



<span id="page-15-0"></span>



On refers to be in the Waiting to Sequence DOWN *state*.





Off refers to be in the Waiting to Sequence UP *state*.



<span id="page-16-0"></span>





Figure 7-7. Current vs Time for V<sub>PULL\_UP2</sub>: SEB On Run #4



<span id="page-17-0"></span>

Figure 7-8. Current vs Time for V<sub>PULL UP1</sub>: SEB Off Run #5



Figure 7-9. Current vs Time for V<sub>PULL\_UP2</sub>: SEB Off Run #5

### **8 Single-Event Transients (SET)**

The primary focus of SETs were heavy-ion-induced transient upsets on EN1, EN4, or FAULT. SET testing was done at room temperature using <sup>165</sup>Ho heavy-ions which produced a LET<sub>EFF</sub> of 75MeV·cm<sup>2</sup>/mg. The output

<span id="page-18-0"></span>signals were monitored by two different scopes, a NI PXIe-5172 and a MSO58. Two PXIe-5172s were used to monitor EN1 and FAULT while the MSO was monitoring EN4. The MSO was triggered using an edge-negative at 2.64V. The PXIe-5172 was triggered with an edge-negative at –20% below the high voltage when in waiting to Sequence DOWN *state.* During the testing when the state machine was in the waiting to Sequence UP *state*, the trigger was set to 0.66V or 0.36V with an edge-positive trigger.

The PXIe-5172 sample rate was set to 2MS/s with a record length of 1M points (or samples). The MSO sample rate was set to 1GS/s and had its horizontal divisions set to 20µs/div (for a total of 200µs). The device was tested with DLY\_TMR disabled (OPEN). Each SENSEx was connected to an external power supply via a resistive divider with R<sub>TOP</sub> = 24.5kΩ and R<sub>BOTTOM</sub> = 1.5kΩ. Under this configuration the external voltage was controlled to provide an overdrive voltage of ±20mV (typically). The device was tested under the following conditions.

- 1. Waiting to Sequence UP State (with a –20mV by forcing VOUTx to 6.27V).
- 2. Waiting to Sequence DOWN State (with a +20mV by forcing VOUTx to 6.19V).

The device was tested on the EVM in two configurations, one shown on [Figure 3-5](#page-6-0) where capacitors are present on VSENSEx (the nominal case) and one shown on [Figure 3-5](#page-6-0) where no capacitors were present (worst-case). The device was also tested under two typical voltages for IN (5V and 12V) and PULL\_UPx (3.3V and 1.8V). Under these configurations not a single transient was recorded on EN1, EN4, or FAULT. This demonstrates the TPS7H3014 is SET-free. The SET test conditions and results for three units are shown in Table 8-1.

#### **Table 8-1. Summary of TPS7H3014-SP SET Test Condition and Results**

Note: For runs #18 and #19 the device was tested in loopback mode with the SENSEx caps removed in order to test a "bullet-proof" worst-case, under these conditions the device still showed to be transient free. See [Figure 3-5](#page-6-0) for schematic.



<span id="page-19-0"></span>

### **9 Event Rate Calculations**

Event rates were calculated for LEO (ISS) and GEO environments by combining CREME96 orbital integral flux estimations and simplified SEE cross-sections according to methods described in *[Heavy Ion Orbital Environment](https://www.ti.com/lit/pdf/slvk046)  [Single-Event Effects Estimations](https://www.ti.com/lit/pdf/slvk046)* application report. We assume a minimum shielding configuration of 100 mils (2.54mm) of aluminum, and "worst-week" solar activity (this is similar to a 99% upper bound for the environment). Using the 95% upper-bounds for the SEL, SEB/SEGR, and SET, the event rate calculation for the SEL, SEB/SEGR, and SET are shown in Table 9-1, Table 9-2, and Table 9-2, respectively. **It is important to note that this number is for reference since no SEL, SEB/SEGR, or SET events were observed.**

#### **Table 9-1. SEL Event Rate Calculations for Worst-Week LEO and GEO Orbits**



#### **Table 9-2. SEB/SEGR Event Rate Calculations for Worst-Week LEO and GEO Orbits**



#### **Table 9-3. SET Event Rate Calculations for Worst-Week LEO and GEO Orbits**



<span id="page-20-0"></span>The purpose of this study was to characterize the effect of heavy-ion irradiation on the single-event effect (SEE) performance of the TPS7H3014-SP. Heavy-ions with LET $_{\sf EFF}$  = 75MeV $\cdot$ cm $^2$ /mg were used for the SEE characterization campaign. Flux of ≈1 × 10<sup>4</sup> to ≈9 × 10<sup>4</sup> ions/cm<sup>2.</sup>s and fluences of ≈10<sup>7</sup> ions/cm<sup>2</sup> per run were used for the characterization. The SEE results demonstrated that the TPS7H3014-SP is free of destructive SEL and SEB/SEGR. The device also shown to be SET free at LET $_{\sf EFF}$  = 75MeV $\cdot$ cm $^2$ /mg and across the full electrical specifications. CREME96-based worst-week event-rate calculations for LEO (ISS) and GEO orbits for the DSEE and SET are presented for reference.

## **A References**

- 1. M. Shoga and D. Binder, "Theory of Single Event Latchup in Complementary Metal-Oxide Semiconductor Integrated Circuits", *IEEE Trans. Nucl. Sci., Vol. 33(6)*, Dec. 1986, pp. 1714-1717.
- 2. G. Bruguier and J. M. Palau, "Single particle-induced latchup", *IEEE Trans. Nucl. Sci., Vol. 43(2)*, Mar. 1996, pp. 522-532.
- 3. G. H. Johnson, J. H. Hohl, R. D. Schrimpf and K. F. Galloway, "Simulating single-event burnout of n-channel power MOSFET's," in IEEE Transactions on Electron Devices, vol. 40, no. 5, pp. 1001-1008, May 1993.
- 4. J. R. Brews, M. Allenspach, R. D. Schrimpf, K. F. Galloway,J. L. Titus and C. F. Wheatley, "A conceptual model of a single-event gate-rupture in power MOSFETs," in IEEE Transactions on Nuclear Science, vol. 40, no. 6, pp. 1959-1966, Dec. 1993.
- 5. G. H. Johnson, R. D. Schrimpf, K. F. Galloway, and R. Koga,"Temperature dependence of single event burnout in n-channel power MOSFETs [for space application]," IEEE Trans. Nucl. Sci., 39(6), Dec. 1992, pp.1605-1612.
- 6. TAMU Radiation Effects Facility website.<http://cyclotron.tamu.edu/ref/>
- 7. "The Stopping and Range of Ions in Matter" (SRIM) software simulation tools website. [www.srim.org/](http://www.srim.org/index.htm#SRIMMENU) [index.htm#SRIMMENU](http://www.srim.org/index.htm#SRIMMENU)
- 8. D. Kececioglu, "Reliability and Life Testing Handbook", Vol. 1, PTR Prentice Hall, New Jersey,1993, pp. 186-193.
- 9. ISDE CRÈME-MC website.<https://creme.isde.vanderbilt.edu/CREME-MC>
- 10. A. J. Tylka, J. H. Adams, P. R. Boberg, et al.,"CREME96: A Revision of the Cosmic Ray Effects on Micro-Electronics Code", *IEEE Trans. on Nucl. Sci., Vol. 44(6)*, Dec. 1997, pp. 2150-2160.
- 11. A. J. Tylka, W. F. Dietrich, and P. R. Boberg, "Probability distributions of high-energy solar-heavy-ion fluxes from IMP-8: 1973-1996", *IEEE Trans. on Nucl. Sci.,Vol. 44(6)*, Dec. 1997, pp. 2140-2149.

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