PR422
TMS320VC550x Design 5

FEATURES:

- Provides sequenced core and I/O voltages from 3.3 V input source.
- /RESET delay fixed at 65 ms minimum, 130 ms typical.
- All switching regulators for high efficiency operation.
- Small solution size.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at http://power.ti.com then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at:
    o http://focus.ti.com/lit/ds/symlink/tps62300.pdf
    o http://focus.ti.com/lit/ds/symlink/tps3103k33.pdf


THEORY OF OPERATION:

PR422 consists of a series pass transistor for the I/O voltage and a TPS62300 buck regulator for the core voltage. A TPS62300 is used to convert the 3.3 V to the selected core voltage. A series pass transistor is used to switch a regulated 3.3 V supply to the I/O rail.

CIRCUIT LIMITATIONS AND CAPABILITIES:

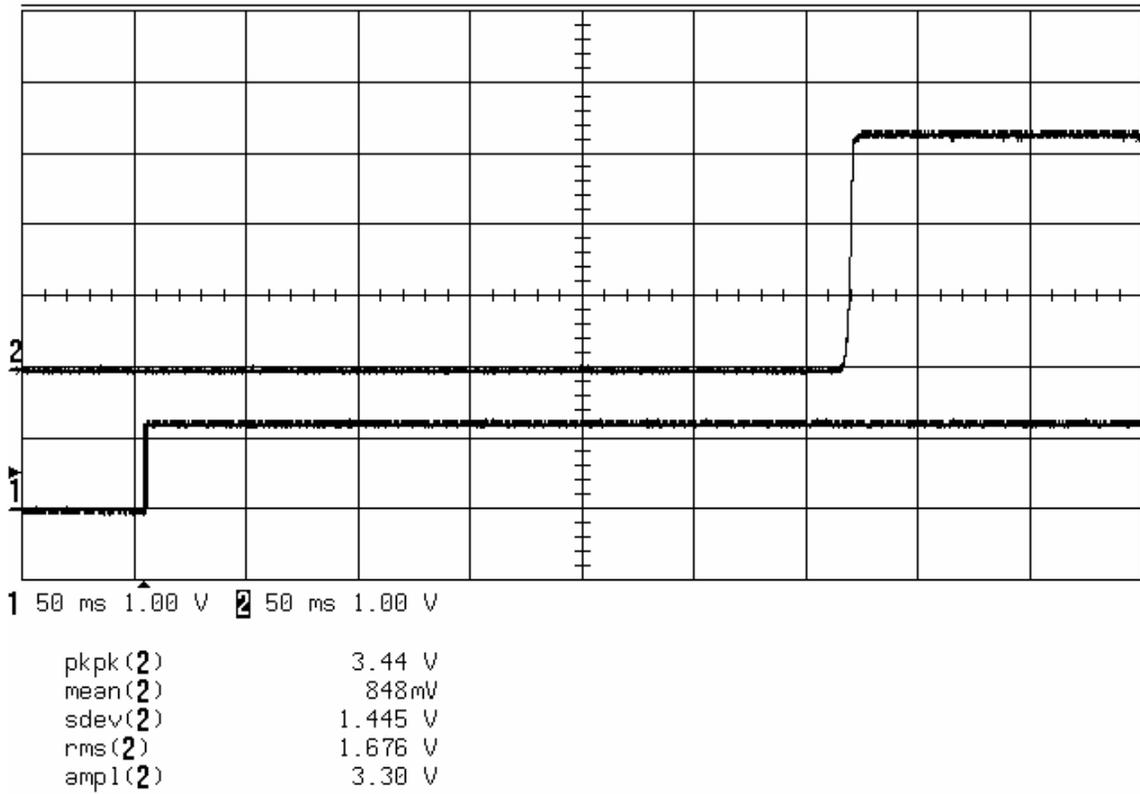The TPS62300 is capable of supplying 500 mA of core current.

POWER UP SEQUENCING:
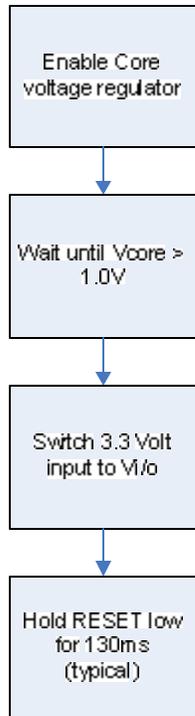
The circuit will switch the I/O voltage on about 200ms after the core voltage is above about 1.0V. The 1.0V threshold will vary with the characteristics of the transistors used in the sequencing circuit. Some systems may require a different time delay between the core and I/O voltage applications. Capacitor C3 can be adjusted to speed-up or slow down the turn on of the I/O voltage. The turn on time would be delayed by the RC time constant created by R3 and C3.
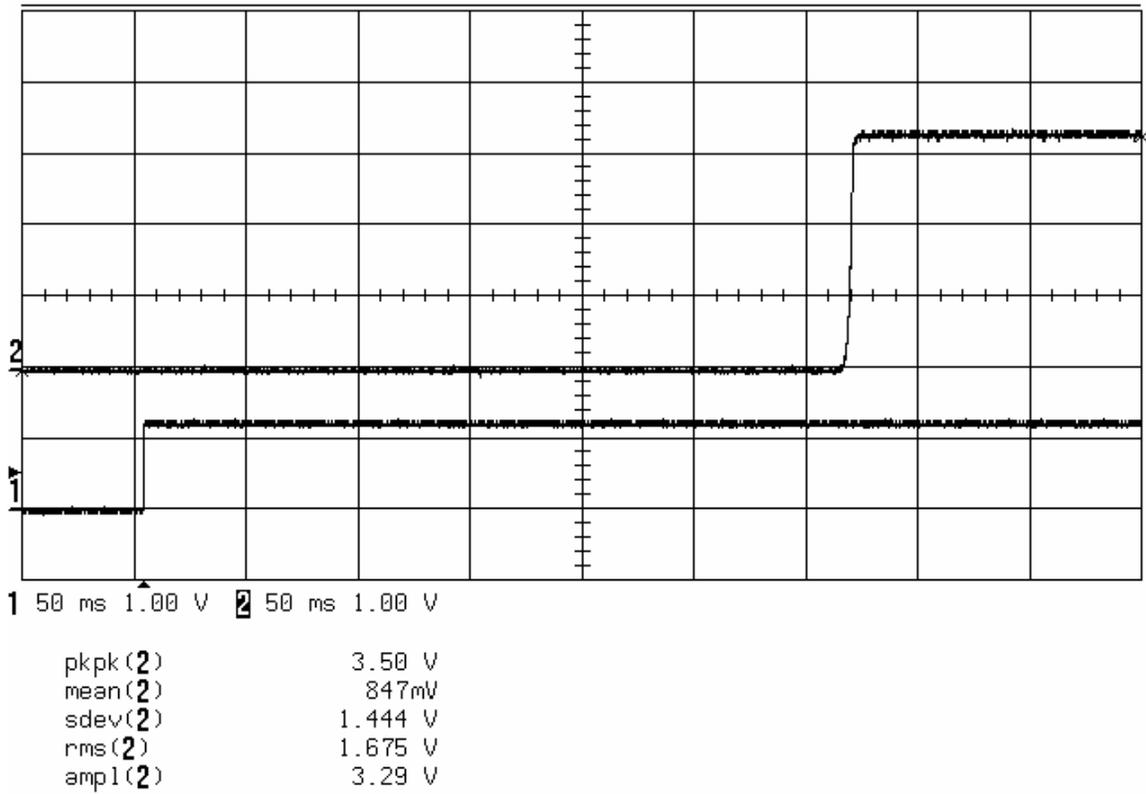
The sequencing circuits can be removed if sequencing is not required. Components R3, R4, C3, Q1 and Q2 can be removed and the 3.3 volt input tied directly to the I/O rail. This will not effect the minimum duration of the RESET signal.

WAVEFORMS:

```
1 50 ms  1.00 V    2 50 ms  1.00 V

   pkpk(2)              3.44  V
   mean(2)              848mV
   sdev(2)             1.445  V
   rms(2)              1.676  V
   ampl(2)             3.30   V

                              □   NORMAL
```

Figure 1 - Power up with V_{IN} = 3.3 V, Vcore=1.2 V @ 110 mA, Vi/o = 3.3 V @ 50 mA

```
1 50 ms  1.00 V    2 50 ms  1.00 V

    pkpk(2)              3.50 V
    mean(2)              847mV
    sdev(2)             1.444 V
    rms(2)              1.675 V
    ampl(2)             3.29 V

                              □   NORMAL
```

Figure 2 - Power up from Enable when V_{IN} = 3.3 V, Vcore=1.2 V @ 110 mA, Vi/o = 3.3 V @ 50 mA

1 50 ms 1.00 V   2 50 ms 1.00 V

```
pkpk(2)          3.44 V
mean(2)          1.566 V
sdev(2)          1.639 V
rms(2)           2.267 V
ampl(2)          3.28 V
```
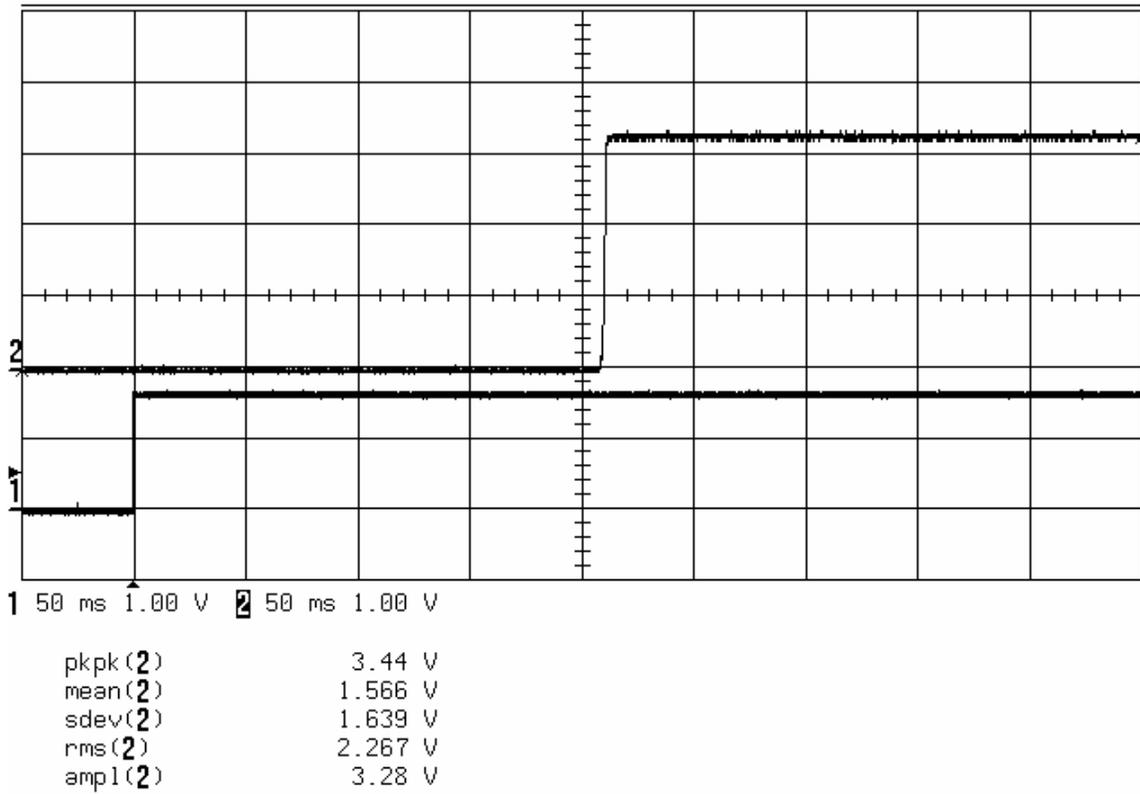
☐ NORMAL

Figure 3 - Power up with V_{IN} = 3.3 V, Vcore=1.6 V @ 250 mA, Vi/o = 3.3 V @ 70 mA

```
1  50 ms  1.00 V   2  50 ms  1.00 V

   pkpk(2)              3.44 V
   mean(2)             1.562 V
   sdev(2)             1.639 V
   rms(2)              2.264 V
   ampl(2)             3.28 V

                              □   NORMAL
```
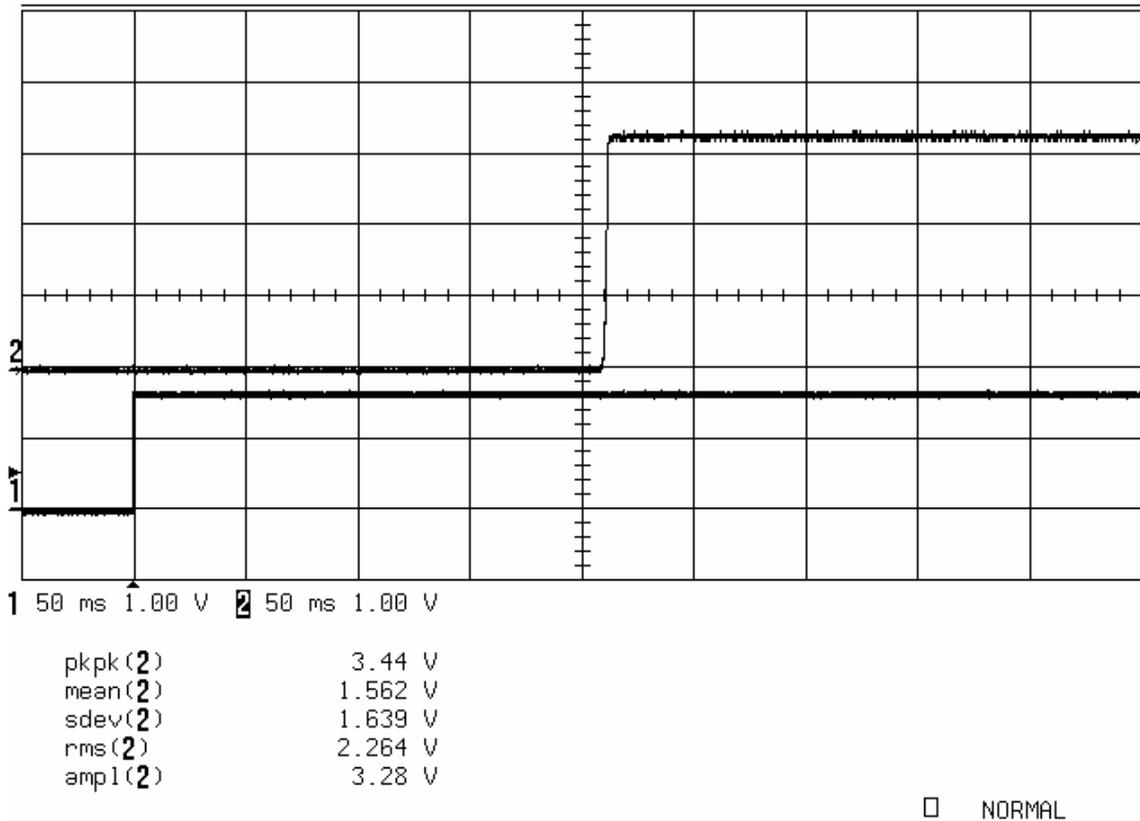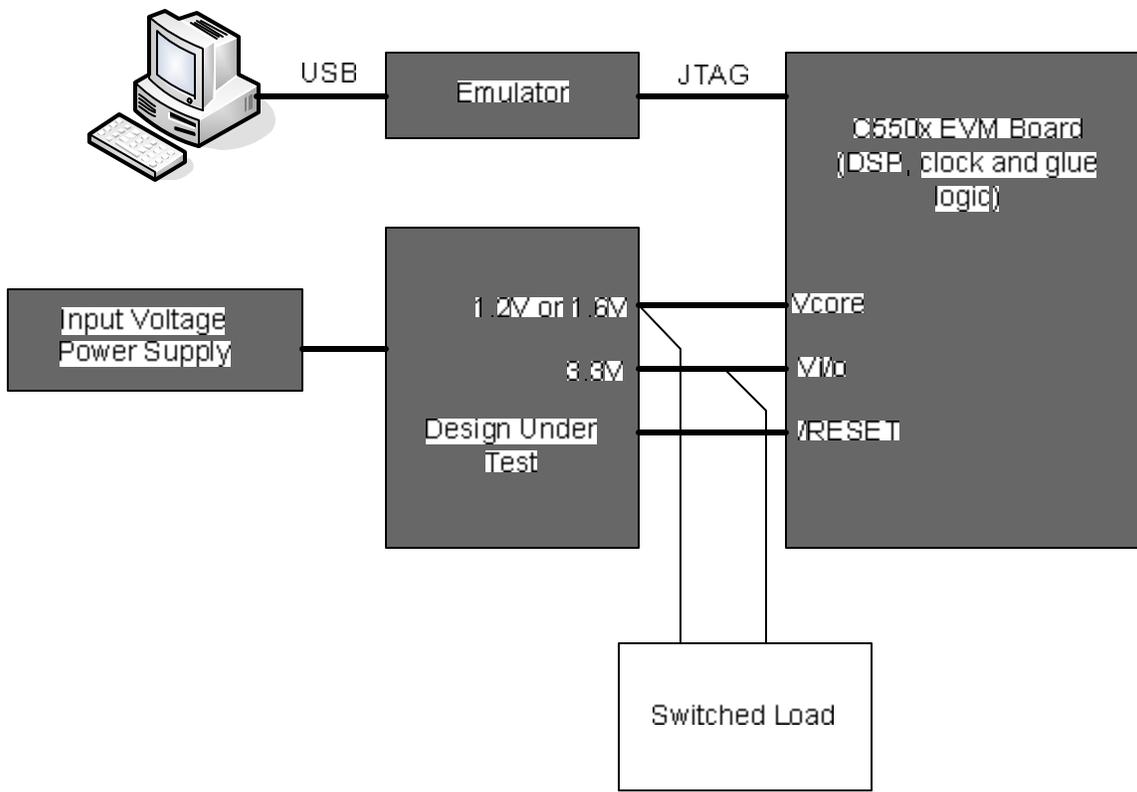
Figure 4 - Power up from Enable when V_{IN} = 3.30 V, Vcore=1.6 V @ 250 mA, Vi/o = 3.3 V @ 70 mA
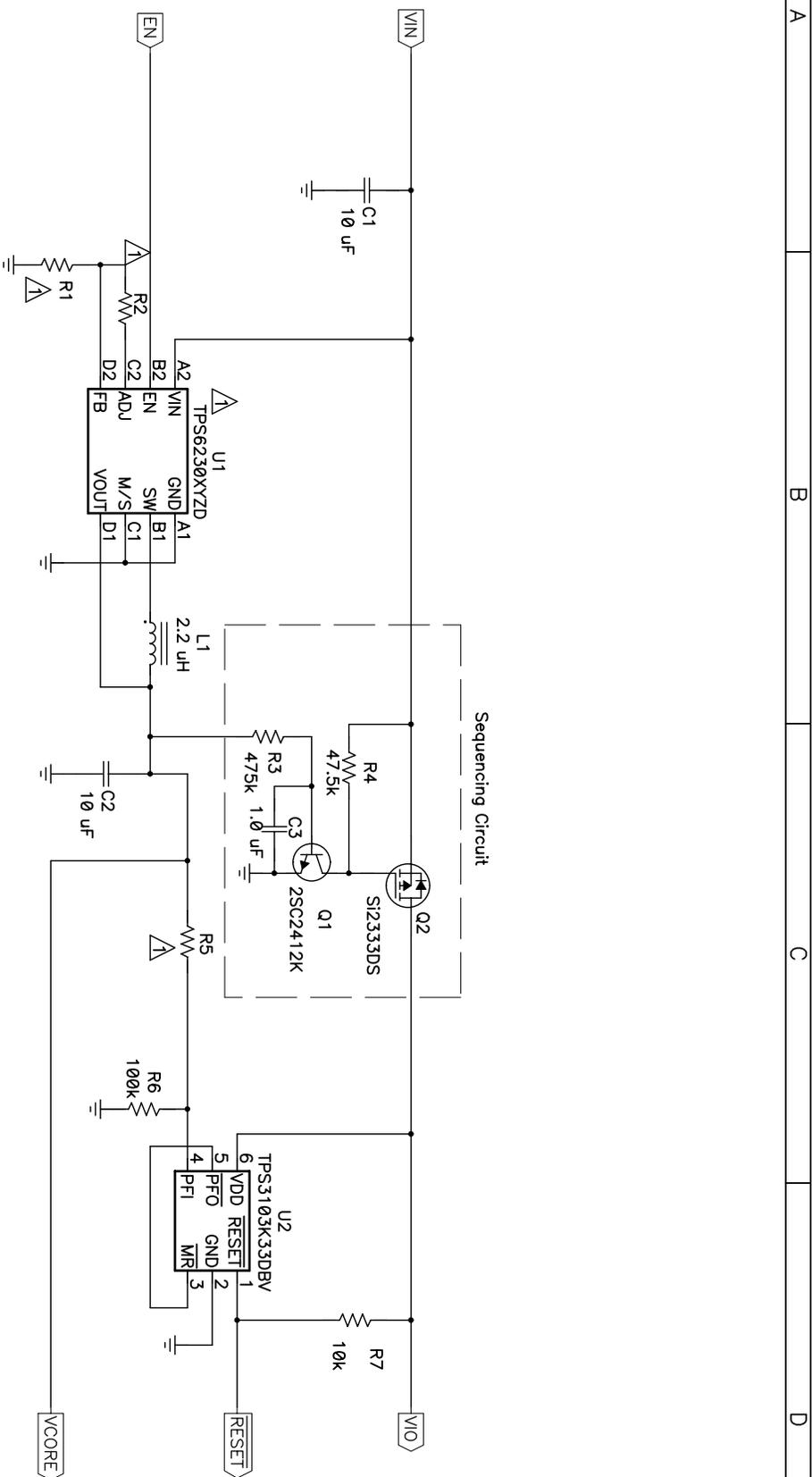
TESTING METHOD:

The solution was tested on the bench and in an actual DSP circuit. Bench testing included start up into full DSP load, switched load from no load to full DSP load, and power up sequencing. The full DSP load is defined as the current draw a C550x DSP would present to the power supply under worst operating conditions. This full DSP load current is heavily dependent on board layout, firmware configurations, DSP clock speed, and core voltage. For testing purposes, the following values were assumed to be the full DSP load current.

Voltage (V)	Function	Full load current (mA)
1.2	core	110
1.6	core	256
3.3	I/O	70

The solution was also tested in an active DSP board. The following test setup was used for this testing:

USB

Emulator

JTAG

C550x EVM Board (DSP, clock and glue logic)

Input Voltage Power Supply

1.2V or 1.6V

Vcore

3.3V

VIo

Design Under Test

/RESET

Switched Load

Send an email to mailto:**dsppower@list.ti.com**

Schematic: C5000 DSP Attach Design 5 for Vin = 3.3V

Title: C5000 DSP Attach Design 5 for Vin = 3.3V
Size: B
Number: PR422
Rev:
Date: 02/14/05
Filename: pr422.sch
Sheet of
Drawn by

Components

- C1 10 uF
- C2 10 uF
- C3 1.0 uF
- L1 2.2 uH
- R3 475k
- R4 47.5k
- R6 100k
- R7 10k
- U1 TPS6230XYZD
- U2 TPS3103K33DBV
- Q1 2SC2412K
- Q2 Si2333DS

Sequencing Circuit

Voltage Table

Voltage	U1	R1	R2	R5
1.2V	TPS62300	332k	332k	97.6k
1.6V	TPS62302	Open	Open	162k

Signals: VIN, EN, VIO, RESET, VCORE

Filename: PR422_bom.xls

Date: 02/14/2005

PR422 BOM

COUNT						
-001	-002	RefDes	Description	Size	Part Number	MFR
2	2	C1, C2	Capacitor, Ceramic, 10-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J106KE01	muRata
1	1	C3	Capacitor, Ceramic, 1.0-uF, 10-V, X5R, 10%	0603	GRM188R61A105KA61	muRata
1	1	L1	Inductor, SMT, 2.2-uH, 770-mA, 230-milliohms	0805	CB2016T2R2M	Taiyo Yuden
1	1	Q1	Transistor, NPN General Purpose, VCE 50V, VCB 60V, VEB 7V, IC 0.15A	SOT-23	2SC2412K	ROHM
1	1	Q2	MOSFET,P-ch, -12 V, 4 A, 51 milliohm	SOT23	Si2333DS	Vishay
1	0	R1	Resistor, Chip, 332k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0		Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
1	0	R2	Resistor, Chip, 332k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0		Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
1	1	R3	Resistor, Chip, 475k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R4	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R5	Resistor, Chip, 97.6k-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 162k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R6	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R7	Resistor, Chip, 10k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	U1	IC, 3MHz Synchronous Step-Down Converter, 400mA	CSP-8	TPS62300YDZ	TI
1	1		IC, 3MHz Synchronous Step-Down Converter, 400mA	CSP-8	TPS62302YDZ	TI
1	1	U2	IC, Ultra Low Current/Supply, Voltage Supervisor	SOT23-6	TPS3103K33DBV	TI

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