User's Guide

SLVU371–March 2009

TPS54240EVM-605 2.5-A, SWIFT™ Regulator Evaluation Module

This user's guide contains information for the TPS54240EVM-605 evaluation module (HPA605). Included are the performance specifications, the schematic, and the bill of materials for the TPS54240EVM-605.

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1 Introduction

This user's guide contains background information for the TPS54240 as well as support documentation for the TPS54240EVM-605 evaluation module (HPA605). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54240EVM-605.

1.1 Background

The TPS54240 dc/dc converter is designed to provide up to a 2.5-A output from an input voltage source of 3.5 V to 40 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small, printed-circuit-board areas that may be achieved when designing with the TPS54240 regulator. The switching frequency is internally set at a nominal 500 kHz. The high-side MOSFET is incorporated inside the TPS54240 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54240 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54240 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 40 V for the TPS54240EVM-605.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54240EVM-605	VIN = 10 V to 20 V	0 A to 2.5 A

1.2 Performance Specification Summary

A summary of the TPS54240EVM-605 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54240EVM-605 is designed and tested for V_{IN} = 10 V to 20 V. The ambient temperature is 25°C for all measurements, unless otherwise noted. Although the EVM is designed and tested to operate from a nominal 12 V input, the input bypass capacitors are rated for 100 V and the catch diode is rated for 60 V. The EVM may be modified by the user to operate from input voltages up to the 60 V operating limit of the TPS54240.

CAUTION

Caution: Risk of electric shock for voltages exceeding 50 VDC.

Table 2. TPS54240EVM-605 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			10	12	20	V
Output voltage set point				3.3		V
Output current range	V_{IN} = 10 V to 20 V		0		2.5	A
Line regulation	I_O = 1.2 A, V_{IN} = 10 V to 20 V			±0.15%		
Load regulation	V_{IN} = 12 V, I_O = 0.001 A to 2.5A			±0.4%		
Load transient response	I_O = 1.5 A to 2.5 A	Voltage change		–70		mV
		Recovery time		0.2		ms
	I_O = 2.5 A to 1.5 A	Voltage change		70		mV
		Recovery time		0.2		ms
Loop bandwidth	V_{IN} = 12 V, I_O = 2.5 A			54.3		kHz
Phase margin	V_{IN} = 12 V , I_O =2.5 A			64		°
Input ripple voltage	I_O = 2.5 A			360		mVpp
Output ripple voltage	I_O = 2.5 A			8		mVpp
Output rise time				6		ms

Table 2. TPS54240EVM-605 Performance Specification Summary (continued)

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating frequency			160		kHz
Maximum efficiency	TPS54240EVM-605, V_{IN} = 12 V, I_O = 0.9 A		84.4%		
CCM/DCM boundary	V_{IN} = 12 V,		0.220		A
Eco-mode™ threshold	V_{IN} = 12 V		45		mA
No load input current (switching)	V_{IN} = 12 V		290		µA

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54240. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The voltage divider of R_6 and R_7 is used to set the output voltage of the EVM. The 51 Ω resistor R_5 is provided as an aid to check the loop response of the circuit. To change the output voltage of the EVM, it is necessary to change the value of resistor R_6. Changing the value of R_6 can change the output voltage above 0.8 V. The value of R_6 for a specific output voltage can be calculated using Equation 1.

$$R_6 = 10\ k\Omega \times \frac{(V_{OUT} - 0.8\ V)}{0.8\ V} \quad (1)$$

Table 3 lists the R_6 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 130 ns, and the maximum duty cycle is less than 94%. Higher duty cycles are possible, but may result in uneven switching behavior. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R_6 Value (kΩ)
1.8	12.4
2.5	21.5
3.3	31.6
5	52.3

Be aware that changing the output voltage can affect the loop response. It may be necessary to modify the compensation components. See the datasheet for details.

1.3.2 Operating Frequency, Slow-Start and UVLO

The operating frequency, slow-start time and UVLO voltage may also be adjusted. R3 sets the operating frequency, C4 sets the slow-start time and the resistor divider of R1 and R2 sets the UVLO start and stop voltages. See the TPS54240 datasheet for details on adjusting these parameters.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54240EVM-605 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS54240EVM-605 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 1.5 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J2 through a pair of 20 AWG wires. The maximum load current capability must be 2.5 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	V_{OUT}, 3.3 V at 0.5 A maximum
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	EN test point. Connect EN to ground to disable, open to enable.
TP4	Slow start monitor test point
TP5	PWRGD test point
TP6	PH test point
TP7	Output voltage test point at voltage divider. Used for loop response measurements.
TP8	Test point between voltage divider network and output. Used for loop response measurements.
TP9	Output voltage test point at OUT connector
TP10	GND test point at OUT connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.8 A with V_{IN} = 12 V, and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS54240EVM-605 at an ambient temperature of 25°C.

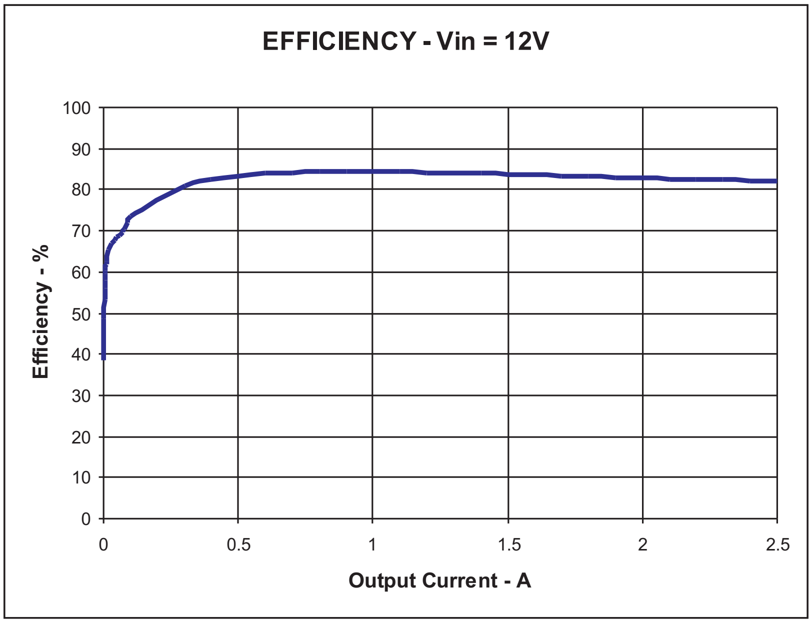

Figure 1. TPS54240EVM-605 Efficiency

Figure 2 shows the efficiency for the TPS54240EVM-605 at lower output currents between 0.001 A and 0.1 A at an ambient temperature of 25°C.

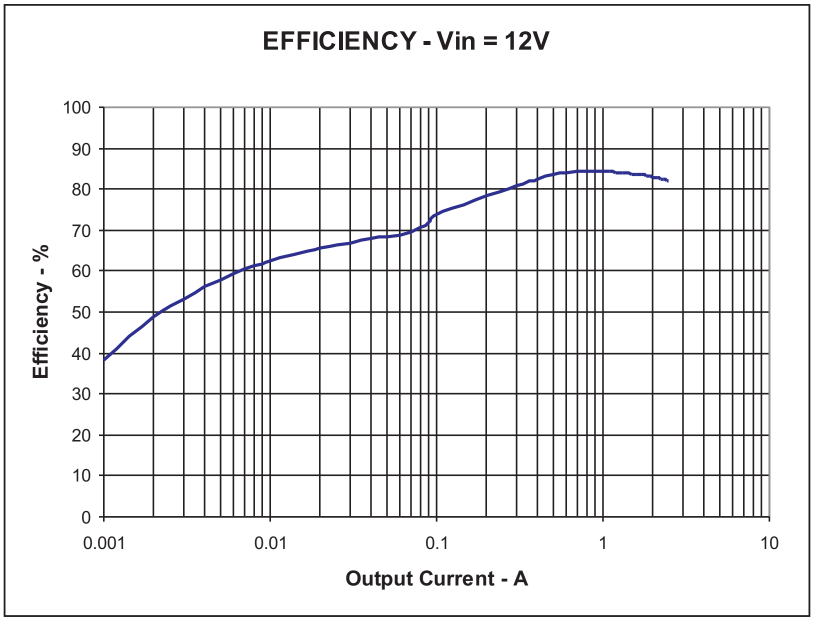

Figure 2. TPS54240EVM-605 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

The load regulation for the TPS54240EVM-605 is shown in Figure 3.

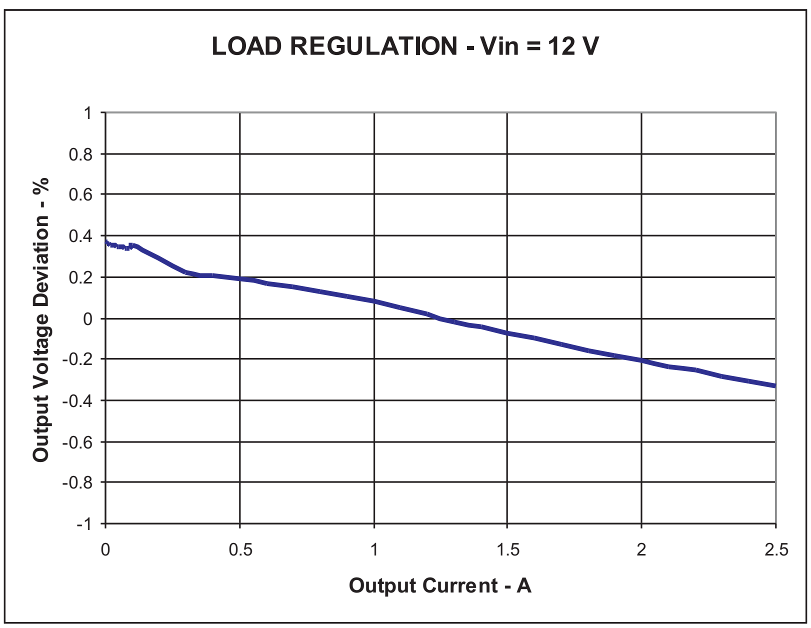

Figure 3. TPS54240EVM-605 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

The line regulation for the TPS54240EVM-605 is shown in Figure 4.

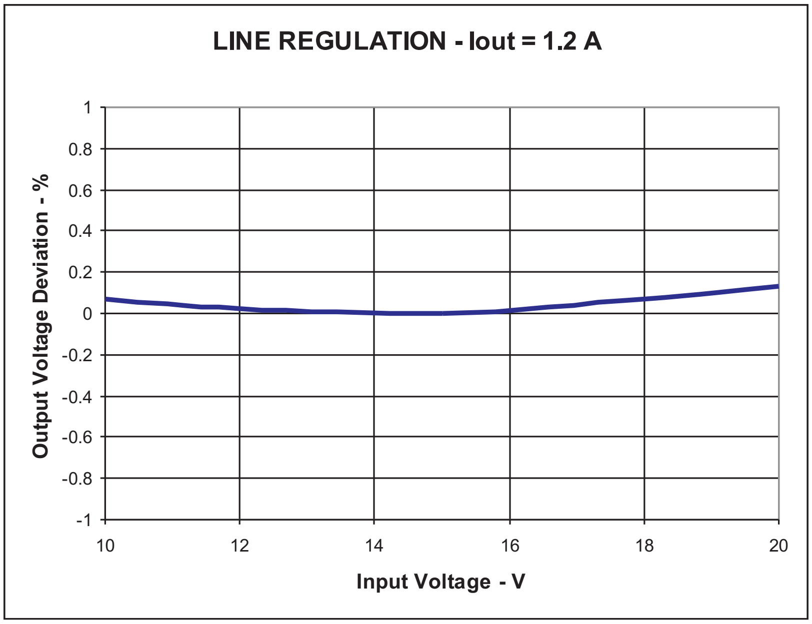

Figure 4. TPS54240EVM-605 Line Regulation

2.5 Load Transients

The TPS54240EVM-605 response to load transients is shown in Figure 5. The current step is from 1.5 A to 2.5 A . The input voltage is 12 V. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

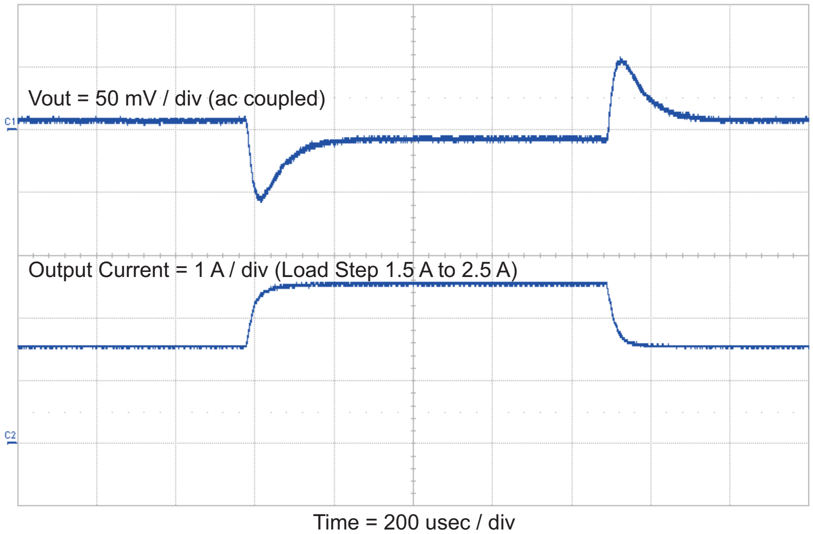

Figure 5. TPS54240EVM-605 Transient Response

2.6 Loop Characteristics

The TPS54240EVM-605 loop-response characteristics are shown in Figure 6 . Gain and phase plots are shown for V_{IN} voltage of 12V. Load current for the measurement is 2.5 A.

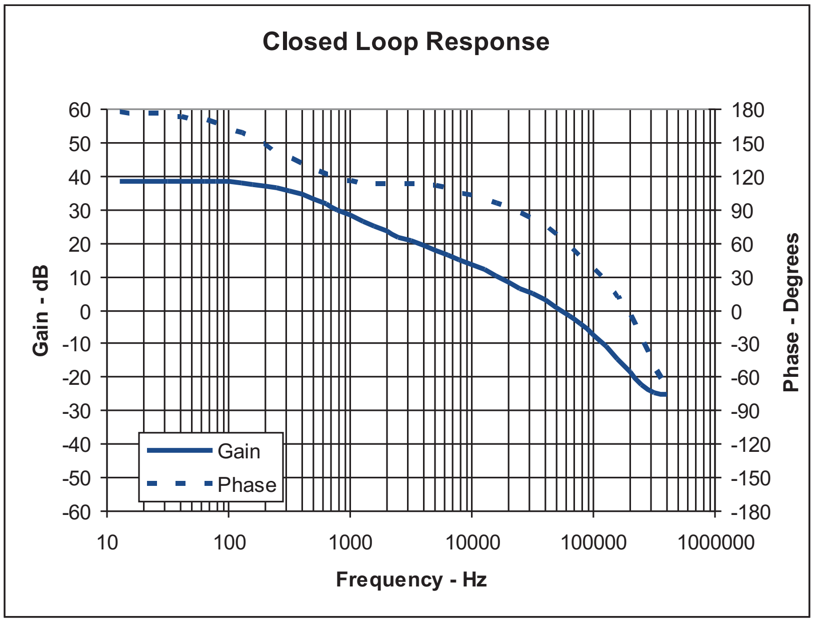

Figure 6. TPS54240EVM-605 Loop Response

2.7 Output Voltage Ripple

The TPS54240EVM-605 output voltage ripple is shown in Figure 7 . The output current is the rated full load of 2.5 A and V_{IN} = 12V. The ripple voltage is measured directly across the output capacitors.

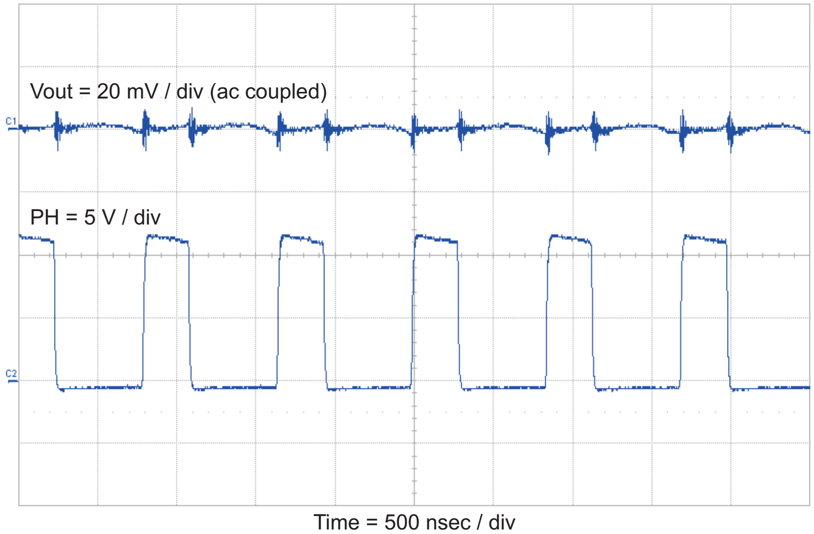

Figure 7. TPS54240EVM-605 Output Ripple

2.8 Input Voltage Ripple

The TPS54240EVM-605 input voltage ripple is shown in Figure 8 . The output current is the rated full load of 2.5 A and V_{IN} = 12 V. The ripple voltage is measured directly across the input capacitors.

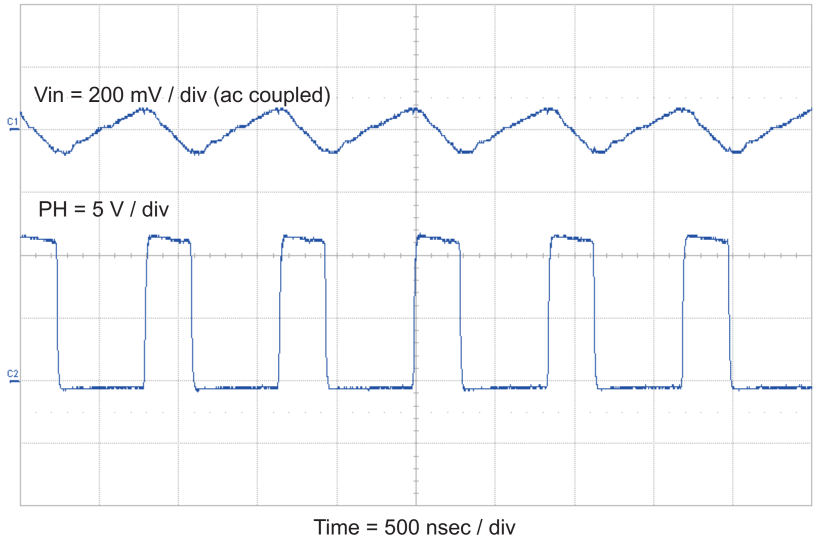

Figure 8. TPS54240EVM-605 Input Ripple

2.9 Powering Up

The start-up waveforms are shown in Figure 9. Start-up is relative to VIN rising. The input voltage is initially applied, and when the input reaches the undervoltage lockout threshold, the start-up sequence begins and the output ramps up at the externally set rate toward the set value of 3.3 V. The input voltage for these plots is 12 V with a 2 Ω load.

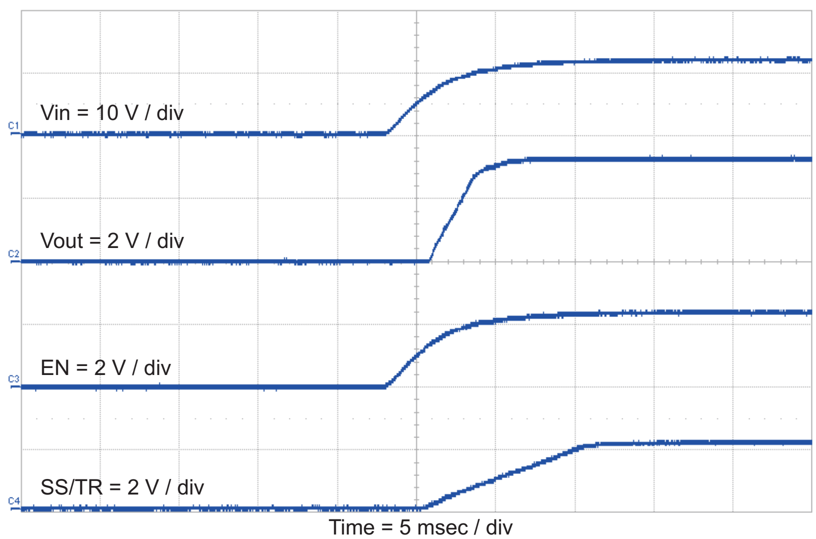

Figure 9. TPS54240EVM-605 Start-Up Relative to V_{IN}

2.10 Continuous Conduction Mode Operation

When the output current is greater than one half the peak to peak inductor current, the circuit is operating in continuous conduction mode (CCM). The output voltage, PH node voltage and inductor current for CCM is shown in Figure 10.

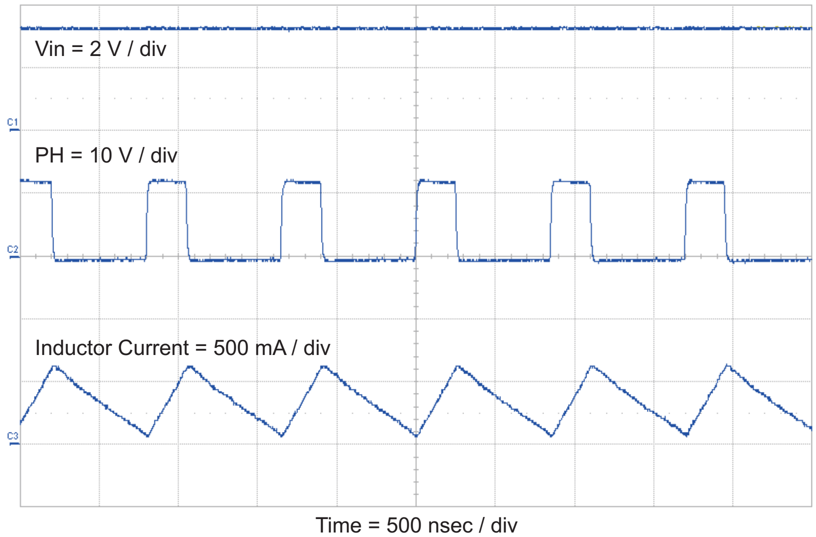

Figure 10. Continuous Conduction Mode Operation

2.11 Discontinuous Conduction Mode Operation

When the output current is less than one half the peak to peak inductor current, the circuit is operating in discontinuous conduction mode (DCM). The circuit enters DCM when the nominal output current falls below 0.337 A. The output voltage, PH node voltage and inductor current for DCM is shown in Figure 11

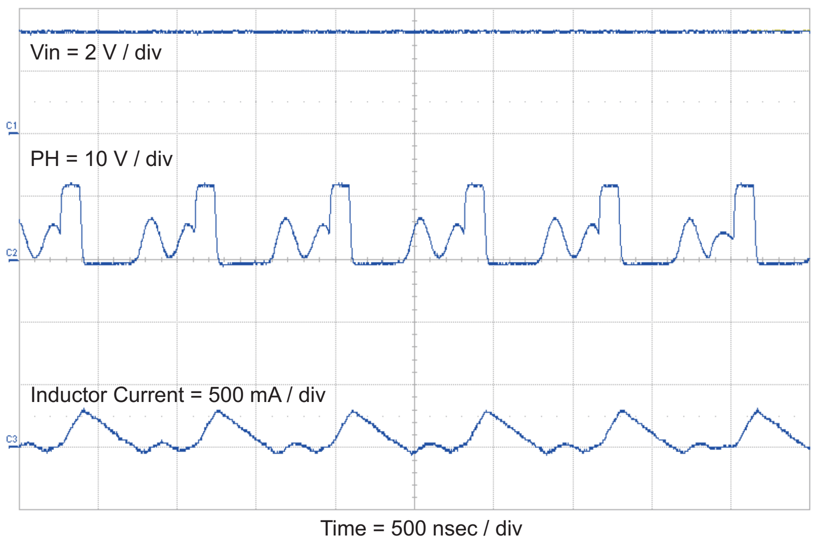

Figure 11. Discontinuous Conduction Mode Operation

2.12 Eco-mode™ Operation

At light load currents, the TPS54240 is designed to operate in the pulse-skipping Eco-mode™ operation. When the COMP pin voltage lowers to 500 mA typical, the device enters the Eco-mode™ operation.

The output voltage, PH node voltage and inductor current for Eco-mode™ is shown inFigure 12.

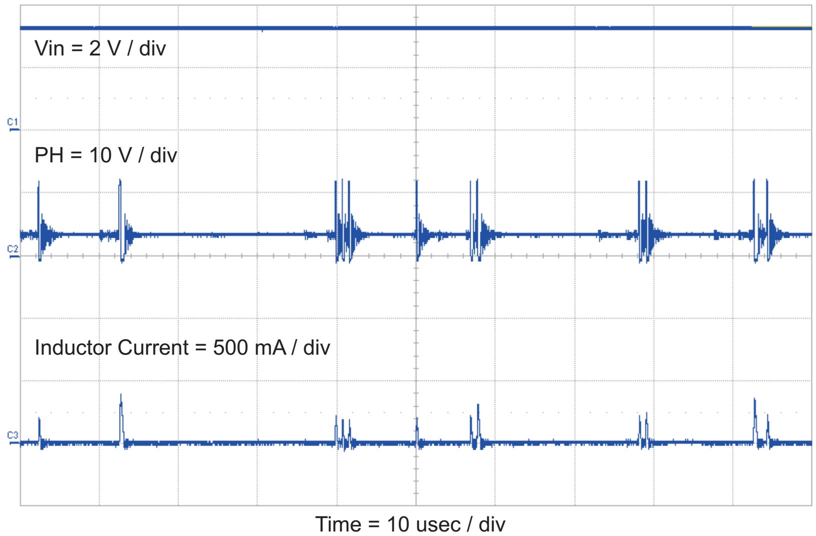

Figure 12. TPS54240EVM–415 Eco–mode™ Operation

3 Board Layout

This section provides a description of the TPS54240EVM-605, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54240EVM-605 is shown in Figure 13 through Figure 15. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54240 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54240 device to provide a thermal path from the top-side ground area to the bottom-side ground plane.

The input decoupling capacitors (C2 and C3) and bootstrap capacitor (C5) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace past the output capacitors (C8 and C9). For the TPS54240, an additional input bulk capacitor may be required (C1), depending on the EVM connection to the input supply.

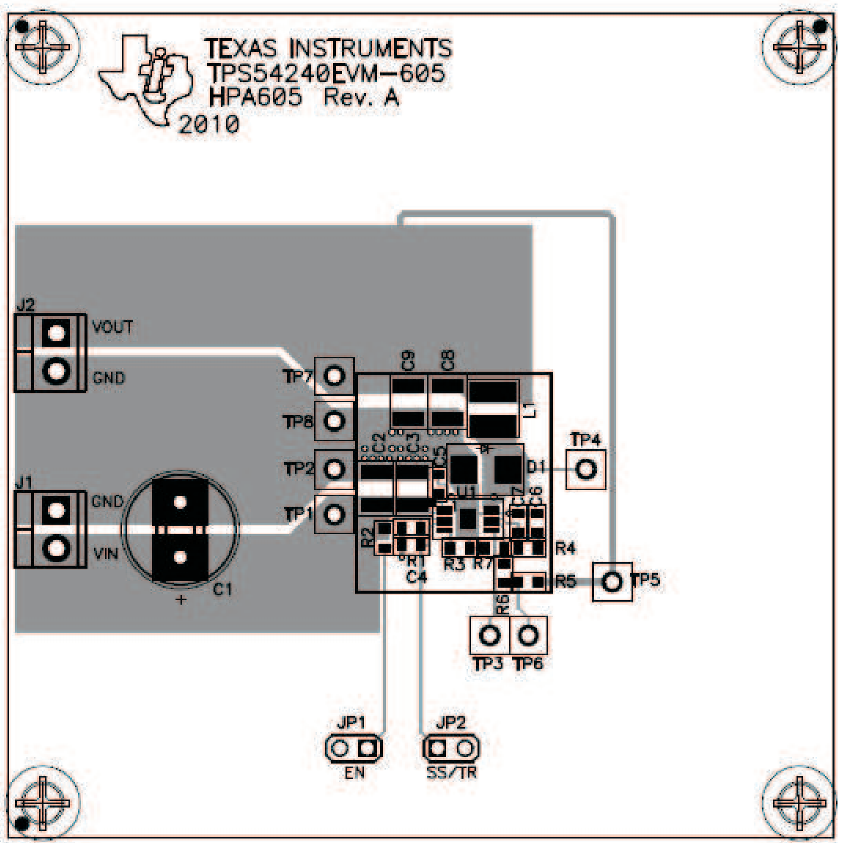

Figure 13. TPS54240EVM-605 Top-Side Assembly

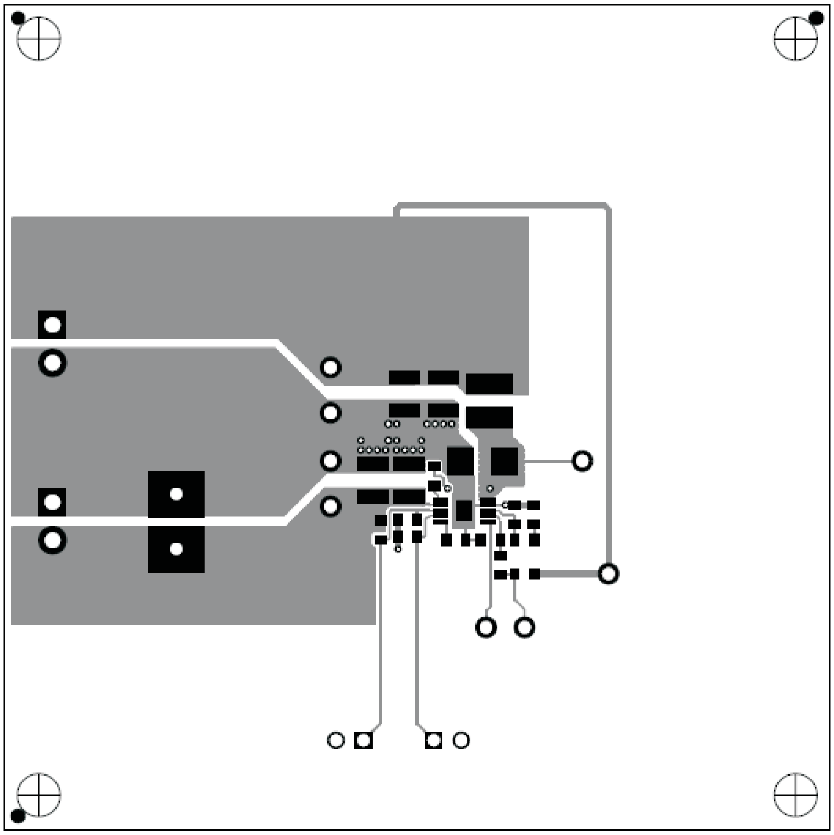

Figure 14. TPS54240EVM-605 Top-Side Layout

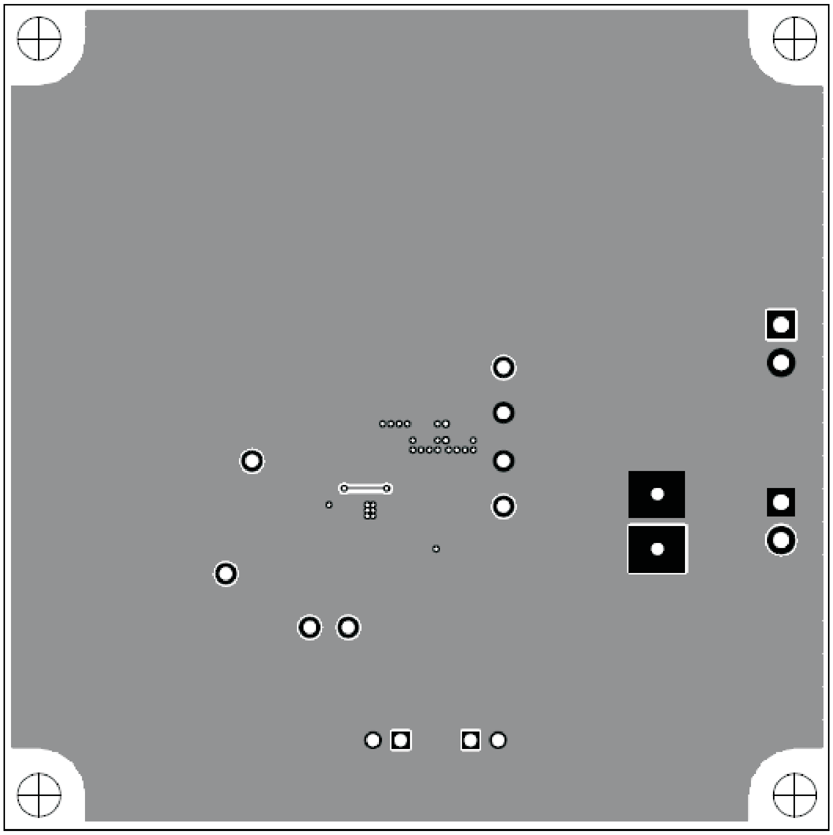

Figure 15. TPS54240EVM-605 Bottom-Side Assembly

3.2 Estimated Circuit Area

The estimated printed-circuit board area for the components used in this design is 0.56 in^2. This area does not include test points or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54240EVM-605 schematic and bill of materials.

4.1 Schematic

Figure 16 is the schematic for the TPS54240EVM-605.

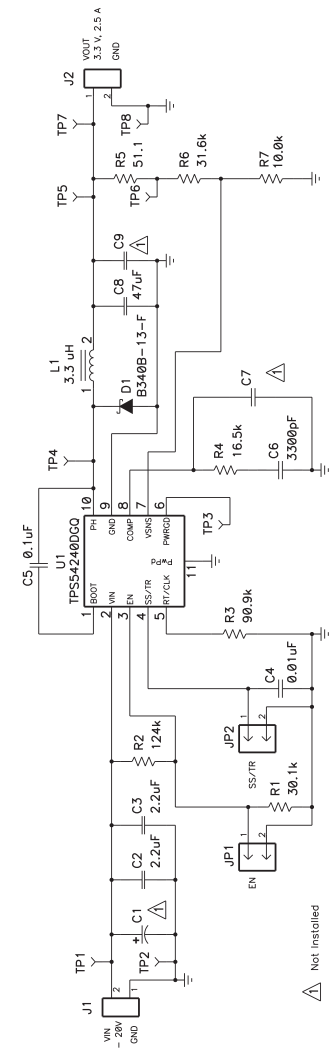

Figure 16. TPS54240EVM-605 Schematic

4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS54240EVM-605.

Table 5. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	open	Capacitor, multi pattern, SM 1210 to E case + F THole	Multi sizes	Engineering Only	Std
2	C2, C3	2.2uF	Capacitor, Ceramic, 100V, X7R, 10%	1210	Std	Std
1	C4	0.01uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
1	C5	0.1uF	Capacitor, Ceramic, 10V, X7R, 10%	0603	Std	Std
1	C6	3300pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
0	C7	open	Capacitor, Ceramic, 25V, X5R, 20%	0603	Std	Std
1	C8	47uF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std
0	C9	open	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std
1	D1	B340B-13-F	Diode, Schottky, 40V, 3A	SMB	B340B-13-F	Diodes, Inc
2	J1, J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25""	ED555/2DS	OST
2	JP1, JP2	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	3.3 uH	Inductor, Power, 2.9 A, 34.8 mohm, ±30%	0.157 x 0.157 inch	XFL4020-332ME	Coilcraft
1	R1	30.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	124k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	90.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	16.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	51.1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	31.6k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
5	TP1, TP4, TP5, TP6, TP7	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
3	TP2, TP3, TP8	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54240DGQ	IC, DC-DC Converter, 3.3V, 2.5A	MSOP-10	TPS54240DGQ	TI
2	–		Shunt, 100-mil, Black	0.100	929950-00	3M
1			PCB, 3.0" x 3.0" x 0.062"	3.0" x 3.0" x 0.062"	HPA605	Any

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.5 V to 40 V and the output voltage range of 0.8 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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