User's Guide
SLVU375–June 2010

A Single-Phase, D-CAP+™ Synchronous Buck Controller for Intel™ Core™ i3/i5/i7Applications

The TPS51621EVM-602 evaluation module (EVM) is a single-phase, D-CAP+™, step-down converter providing 7-bit VID with 0.3-V to 1.5-V output range at up to 40 A from a 12-V input bus. The EVM uses the TPS51621 step-down controller with selectable 200/300/400/500-kHz switching frequency.

Contents

List of Figures

List of Tables

1 Description

The TPS51621EVM-602 is designed to use a regulated 12-V (8-V to 14-V) bus to produce a regulated, variable output at up to 40 A of the load current. The output voltage varies from 0.3 V to 1.5 V via a 7-bit VID digital-to-analog converter (DAC). The TPS51621EVM-602 is designed to demonstrate the TPS51621 in a typical low-voltage application while providing a number of test points to evaluate the performance of the TPS51621.

1.1 Typical Applications

- IMVP-6.5 Vcore applications for adapter, battery, NVDC or 3-V/5-V/12-V rails

1.2 Features

The TPS51621EVM-602 features:

- Output voltage variable from 0.3 V to 1.5 V via a 7-bit VID DAC
- 40-Adc, steady-state current
- Selectable 200/300/400/500-kHz switching frequency
- Selectable current limit
- Selectable output overshoot reduction (OSR™)
- S1 for VR_ON enable function
- Onboard dynamic load
- LEDs light up to indicate corresponding signal is active
- Convenient test points for probing critical waveforms
- Four-layer PCB with 2-oz copper on the outside layer

2 Electrical Performance Specifications

Table 1. TPS51621EVM-602 Electrical Performance Specifications(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
VIN Input Voltage range	VIN	8	12	14	V
Maximum input current	VIN = 8 V,1.5 V/40 A at 300 kHz			8	A
No load input current	VIN = 14 V, Io = 0 A			1	mA
5V Input Voltage range	V5IN	4.5	5	5.5	V
OUTPUT CHARACTERISTICS					
Output voltage Vo	VID0 = VID1 = VID2 = VID3 = VID4 = VID5 = VID6 = 0		1.5		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation (Droop) Load Line		–1.9		mΩ
Output voltage ripple	VIN = 12 V, Io = 40 A at 300 kHz			30	mVpp
Output load current		0		40	A
Output overcurrent	Per phase		26		A
SYSTEMS CHARACTERISTICS					
Switching frequency	Selectable	200	300	500	kHz
Peak efficiency	VIN = 12 V, 1.5 V/20 A at 300 kHz		92.44%		
Full-load efficiency	VIN = 12 V, 1.5 V/40 A at 300 kHz		89.90%		
Operating temperature			25		°C

(1) Jumpers set to default locations, see Section 5.

3 Schematics

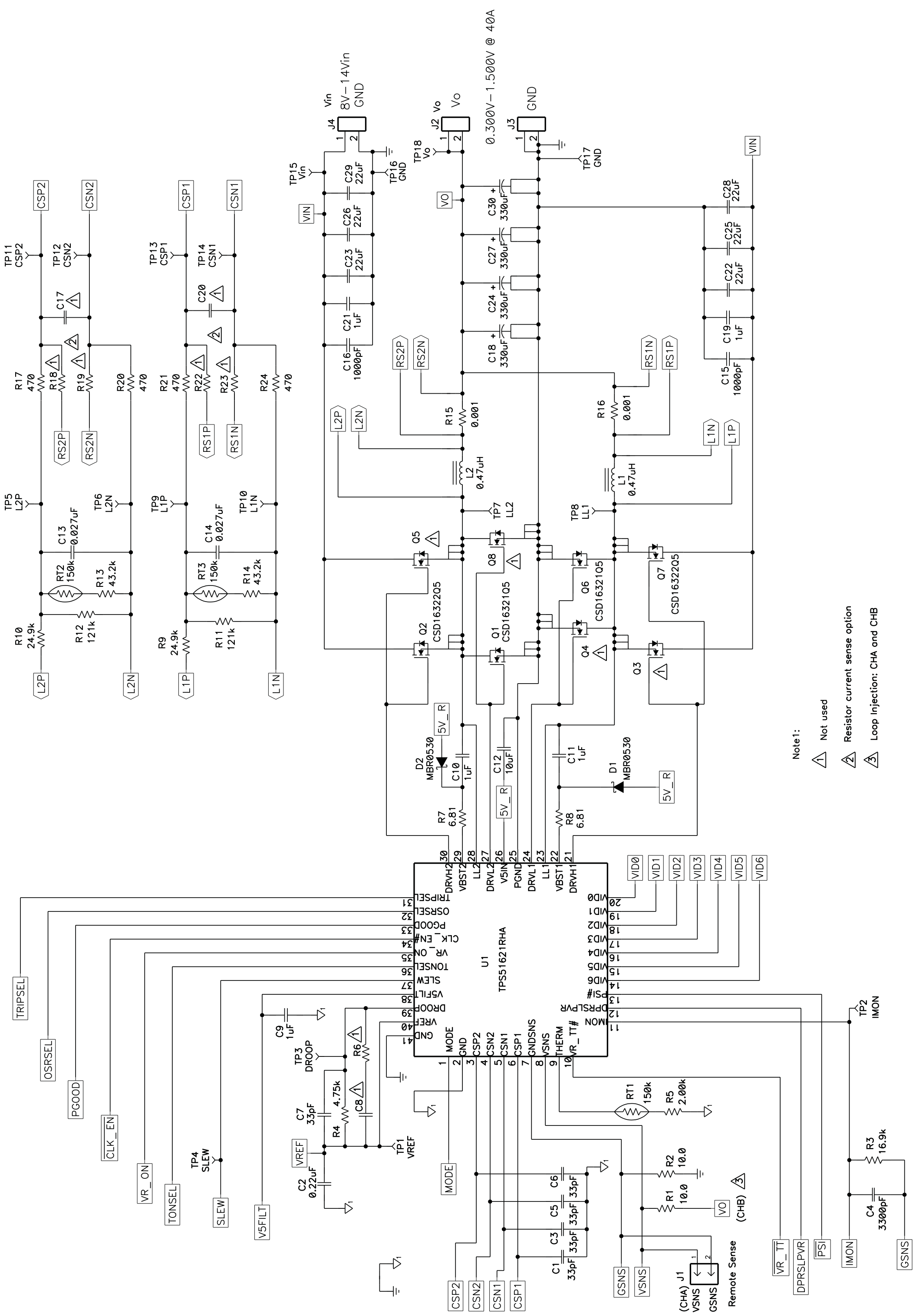


Figure 1. TPS51621EVM-602 Schematic, 1 of 3

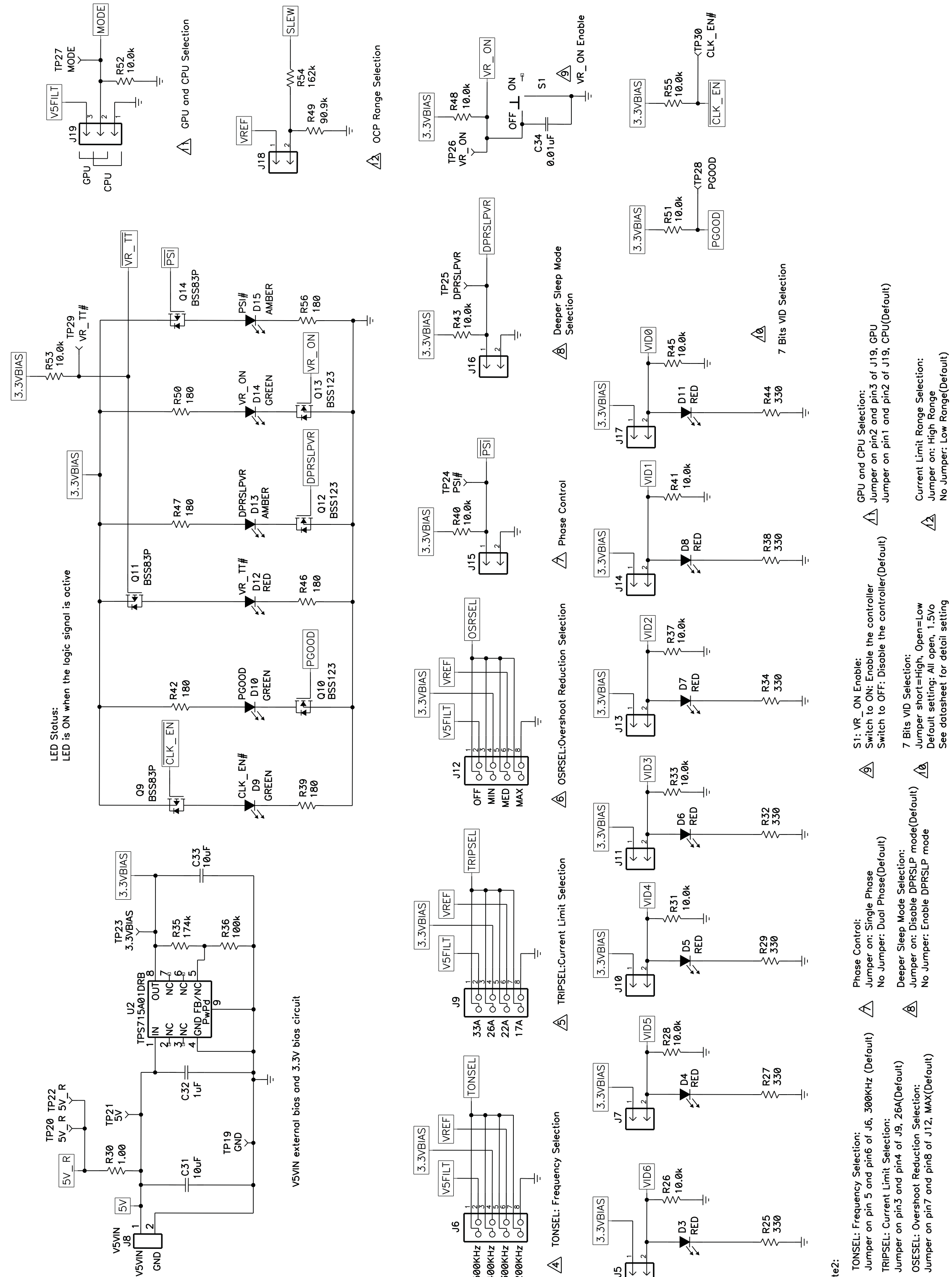


Figure 2. TPS51621EVM-602 Schematic, 2 of 3

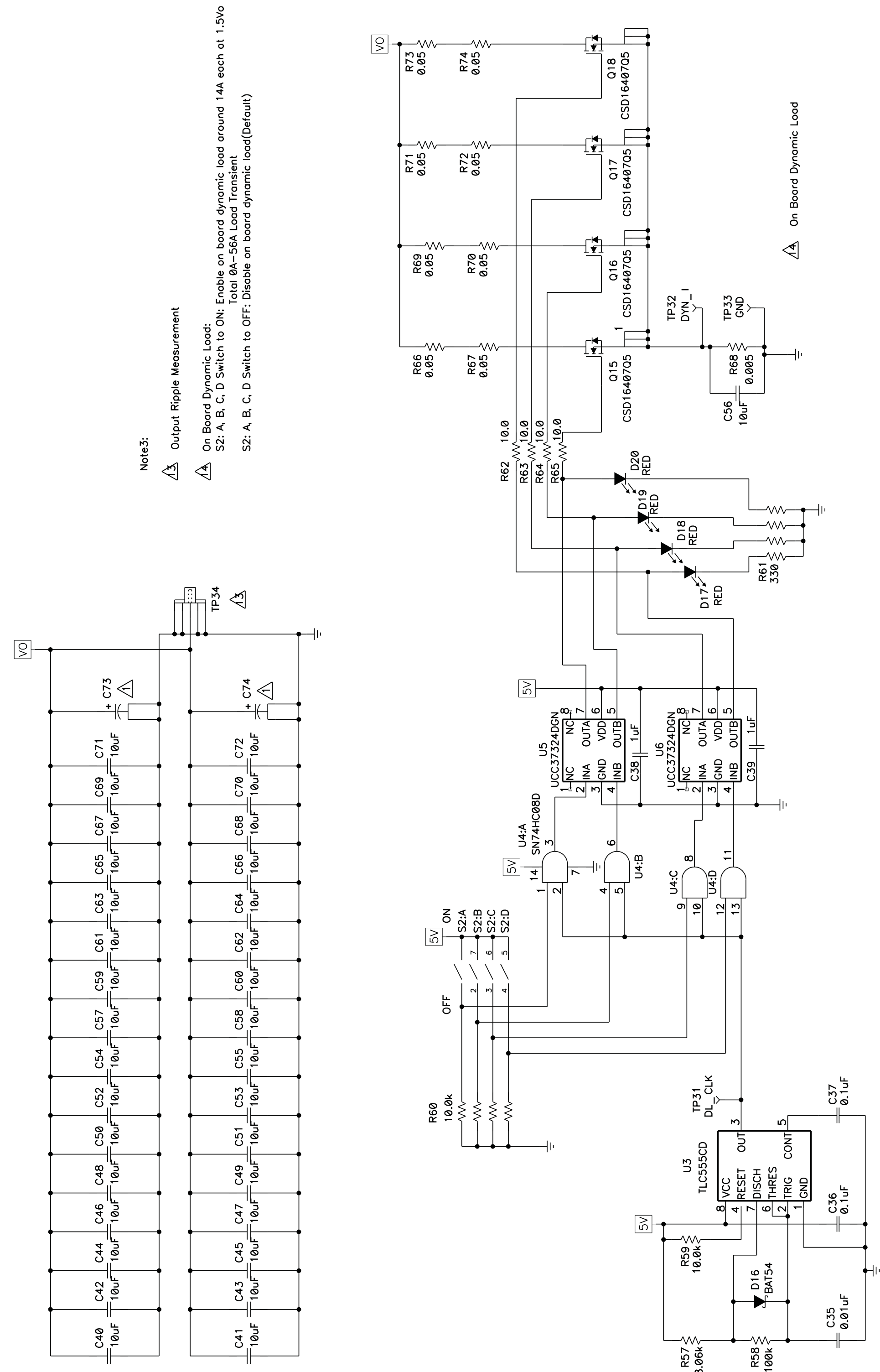


Figure 3. TPS51621EVM-602 Schematic, 3 of 3

4 Test Setup

4.1 Test Equipment

Voltage Source VIN: The input voltage source VIN must be a 0-V to 14-V variable dc source capable of supplying 20-Adc. Connect VIN to J4 as shown in Figure 4.

Voltage Source V5IN: The input voltage source 5 V must be a 0-V to 5.5-V variable dc source capable of supplying 1 Adc. Connect V5VIN to J8 as shown in Figure 4.

Multimeters:
V1: VIN at TP15 (VIN) and TP16 (GND)
V2: V5VIN at TP21 (5 V) and TP19 (GND)
V3: Vo at TP18 (1.5 V) and TP17 (GND)
A1: VIN input current
A2: V5VIN input current

Output Load: The output load must be an electronic Constant Resistance mode load capable of 0 Adc to 50 Adc at 1.5 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 2 µs/division horizontal resolution, 50 mV/division vertical resolution. Test points TP34 can be used to measure the output ripple voltage.

Do not use a leaded ground connection as this may induce additional noise due to the large ground loop.

Fan: Some of the components in this EVM may get hot, approaching temperatures of 60°C or greater during operating. A small fan capable of 200–400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM must not be probed if the fan is not running.

Recommended Wire Gauge:

1. VIN to J4: The recommended wire size is AWG 14 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return).
2. V5VIN to J8: The recommended wire size is AWG 18 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return).
3. J2, J3 to LOAD the minimum recommended wire size is 2X AWG 14, with the total length of wire less than 4 feet (2-foot output, 2-foot return)

4.2 Recommended Test Setup

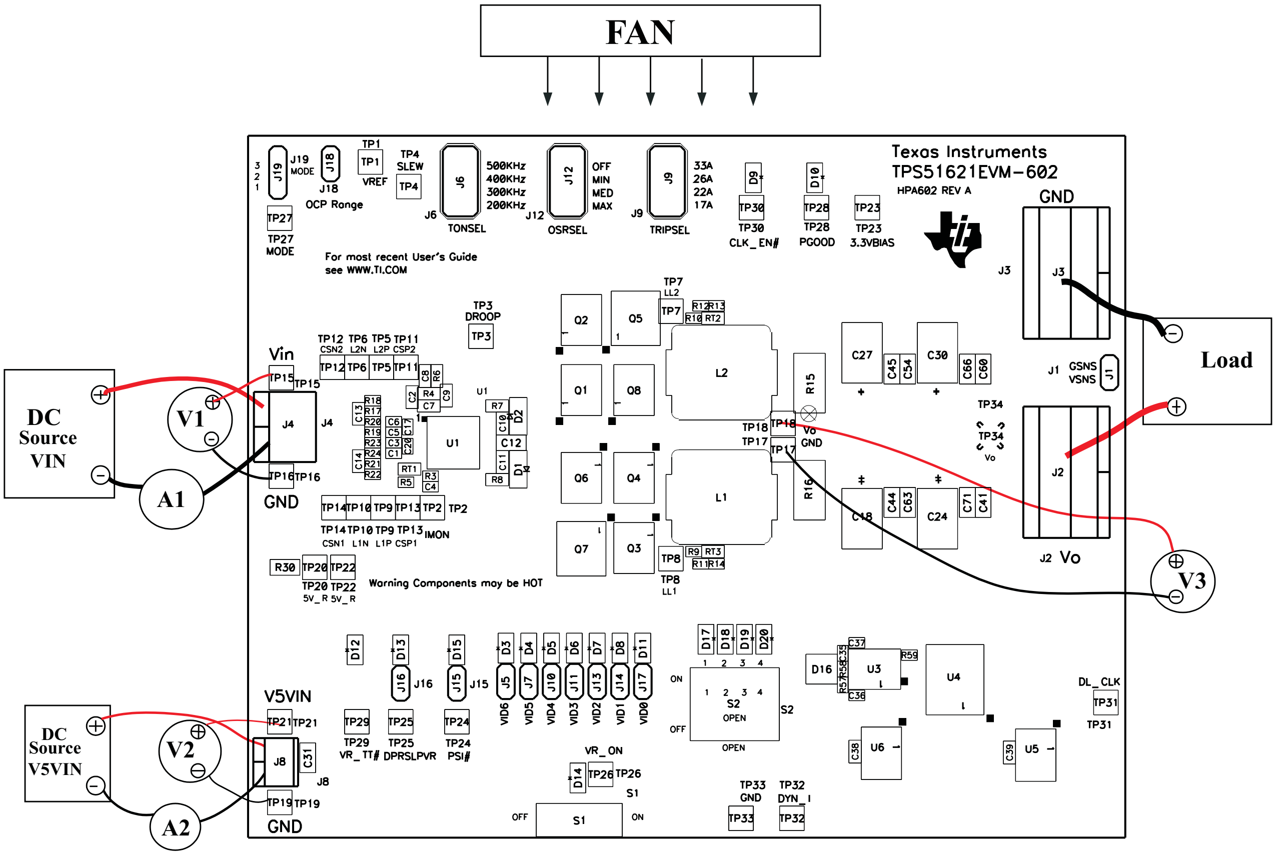


Figure 4. TPS51621EVM-602 Recommended Test Setup

Figure 4 is the recommended test setup to evaluate the TPS51621EVM-602. When working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before handling the EVM.

4.2.1 Input Connections:

1. Prior to connecting the dc input source VIN, it is advisable to limit the source current from VIN to 10 A maximum. Ensure that VIN is initially set to 0 V and connected as shown in Figure 4.
2. Prior to connecting the dc input source V5VIN, it is advisable to limit the source current from V5VIN to 1 A maximum. Ensure that 5 V is initially set to 0 V and connected as shown in Figure 4.
3. Connect a voltmeter V1 at TP15(VIN) and TP15(GND) to measure VIN input voltage.
4. Connect a current meter A1 between VIN DC source and J4.
5. Connect a voltmeter V2 at TP21(5V) and TP19(GND) to measure 5-V input voltage.
6. Connect a current meter A2 between V5VIN dc source and J8.

4.2.2 Output Connections:

1. Connect load to J2, J3 and set load to Constant Resistance mode to sink 0 Adc before VIN is applied.
2. Connect a voltmeter V3 at TP18 (Vo) and TP17(GND) to measure the Vo voltage.

5 Configuration

All jumper selections must be made prior to applying power to the EVM. The user can configure this EVM per the following configurations.

5.1 Current Limit Trip Selection (J9: Trip Select)

The overcurrent protection (OCP) can be set by J9 Trip Select (TRIPSEL).

Default setting: 26A per phase.

Table 2. Current Limit Trip Selection

Jumper Set to	TRIPSEL	OCP Limit per Phase(Typ.)
Top (1-2 pin shorted)	5VFILT	33 A
Second (3-4 pin shorted)	**3.3VBIAS**	**26 A**
Third (5-6 pin shorted)	VREF	22 A
Bottom (7-8 pin shorted)	GND	17 A

5.2 Frequency Selection (J6: TON Select)

The operating frequency can be set by J6 TON Select (TONSEL).

Default setting: 300kHz.

Table 3. Frequency Selection

Jumper Set to	TONSEL	Frequency (kHz)
Top (1-2 pin shorted)	5VFILT	500
Second (3-4 pin shorted)	3.3VBIAS	400
Third (5-6 pin shorted)	**VREF**	**300**
Bottom (7-8 pin shorted)	GND	200

5.3 Overshoot Reduction Selection (J12: OSR™ Select)

The overshoot reduction can be set by J12 OSR™ Select (OSRSEL).

Default setting: Max.

Table 4. Overshoot Reduction Selection

Jumper Set to	OSR	Overshoot Voltage Reduction
Top (1-2 pin shorted)	5VFILT	OFF
Second (3-4 pin shorted)	3.3VBIAS	Minimum
Third (5-6 pin shorted)	VREF	Medium
Bottom (7-8 pin shorted)	**GND**	**Maximum**

5.4 VID Bits Selection

The Vo voltage can be set by J5, J7, J10, J11, J13, J14, J17 (VID bits).

Default setting: 0000000.

Table 5. VID Bits Selection [1]

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcore (V)
0	**0**	**0**	**0**	**0**	**0**	**0**	**1.5000**
0	0	1	1	0	0	0	1.2000
0	1	0	1	0	0	0	1.0000
0	1	1	1	0	0	0	0.8000
1	0	0	1	0	0	0	0.6000
1	0	1	1	0	0	0	0.4000
1	1	0	0	0	0	0	0.3000

(1) See data sheet for details; 7-bit VID Table (1 = 3.3VBIAS, 0 = GND)

5.5 Deep Sleep Mode Selection (DPRSLPVR)

The Deep Sleep mode can be set by J16.

Default setting: Jumper on DPRSLPVR of J16

Table 6. Deep Sleep Mode Selection

Jumper Set to	Mode
Jumper on DPRSLPVR	**Disable the Deep Sleep mode**
No jumper on DPRSLPVR	Enable the Deep Sleep mode

5.6 Phase Control Option (J15: PSI#)

The phase control option can be set by J15.

Default setting : No Jumper shorts on J15 to set dual phase

Table 7. Phase Control Option

Jumper Set to	Option
No jumper	**Dual Phase**
Jumper shorted	Single Phase

5.7 Overcurrent Protection Range Selection (J18: SLEW)

The overcurrent protection range can be set by J18.

Default setting: No jumper shorts on J18 to set low range

Table 8. Overcurrent Protection Range Selection

Jumper Set to	Selection
No jumper	**Low Range**
Jumper shorted	High Range

5.8 CPU and GPU Mode Selection (J19: Mode)

The CPU and GPU mode can be set by J19.

Default setting: Jumper shorts pin 1 and pin 2 of J19 to set CPU mode

Table 9. CPU and GPU Mode Selection

Jumper Set to	Selection
Jumper shorts on pin 1 and pin 2	**CPU mode**
Jumper shorts on pin 2 and pin 3	GPU mode

5.9 Onboard Dynamic Load Selection (S2)

The onboard dynamic load can be set by S2.

Default setting: Press four switches to OPEN (OFF position) to disable onboard dynamic load (no red LEDs light on)

Table 10. Onboard Dynamic Load Selection

Jumper set to	Selection(1.5Vo)
Press switch S2(1) to ON position	Enable 14A onboard dynamic load
Press switch S2(1, 2) to ON position	Enable 28A onboard dynamic load
Press switch S2(1, 2, 3) to ON position	Enable 42A onboard dynamic load

Table 10. Onboard Dynamic Load Selection (continued)

Jumper set to	Selection(1.5Vo)
Press switch S2(1, 2, 3, 4) to ON position	Enable 56A onboard dynamic load

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Ensure that the load is set to Constant Resistance mode and sinks 0 A.
2. Ensure that all jumper configuration settings are per Section 5.
3. Ensure that S1 VR_ON enable switch is to the left before V5VIN and VIN are applied.
4. Increase V5VIN from 0 V to 5 V. Use V2 to measure 5-V voltage.
5. Increase VIN from 0 V to 12 V. Use V1 to measure VIN voltage.
6. Switch S1 is positioned to the right to enable the controller.
7. The VR_ON, CLKEN#, and PGOOD LEDs illuminate.
8. Vary Load from 0 A to 40 A; Vo must remain in load regulation.
9. Vary VIN from 8 V to 14 V; Vo must remain in line regulation.
10. Switch S1 is positioned to the left to disable the controller.
11. Decrease load to 0 A.
12. Decrease VIN to 0 V.
13. Decrease V5VIN to 0 V.

6.2 Onboard Transient Response Measurement

1. Ensure that all the jumper configuration settings are per Section 5.
2. Remove the load from J2, J3.
3. Ensure that S1 VR_ON enable switch is positioned to the left before V5VIN and VIN are applied.
4. Increase V5VIN from 0 V to 5 V. Use V2 to measure 5-V voltage.
5. Increase VIN from 0 V to 12 V. Use V1 to measure VIN voltage.
6. Use TP31(DL_CLK) and TP33(GND) to measure transient timing signal.
7. Use TP32(DYN_I) and TP33(GND) to measure dynamic current signal.
8. Press switches S2 (1, or 2, or 3, or 4) to ON position based on your application.
9. The onboard dynamic load LEDs(D17, D18, D19, D20) illuminate.
10. Measure the Vo transient response by using TP34.

6.3 Loop Gain/ Phase Measurement

1. Set up EVM as described in Section 6.1 and Figure 4.
2. Connect the isolation transformer to VSNS of J1 and Vo (+) of J2.
3. Connect input signal CHA to VSNS pin of J1, and connect output signal CHB to Vo (+) of J2.
4. Connect the GND lead of CHA and CHB to GND of TP34.
5. Inject around 50-mV or less signal through the isolate transformer.
6. Sweep the frequency from 100 Hz to 1 MHz with 10 Hz or lower post filter. The control loop gain and phase margin can be measured.
7. Disconnect isolate transformer from the bode plot set up before making other measurements (Signal injection into feedback may interfere with accuracy of other measurement.)

6.4 List of Test Points

Table 11. Functions of Each Test Points

Test Points	Name	Description
TP1[(1)]	VREF	1.7-V Reference Voltage
TP2	IMON	Current Monitor Output, Refer to Figure 8
TP3	DROOP	Droop setup
TP4	SLEW	Slew rate
TP5	L2P	Positive current sense output for CH2
TP6	L2N	Negative current sense output for CH2
TP7	LL2	Switching node for CH2
TP8	LL1	Switching node for CH1
TP9	L1P	Positive current sense output for CH1
TP10	L1N	Negative current sense output for CH1
TP11	CSP2	Positive current sense input for CH2
TP12	CSN2	Negative current sense input for CH2
TP13	CSP1	Positive current sense input for CH1
TP14	CSN1	Negative current sense input for CH1
TP15	VIN	12VIN
TP16	GND	Ground
TP17	GND	Ground
TP18	Vo	Vout
TP19	GND	Ground
TP20	5V_R	V5VIN
TP21	5V	5-V external bias
TP22	5V_R	V5VIN
TP23	3.3VBIAS	3.3Vbias
TP24	PSI#	Phase control
TP25	DPRSLPVR	Deep sleep mode control
TP26	VR_ON	IMVP-6.5 VR enable
TP27	MODE	CPU and GPU mode selection
TP28	PGOOD	Power good
TP29	VR_TT#	Thermal flag open-drain output
TP30	CLK_EN#	Clock enable
TP31	DL_CLK	Onboard dynamic load clock signal
TP32	DYN_I	Onboard dynamic load current measurement point
TP33	GND	Ground
TP34	Vo	Output ripple measurement point

(1) For test point locations, see Figure 4

6.5 Equipment Shutdown

1. Shut down load.
2. Shut down VIN and V5VIN.
3. Shut down fan.

7 Performance Data and Typical Characteristic Curves

Figure 5 through Figure 19 present typical performance curves for the TPS51621EVM-602. Jumpers are set to default locations; see Section 5.

7.1 Efficiency

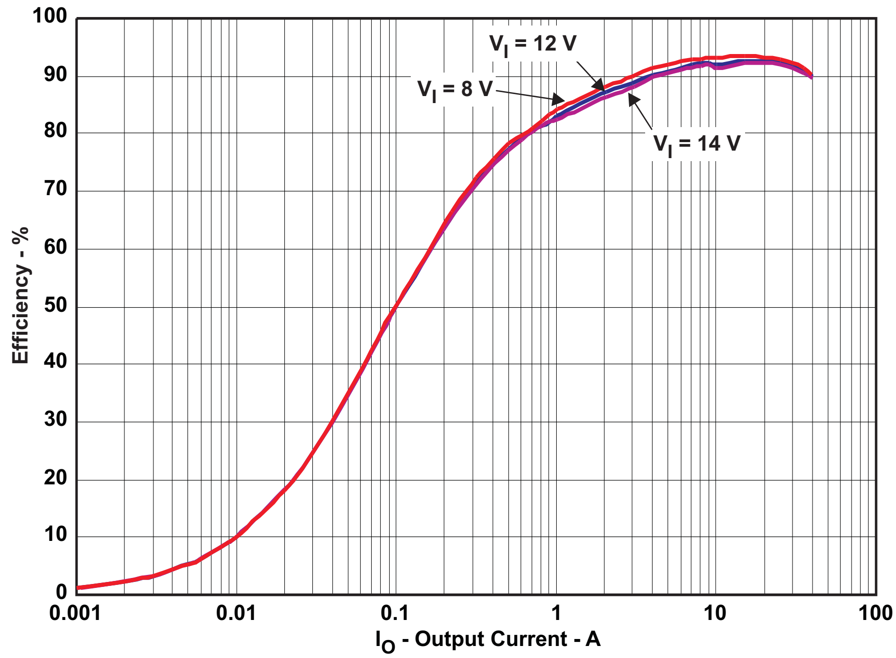


Figure 5. TPS51621EVM-602 Efficiency

7.2 Load Regulation

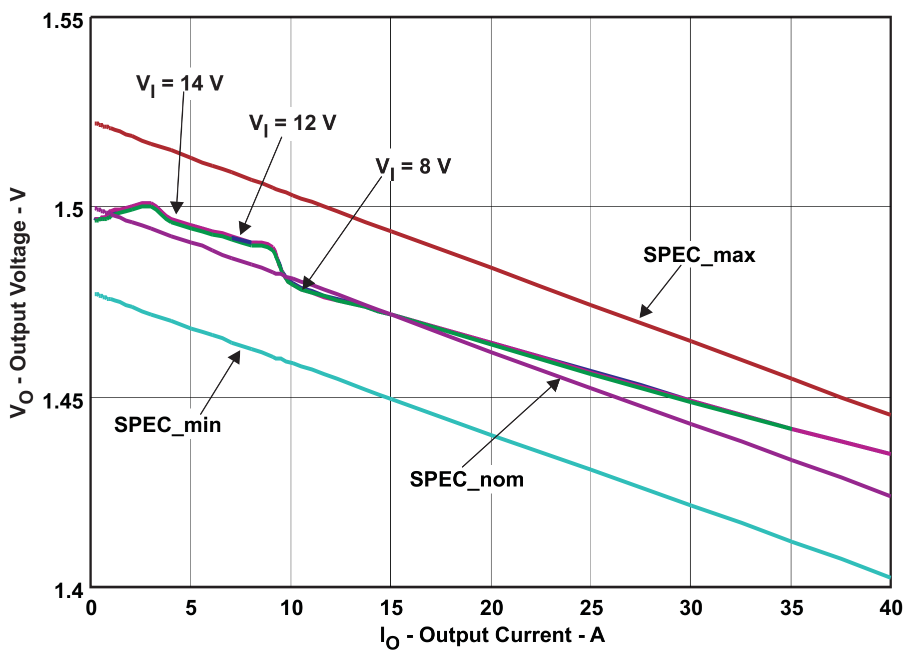


Figure 6. TPS51621EVM-602 Load Regulation

7.3 Line Regulation

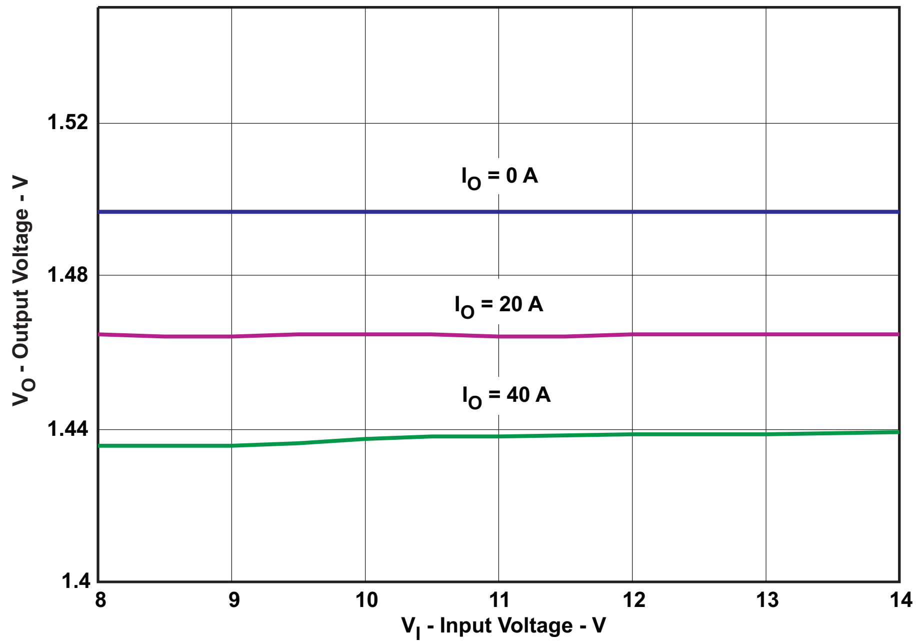


Figure 7. TPS51621EVM-602 Line Regulation

7.4 Current Monitor Voltage

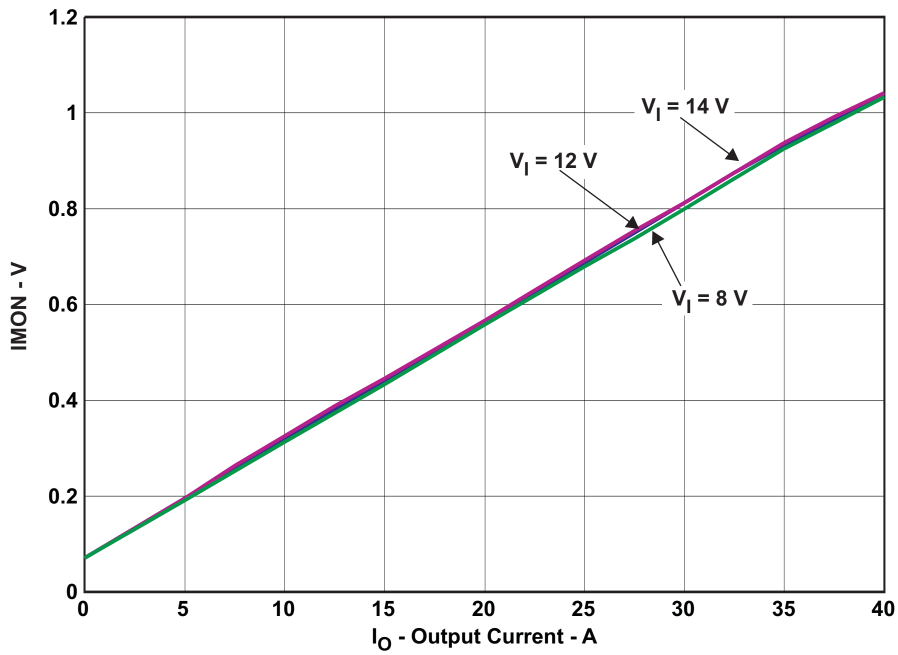


Figure 8. TPS51621EVM-602 IMON Voltage

7.5 Current Share Imbalance

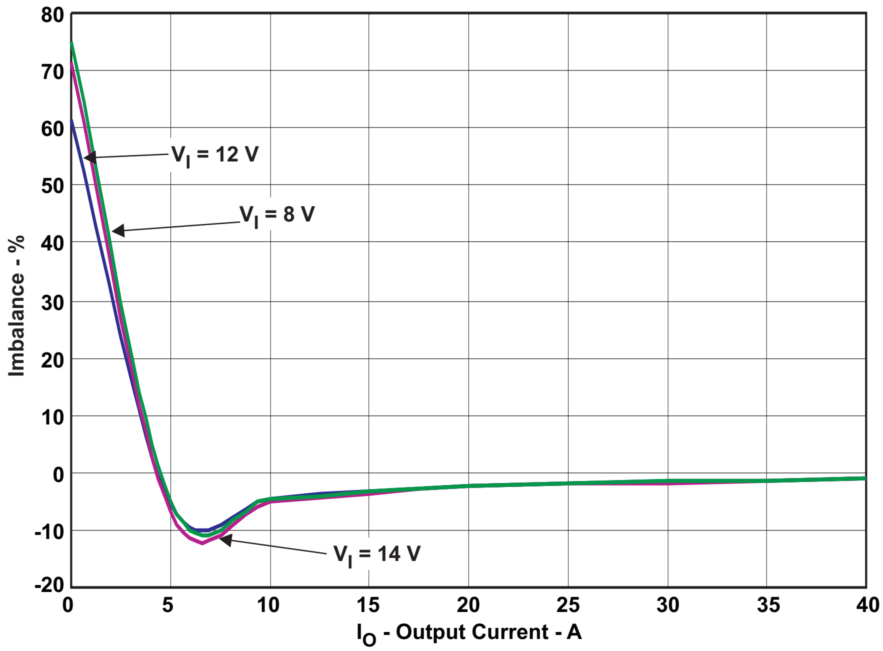


Figure 9. TPS51621EVM-602 Current Share Imbalance

7.6 Output Ripple

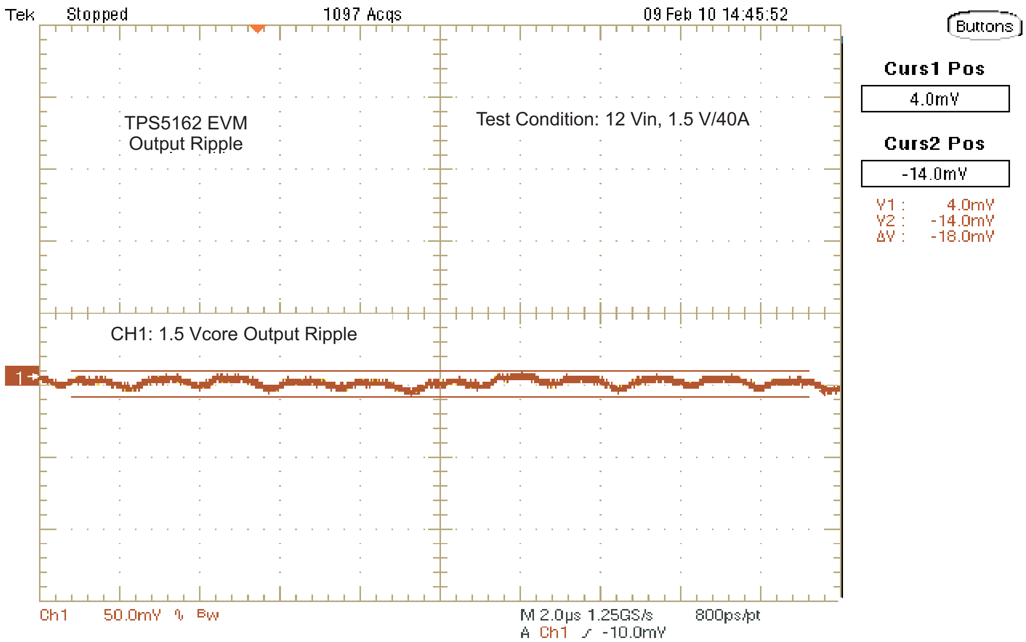


Figure 10. TPS51621EVM-602 Output Ripple

7.7 Switching Node at 40 A

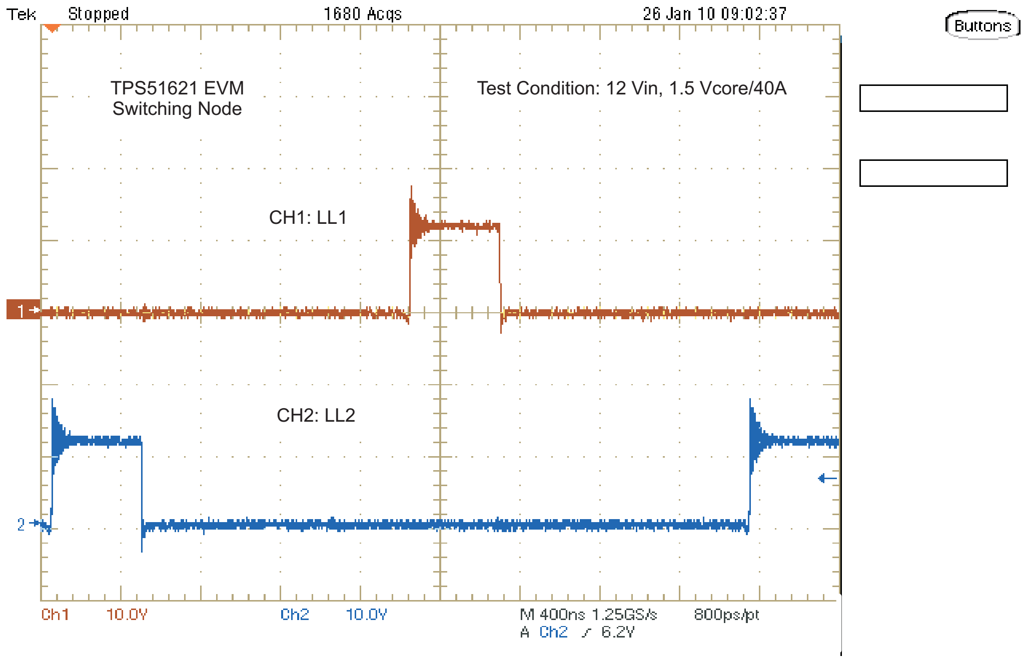


Figure 11. TPS51621EVM-602 Switching Node at 40 A

7.8 Switching Node at 2 A

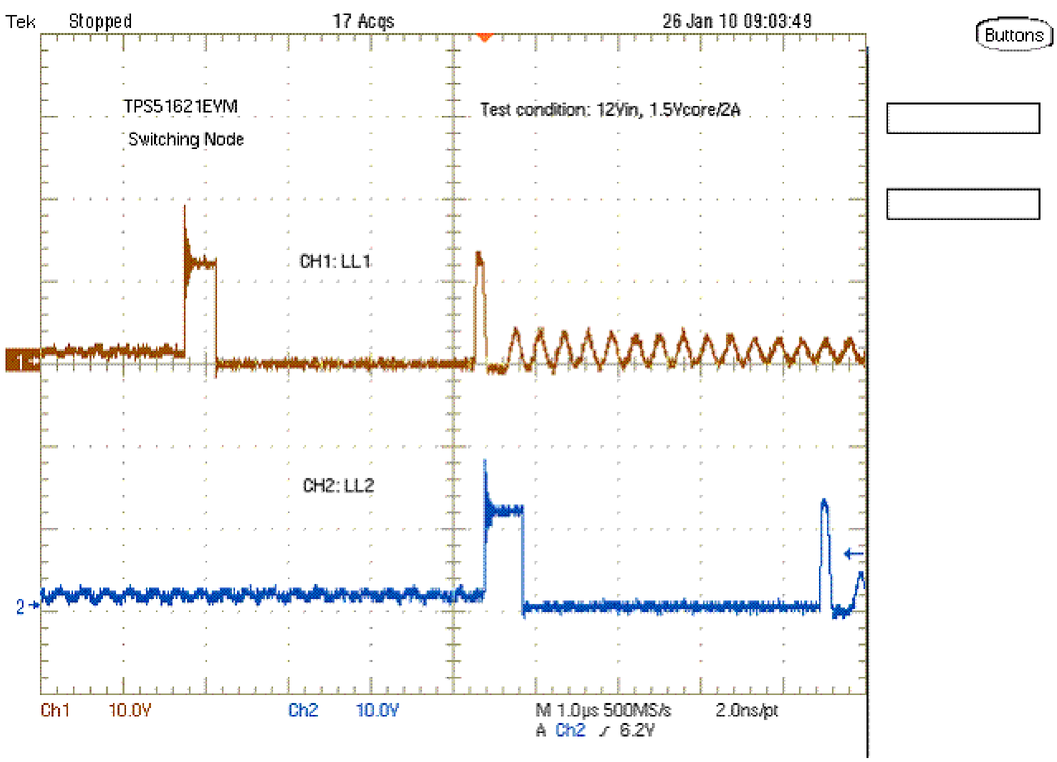


Figure 12. TPS51621EVM-602 Switching Node at 2 A

7.9 Output Transient

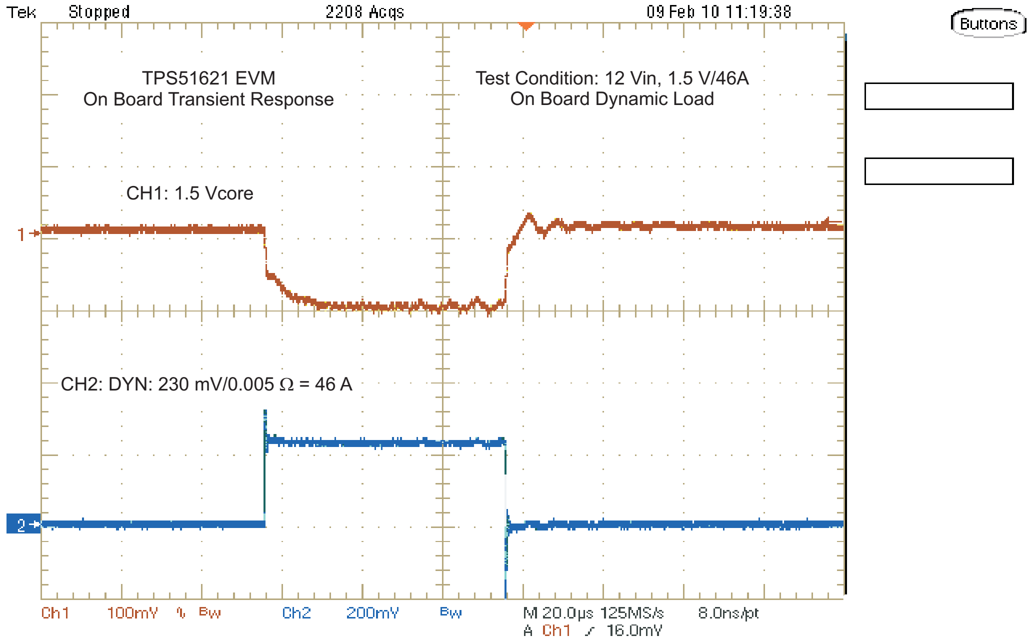


Figure 13. TPS51621EVM-602 Output Transient

7.10 Output Transient Overshoot Reduction OFF

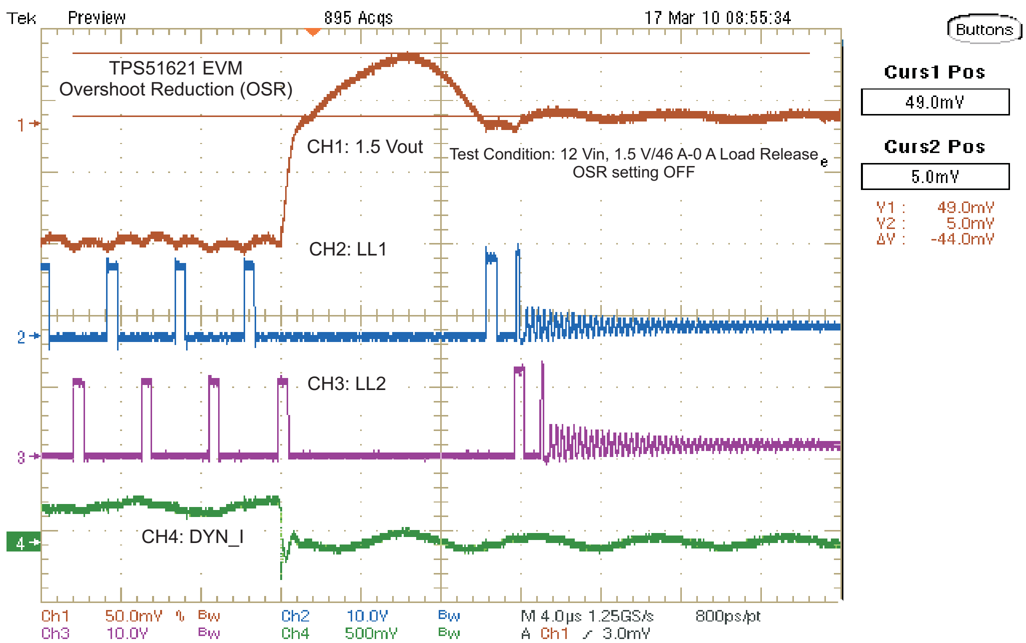


Figure 14. TPS51621EVM-602 Output Transient Release Without Overshoot Reduction

7.11 Output Transient Overshoot Reduction MAX

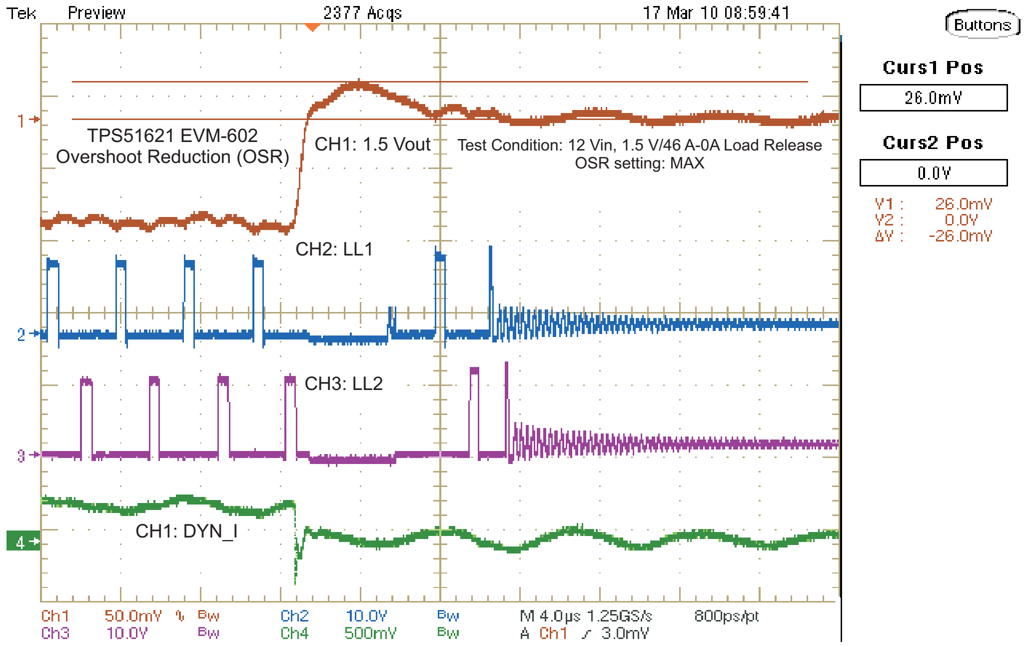
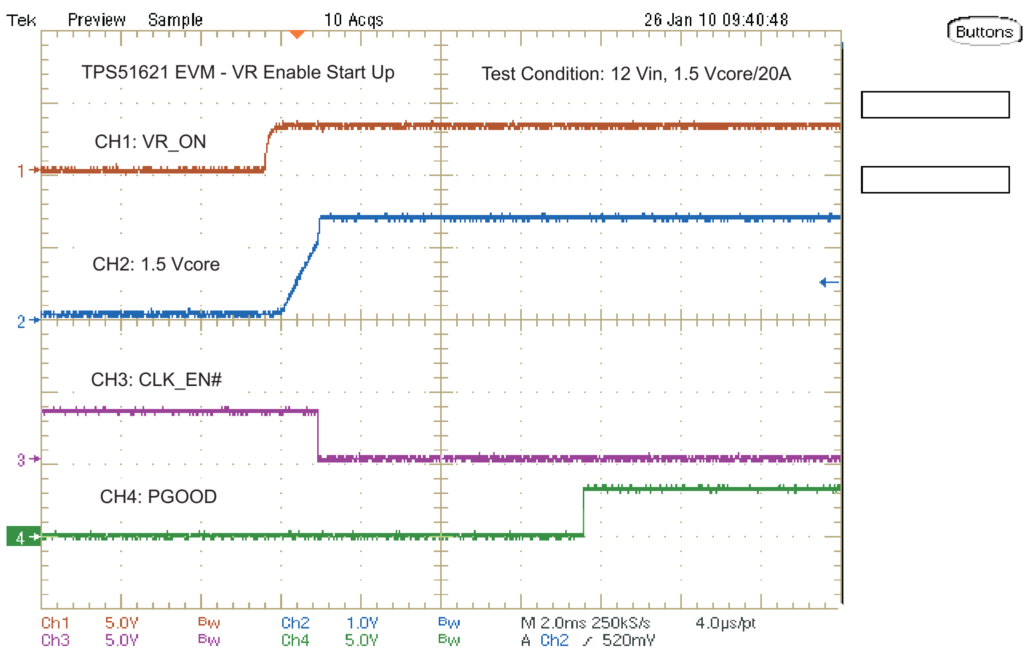


Figure 15. TPS51621EVM-602 Output Transient Release With Maximum Overshoot Reduction

7.12 Turn On Waveform



NOTE: Meets Intel IMVP6+ 1.2V VBOOT requirement

Figure 16. TPS51621EVM-602 Enable Turns On Waveform

7.13 Turn Off Waveform

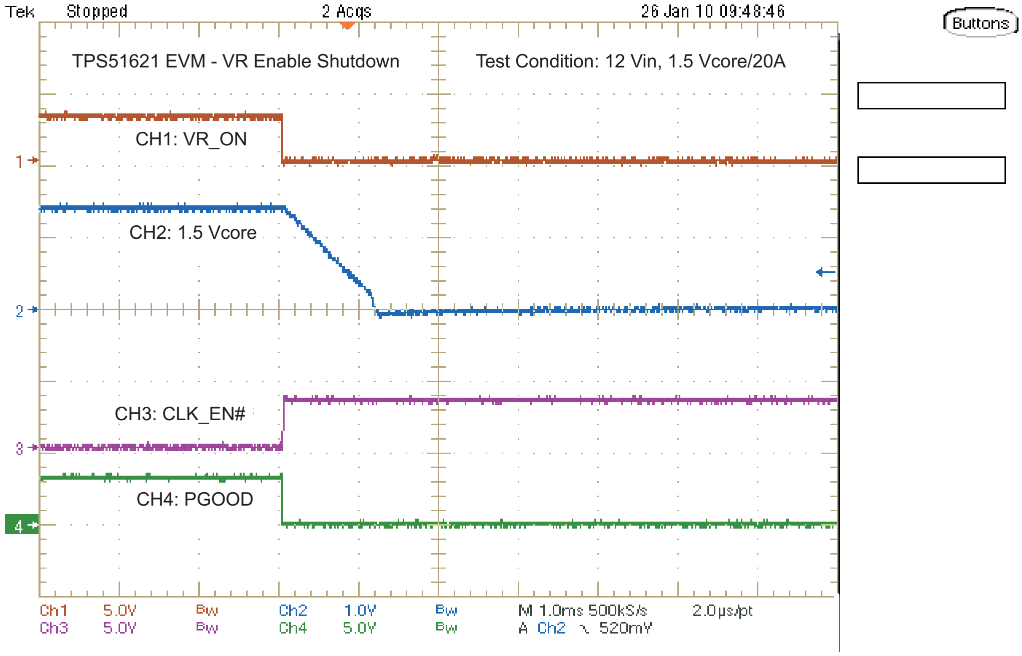


Figure 17. TPS51621EVM-602 Enable Turns Off Waveform

7.14 Bode Plot

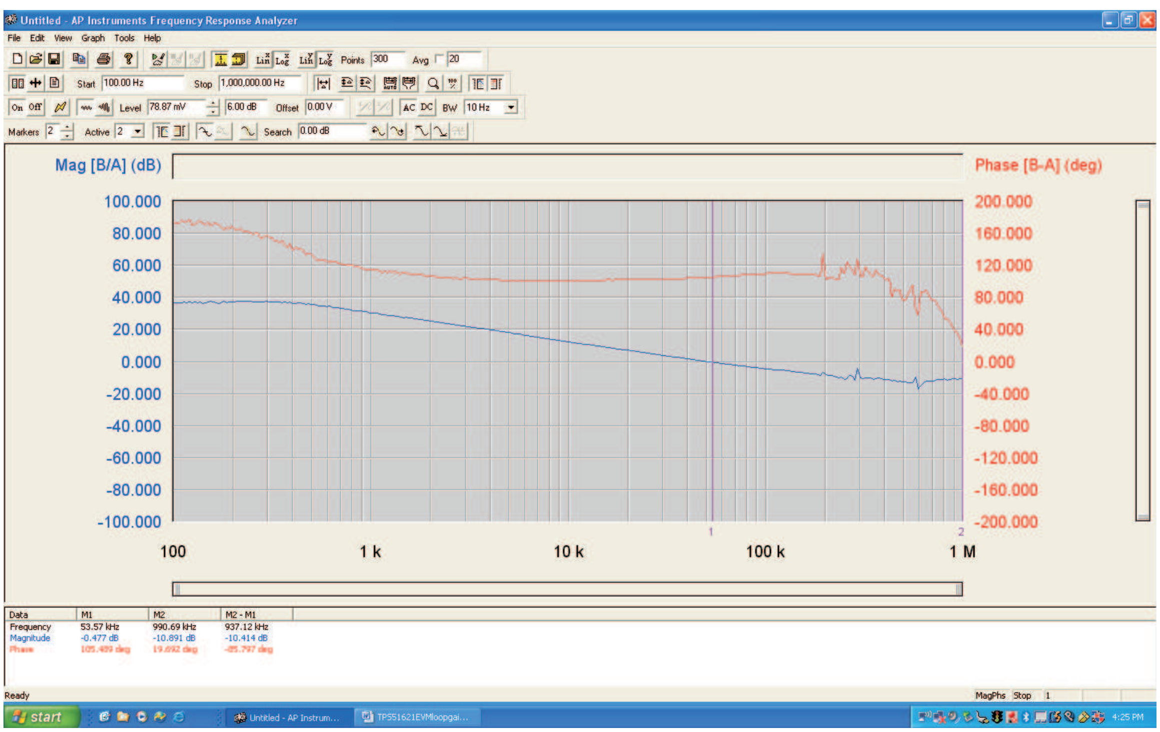


Figure 18. TPS51621EVM-602 Bode Plot, Test Condition: 12 Vin, 1.5 V/40 A

7.15 EVM Top Board Thermal Image

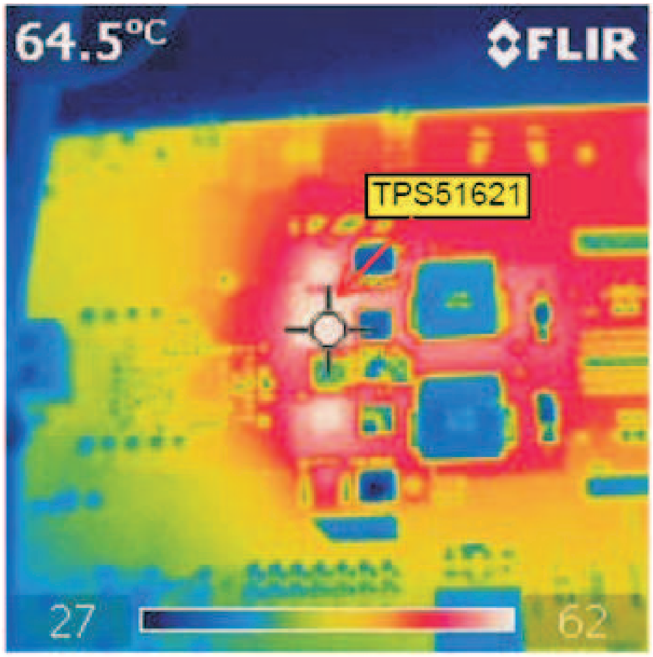


Figure 19. TPS51621EVM-602 Top Side Thermal Image, Test Condition: 12 Vin, 1.5 V/40 A

8 EVM Assembly Drawings and PCB Layout

The following figures (Figure 20 through Figure 25) show the design of the TPS51621EVM-602 printed-circuit board. The EVM has been designed using a 6-layers circuit board with 2-oz copper on outside layers.

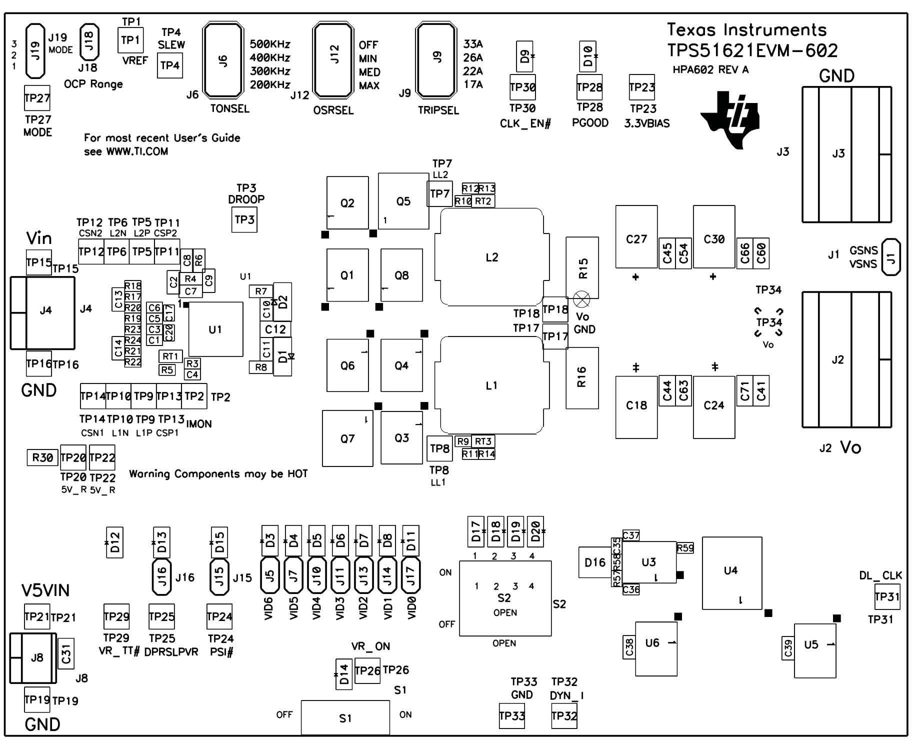


Figure 20. TPS51621EVM-602 Top Layer Assembly Drawing, Top View

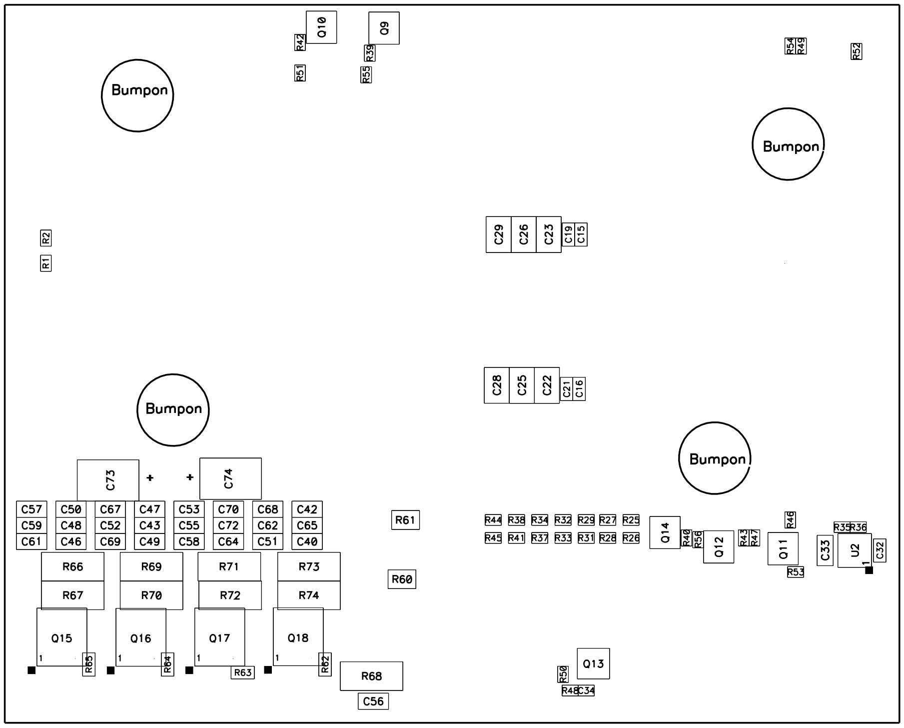


Figure 21. TPS51621EVM-602 Bottom Assembly Drawing, Bottom View

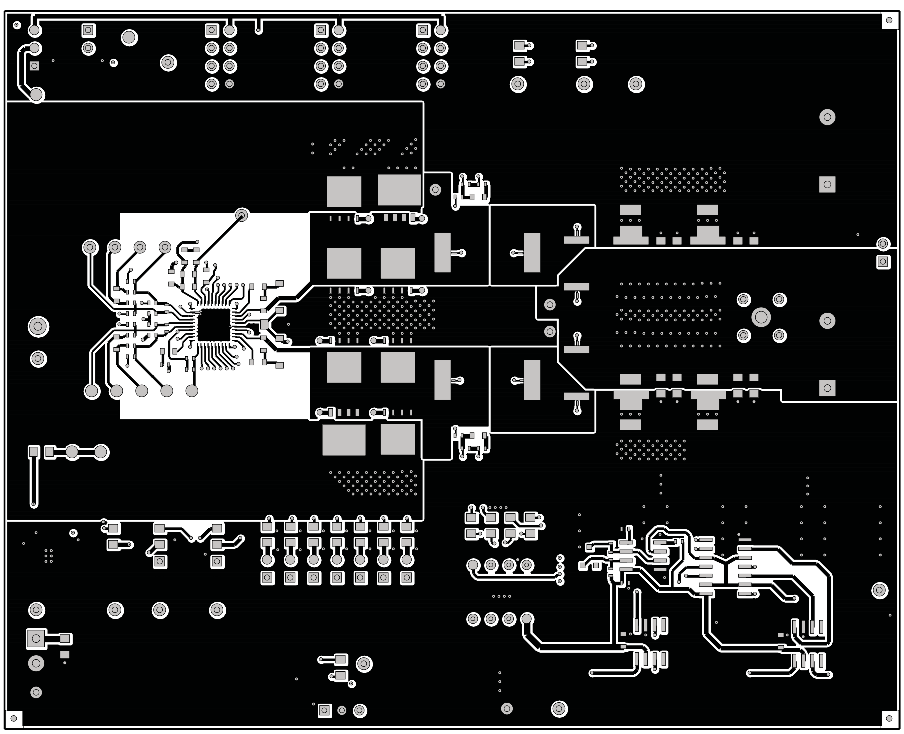


Figure 22. TPS51621EVM-602 Top Copper, Top View

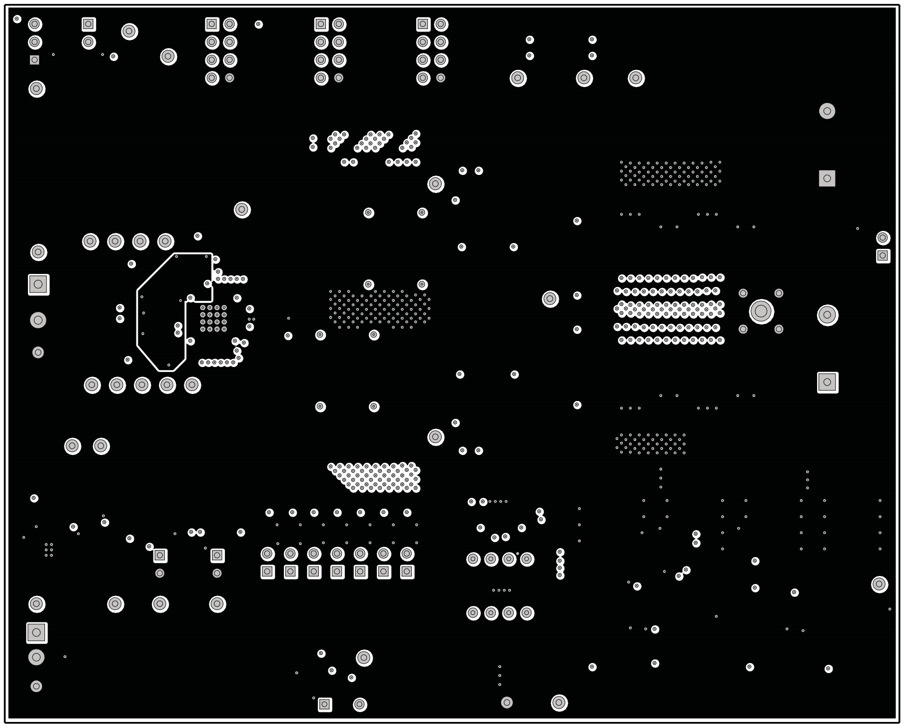


Figure 23. TPS51621EVM-602 Internal Layer 2, Top View

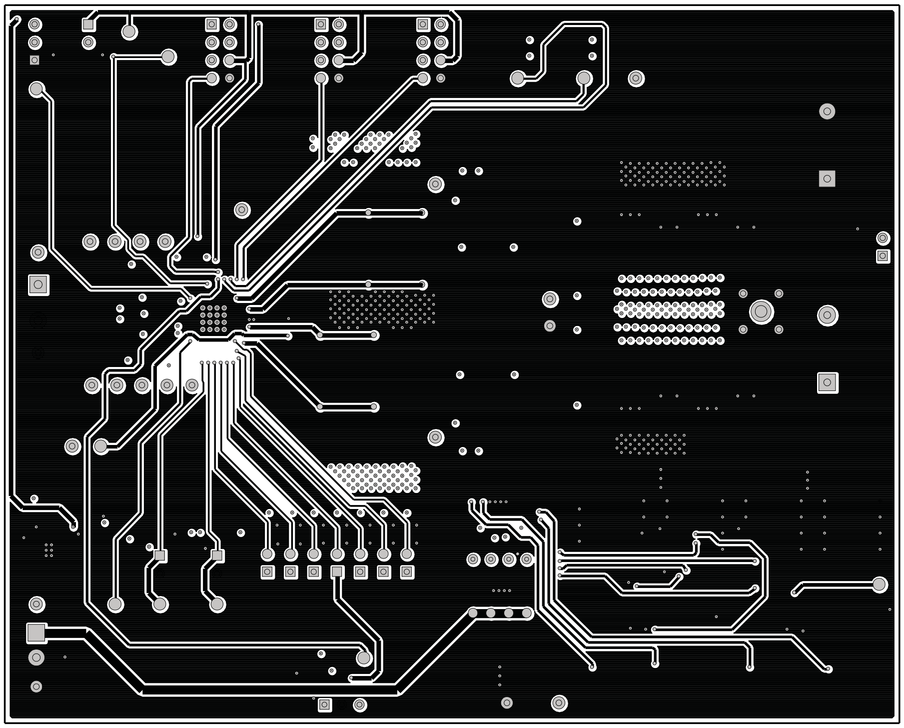


Figure 24. TPS51621EVM-602 Internal Layer 3, Top View

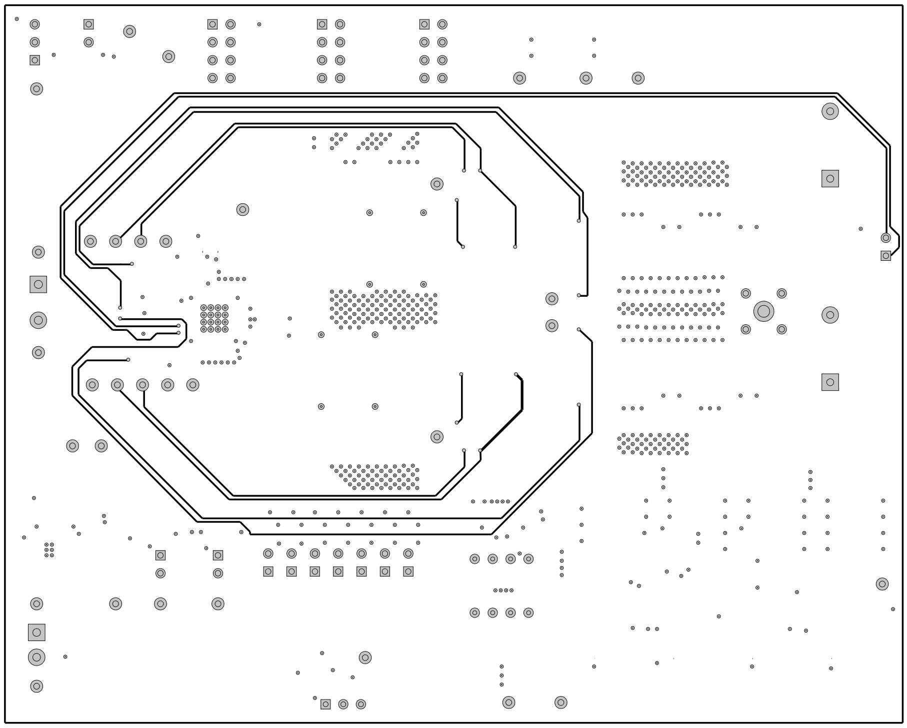


Figure 25. TPS51621EVM-602 Internal Layer 4, Top View

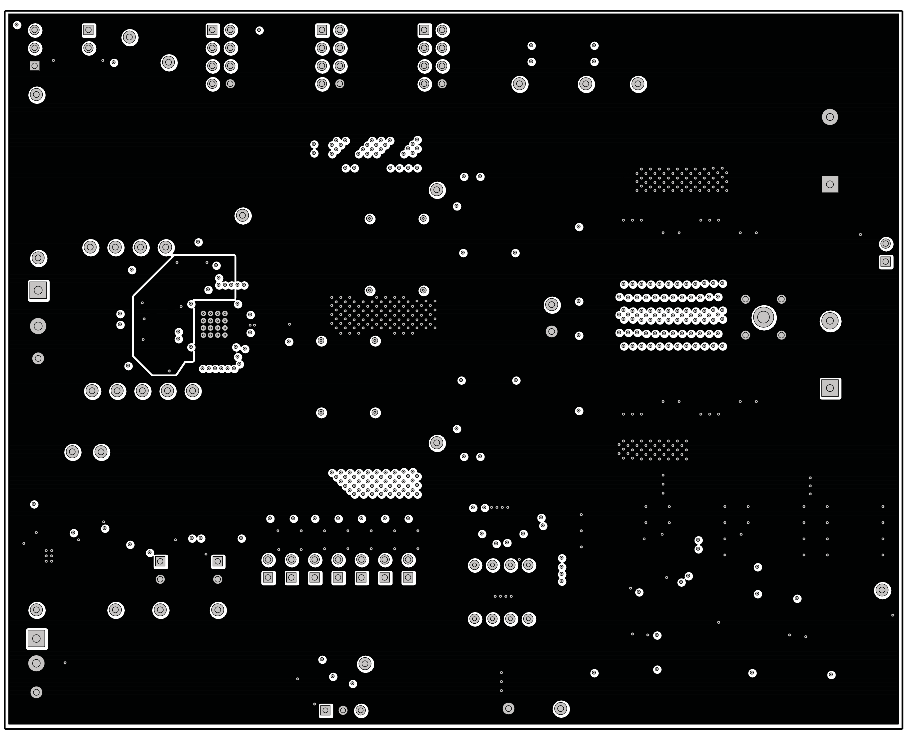


Figure 26. TPS51621EVM-602 Internal Layer 5, Top View

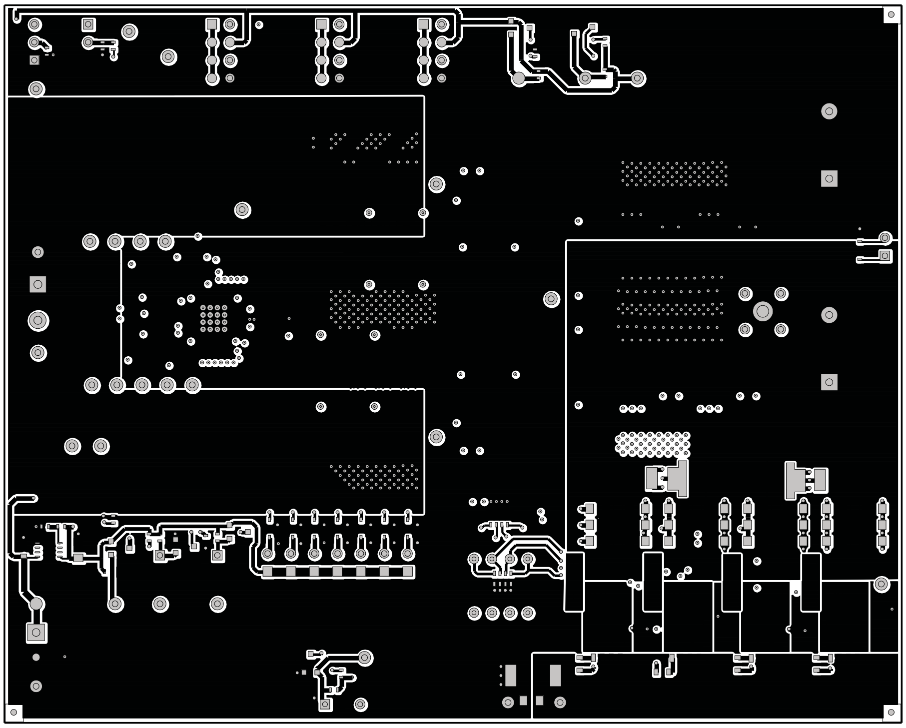


Figure 27. TPS51621EVM-602 Bottom Layer, Top View

9 Bill of Materials

Table 12. EVM Major Components List(1)

QTY	REFDES	Description	MFR	Part Number
4	C1, C3, C5, C6	Capacitor, Ceramic, 33 pF, 50V, C0G, 5%, 0402	STD	STD
4	C18, C24, C27, C30	Capacitor, Aluminum, 330 µF, 2.5V, 20%, 7 mΩ, 7343	Kemet	T520V337M2R5AT
36	C12, C31, C33, C40–C72	Capacitor, Ceramic, 10 µF, 6.3V, X5R, 20%, 0805	STD	STD
2	C13, C14	Capacitor, Ceramic, 0.027 µF, 50V, X7R, 10%, 0603	STD	STD
2	C15, C16	Capacitor, Ceramic, 1000 pF, 50V, X7R, 10%, 0603	STD	STD
6	C22, C23, C25, C26, C28, C29	Capacitor, Ceramic, 22 µF, 25V, X5R, 20%, 1210	STD	STD
1	C2	Capacitor, Ceramic, 0.22 µF, 25V, X7R, 20%, 0603	STD	STD
2	C34, C35	Capacitor, Ceramic, 0.01 µF, 25V, X5R, 20%, 0402	STD	STD
2	C36, C37	Capacitor, Ceramic, 0.1 µF, 16V, X7R, 20%, 0402	STD	STD
1	C4	Capacitor, Ceramic, 3300 pF, 25V, X7R, 10%, 0402	STD	STD
1	C7	Capacitor, Ceramic, 33 pF, 50V, C0G, 10%, 0603	STD	STD
8	C9–C11,C19, C21, C32, C38, C39	Capacitor, Ceramic, 1 µF, 16V, X7R, 20%, 0603	STD	STD
2	D1, D2	Diode, Schottky, 0.5A, 30V, SOD-123	On Semi	MBR0530T1G
2	L1, L2	,Inductor, SMT 0.47 µH, 32A, 1.1 mΩ, 0.51" × 0.51"	Vishay	IHLP5050FDERR47M01
2	Q1, Q6	MOSFET, N-ch, 25V, 31A, 2.1 mΩ, TDSON 5 × 6mm	TI	CSD16321Q5
2	Q2, Q7	MOSFET, N-ch, 25V, 21A, 4.6 mΩ, TDSON 5 × 6mm	TI	CSD16322Q5
4	Q15–Q18	MOSFET, N-ch, 25V, 31A, 2.5 mΩ, TDSON5X6mm	TI	CSD16407Q5
2	R1, R2	Resistor, Chip, 10, 1/16W, 1%, 0402	STD	STD

(1) Major Components List according to the schematic shown in Figure 1, Figure 2, and Figure 3.

Table 12. EVM Major Components List[(1)] (continued)

QTY	REFDES	Description	MFR	Part Number
2	R11, R12	Resistor, Chip, 121K, 1/16W, 1%, 0402	STD	STD
2	R13, R14	Resistor, Chip, 43.2K, 1/16W, 1%, 0402	STD	STD
2	R15, R16	Resistor, Chip, 0.001, 1W, 1%, 2512, Current sense	Vishay	WSL25121L000FEA
4	R17, R20, R21, R24	Resistor, Chip, 470, 1/16W, 1%, 0402	STD	STD
1	R3	Resistor, Chip, 16.9K, 1/16W, 1%, 0402	STD	STD
1	R30	Resistor, Chip, 1, 1/8W, 1%, 0805	STD	STD
1	R35	Resistor, Chip, 174K, 1/16W, 1%, 0402	STD	STD
2	R36, R58	Resistor, Chip, 100K, 1/16W, 1%, 0402	STD	STD
1	R4	Resistor, Chip, 4.75K, 1/10W, 1%, 0603	STD	STD
1	R49	Resistor, Chip, 90.9K, 1/16W, 1%, 0402	STD	STD
1	R5	Resistor, Chip, 2.00K, 1/16W, 1%, 0402	STD	STD
1	R54	Resistor, Chip, 162K, 1/16W, 1%, 0402	STD	STD
2	R7, R8	Resistor, Chip, 6.81, 1/10W, 1%, 0603	STD	STD
2	R9, R10	Resistor, Chip, 24.9K, 1/16W, 1%, 0402	STD	STD
3	RT1–RT3	NTC, Chip, Thermistor, 150K, 5%, 0603	Panasonic	ERT-J1VV154J
1	U1	IC, Dual-phase, D-CAP+, IMVP-6.5Vcore Controller, QFN-40	TI	TPS51621RHA
1	U2	IC, High input voltage, Micropower, 3.2uA at 80mA,QFN-8	TI	TPS715A01DRBR
1	U3	IC, Timer, Low-power CMOS, SO-8	TI	TLC555CD
1	U4	IC, Quadruple 2 input positive And gates	TI	SN74HC08D
2	U5, U6	IC, Dual 4A high speed low side MOSFET driver, MSOP-8	TI	UCC37324DGN

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of 0.3 V to 1.5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70° C. The EVM is designed to operate properly with certain components above 70° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265