User's Guide

SLVU416–December 2010

TPS70728EVM-612

This user's guide describes operational use of the TLV70728EVM-612 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TLV70728, low dropout (LDO) linear regulator. Included in this user's guide are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

Contents

List of Figures

List of Tables

1 Introduction

The Texas Instruments TLV70728EVM-612 evaluation module helps design engineers to evaluate the operation and performance of the TLV707xx family of linear regulators for possible use in their own circuit application. This particular EVM configuration contains a single linear regulator with internal thermal and current limit shutdowns, and enable (disable) circuitry in an extremely small, 1-mm × 1-mm, package. The regulator, including external components, is capable of delivering up to 150 mA to the load depending on the input-output power dissipation across the part. The TLV707xx does not require an input capacitor, and the output capacitor only need be 0.47 µF (effective minimum) for stability; however, for conservative design practice accounting for widely varying noise environments, and dynamic line/load conditions, a 1-µF capacitor has been used at the input and output ports.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TLV70728EVM.

2.1 Input/Output Connectors and Jumper Descriptions

- **J1 – VIN** – Input power supply voltage connector.
  Twist the positive input lead and ground return lead from the input power supply and keep them as short as possible to minimize EMI transmission. Add additional bulk capacitance between J1 and J2 if the supply leads are greater than six inches. For example, an additional 47-µF electrolytic capacitor connected from J1 to ground can improve the transient response of the TLV70728 while eliminating unwanted ringing on the input due to long wire connections.
- **J2 – GND** – Ground-return connector for the input power supply.
- **J3 – OUT** – Regulated output voltage connector.
- **J4 – GND** – Output ground-return connector.
- **JP1–EN** – Output enable. To enable the output, connect a jumper to short the VIN pin 1 to the EN center pin 2. To disable the output, connect a jumper to short EN pin 2 to GND pin 3.

2.2 Soldering Guidelines

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit (IC) especially.

2.3 Equipment Interconnect

- Turn off the input power supply after verifying that its output voltage is set to less than 5.5 V. Connect the positive voltage lead from input power supply to VIN, at the J1 connector of the EVM. Connect the ground lead from the input power supply to GND at the J2 connector of the EVM.
- Connect a 0-mA to 150-mA load between the output, OUT, at connector J3, and ground, GND, at connector J4.
- Disable the output by jumpering JP1, the EN pin to the GND pin.

3 Operation

- Turn on the input power supply. For initial operation, it is recommended that the input power supply, VIN – J1, be set to 3.8 V
- Enable the output by reconnecting the jumper on JP1 from the EN pin to the VIN pin.
- Vary the respective loads and VIN voltages as necessary for test purposes.

4 Test Results

This section provides typical performance waveforms for the TLV70728EVM-612 printed-circuit board (PCB).

4.1 Turnon Sequence

Figure 1 shows the turnon/off characteristic where VIN is preset to 3 V, the output drives full load, and the EN turnon is stepped to 3 V (C4, green). The output soft start (C3, blue) shows a monotonic rise time of approximately 50µs after a built in delay of approximately 70µs. The input rush current (C2, red) follows the output voltage ramp. The output voltage startup ramp is not load dependant.

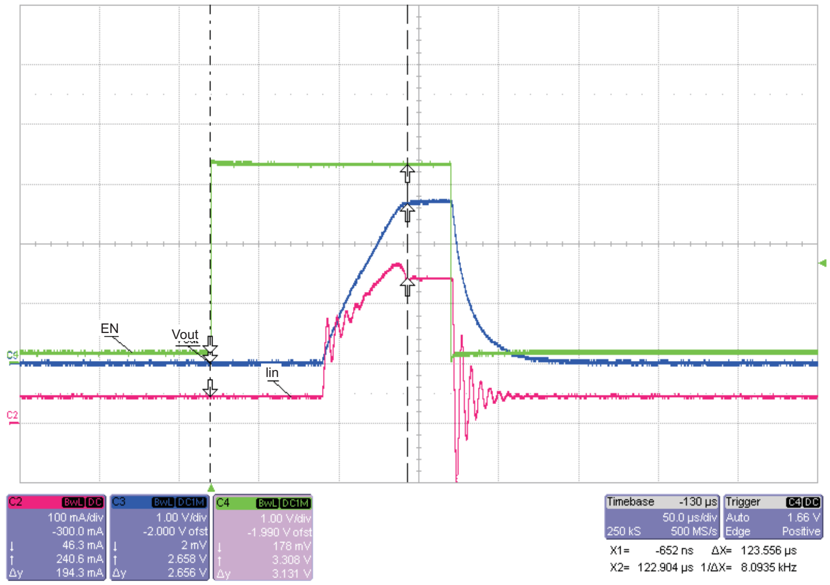


Figure 1. Turnon Sequence: C4 EN – Turnon to 3 V, C3 OUT – 2.8-V Turnon Ramp, C2 – Input Rush Current at Turnon

4.2 Output Load Transient

Figure 2 shows the load transient response – oscilloscope C3 – for a full-load step transient. The load current, transient step is shown on oscilloscope C2.

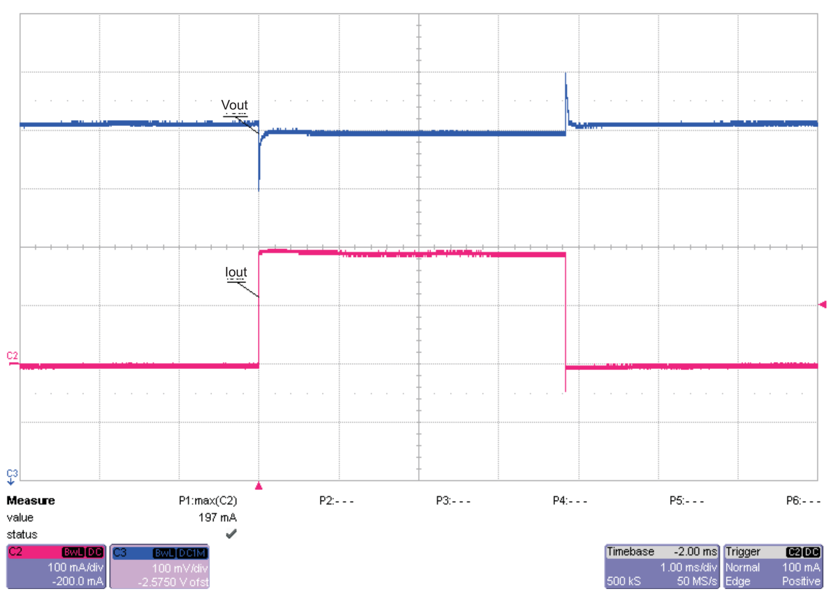


Figure 2. Step Load and Transient Response: C2 – Full Load Step Current Transient, C3 OUT – Output Voltage Transient Response

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$$T_j = T_a + Pd \times \theta_{ja}$$

where T_j is the junction temperature, T_a is the ambient temperature, P_d is the power dissipation in the device (Watts), and θ_{ja} is the thermal resistance from junction to ambient. All temperatures are in degrees Celcius. The maximum silicon junction temperature, T_j, must not be allowed to exceed 150°C. The layout design must use copper trace and plane areas effectively as thermal sinks, in order not to allow T_j to exceed the absolute maximum rating under all temperature conditions and voltage conditions across the part.

The designer must consider the layout carefully so that the thermal design of the PCB achieves optimal performance over temperature. For this EVM, Figure 5 shows that the DQN package footprint uses a thermal pad to further cool the part. The thermal pad contains a single, 6-mil thermal via connection to the bottom-side copper ground plane as well as a direct connection to the top-side surface copper over the ground pad/pin for the IC. The PCB is a two-layer board with 2 ounces of copper on top and bottom layers. The DQN package drawing can be found at the Texas Instruments Web site in the product folder for the TPS707 LDO.

Table 1 repeats information from the Dissipation Ratings Table of the TPS707 (SLVS718) data sheet for comparison with the thermal resistance, θ_{ja}, calculated for this EVM layout to show the wide variation in thermal resistances for given copper areas. The high-K value is determined using a standard JEDEC high-k (2s2p) board having dimensions of 3 inch × 3 inch with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

Table 1. EVM Thermal Resistance, θ_{ja} , and Maximum Power Dissipation

Board	Package	θ_{ja}	Max. Dissipation Without Derating (T_A = 25°C)	Max. Dissipation Without Derating (T_A = 70°C)
High-K	DQN	206°C/W	485 mW	269 mW
TPS70728EVM-612	DQN	88°C/W	1.136 W	625 mW

The thermal resistance for the TPS70728EVM-612, θ_{ja}, is the measured value for this particular layout scheme. The maximum power dissipation is proportional to the volume of copper volume connected to the package.

6 Board Layout

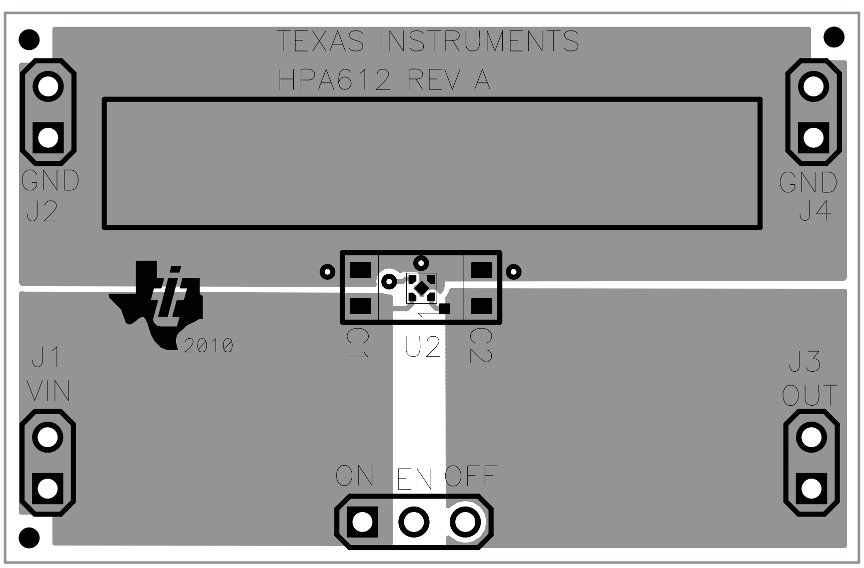


Figure 3. Assembly Layer

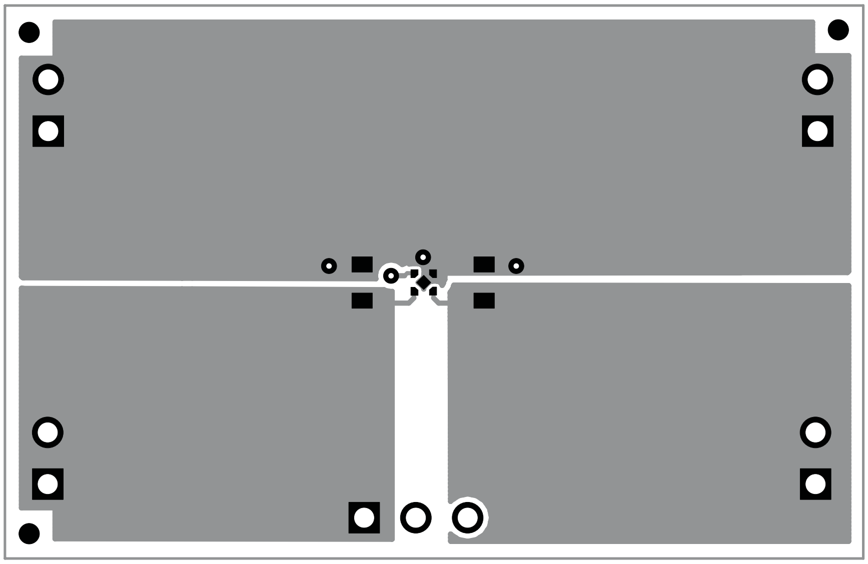


Figure 4. Top Layer Routing

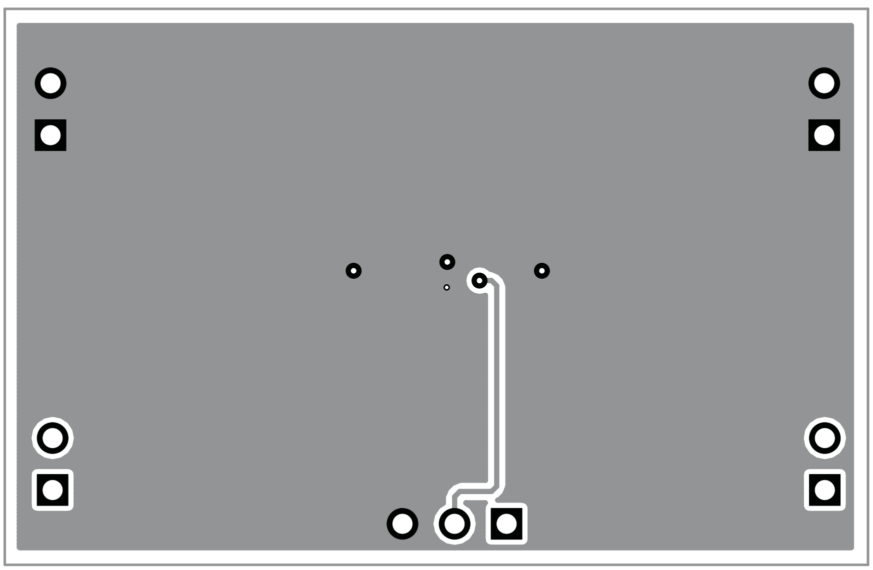
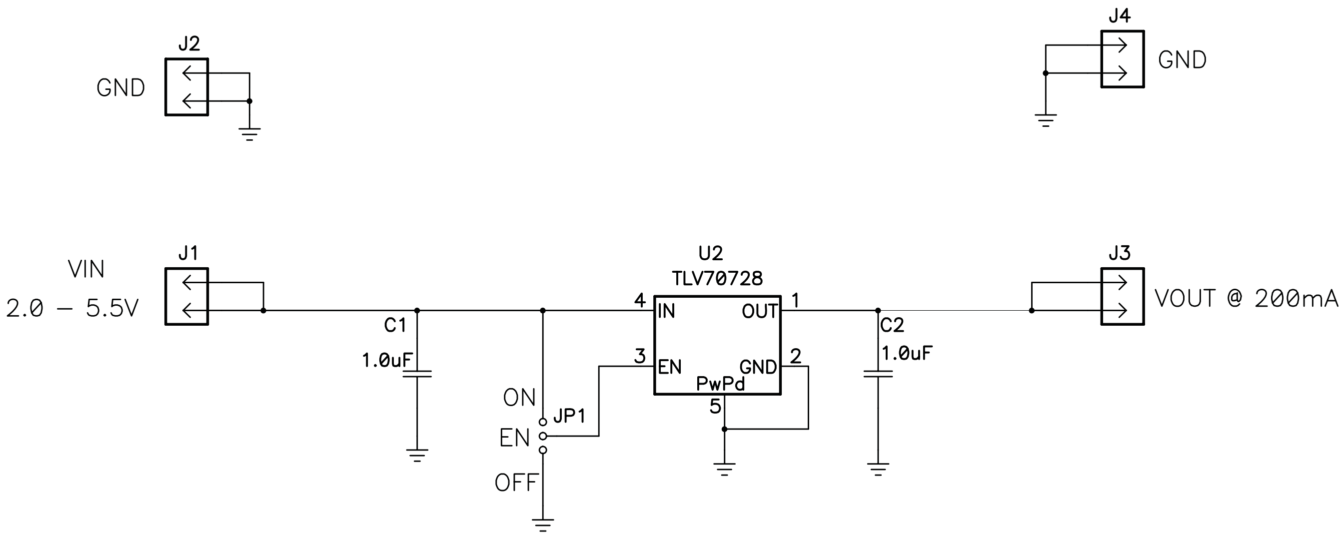


Figure 5. Bottom Layer Routing

7 Schematic and Bill of Materials

7.1 Schematic



ASSY	U1	VOUT
–001	TLV70728	2.8V

Figure 6. TLV70728EVM-612 Schematic

7.2 Bill of Materials

Table 2. TLV70728EVM-612 Bill of Materials

-001	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2	1.0 µF	Capacitor, Ceramic, Low Inductance, 6.3V, X7R, 10%	0603	Std	Murata
4	J1, J2, J3, J4	PEC02SAAN	Header, 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	JP1	PEC03SAAN	Header, 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	U2	TLV70728DQN	IC, 150mA, Low IQ, LDO Regulator	DQN	TLV70728DQN	TI
1			Label	1.25 x 0.25 inch	THT-13-457-10	Brady
1	–		Shunt, 100-mil, Black	0.100	929950-00	3M
1	–		PCB, 1.070 In x1.660 In x 0.062 In	–	PCB	Any

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2. Ref designators marked with an asterisk ('**') cannot be substituted.

4. All other components can be substituted with equivalent MFG's components.

5. Install label after final wash. Text shall be 8 pt font. Text shall be per Table 1 below.

Table 1	
Assembly number	Text
HPA612-001	TLV70728EVM-612

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2 V to 5.5 V and the output voltage range of 0.7 V to 3.6 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125° C. The EVM is designed to operate properly with certain components above 125° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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