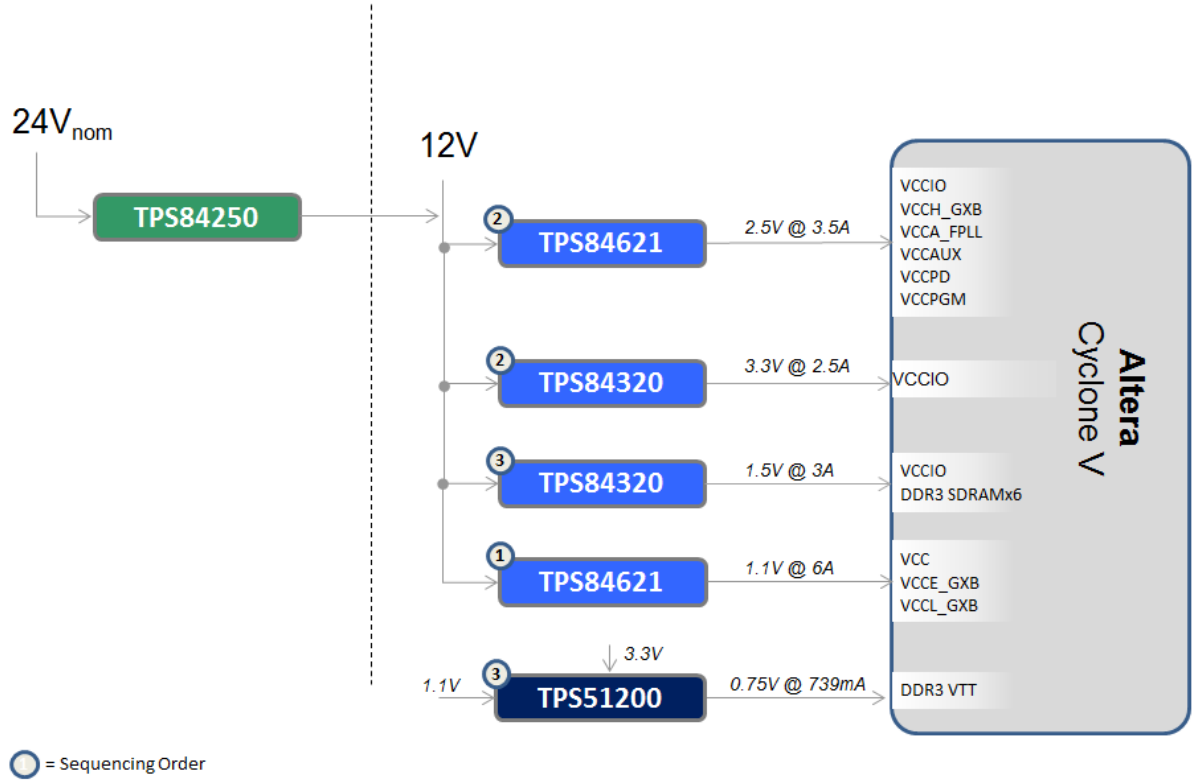
PMP8571 Test Results

1. Block Diagram



2. Startup/Sequencing

The startup waveform is shown in Figure 1. The input voltage is 12V, with no load at the output.

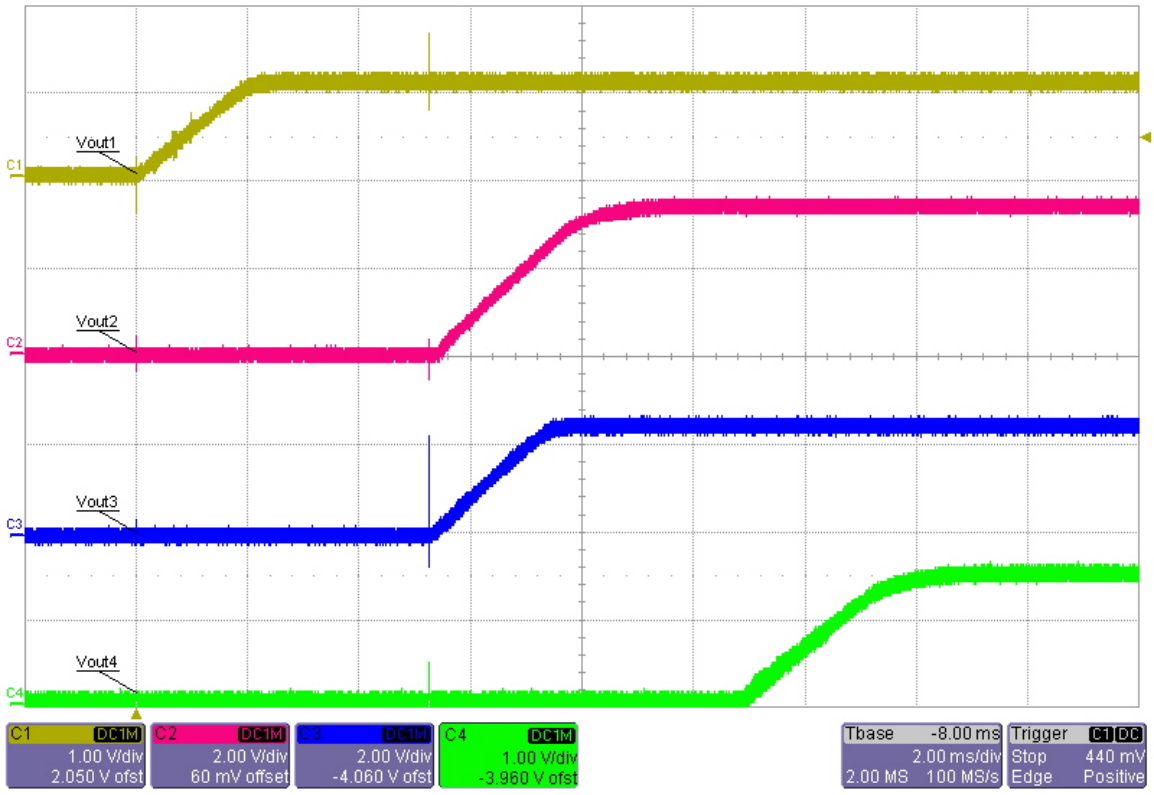


Figure 1

Ch1 => Output voltage 1.1V order #1
Ch2 => Output voltage 3.3V order #2
Ch3 => Output voltage 2.5V order #2
Ch4 => Output voltage 1.5V order #3

2ms/div
Full Bandwidth

3. Synchronization

The switching nodes of the buck stages are shown in Figure 2. The input voltage is 12V, with no load at the output.

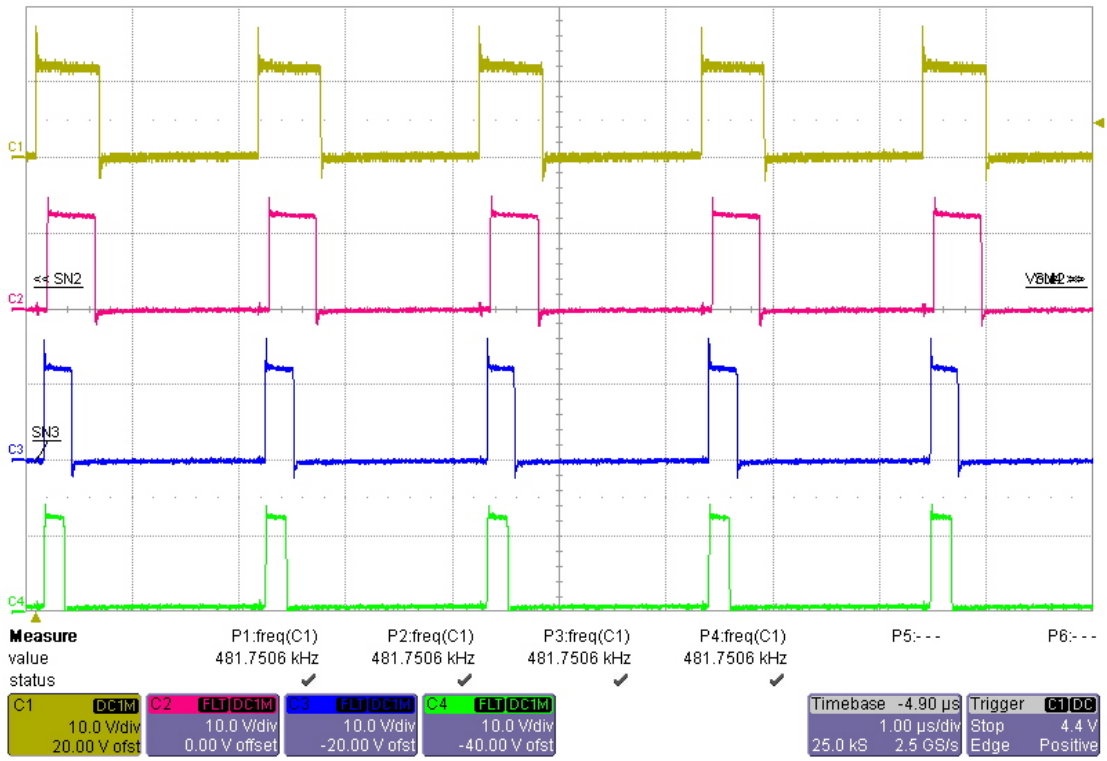


Figure 2

Ch1 => Switching node for 3.3 Vout
Ch2 => Switching node for 2.5 Vout
Ch3 => Switching node for 1.5 Vout
Ch4 => Switching node for 1.1 Vout

Common frequency: 481.75 kHz

1µs/div
Full Bandwidth

4. DDR Tracking

DDR tracking is shown in the Figures 3 and 4.

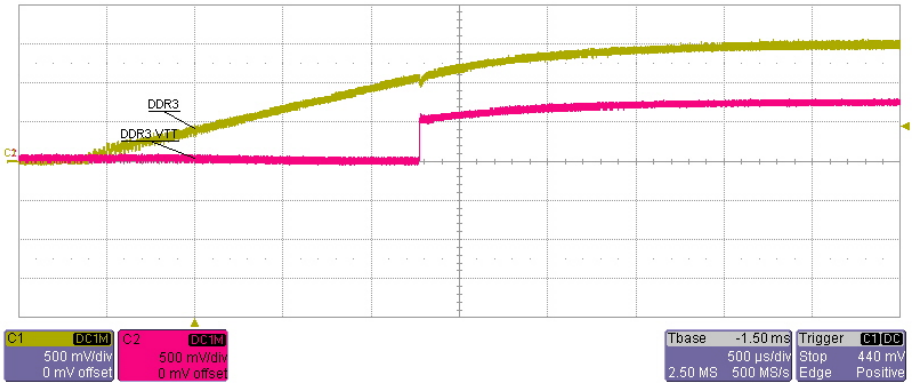


Figure 3

Ch1 => DDR3 1.5V output voltage from buck stage
Ch2 => DDR3 0.75V termination voltage from TPS51200
500µs/div
Full Bandwidth

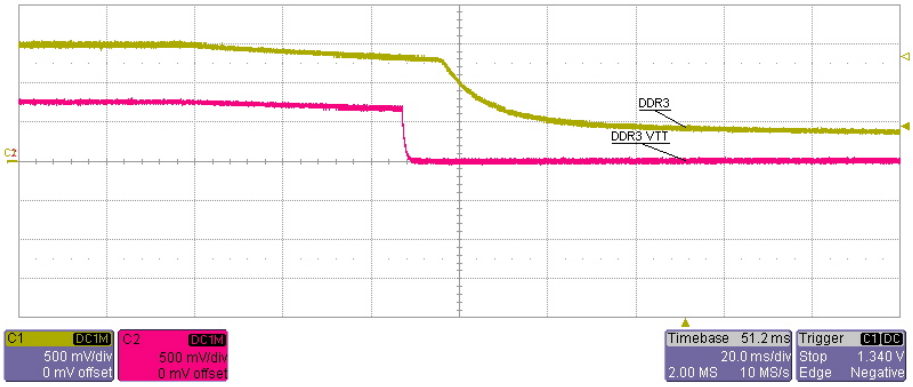


Figure 4

Ch1 => DDR3 1.5V output voltage from buck stage
Ch2 => DDR3 0.75V termination voltage from TPS51200
20ms/div
Full Bandwidth

5. Efficiency

The respective efficiencies of the buck stages providing 1.1V, 1.5V, 3.3V, and 2.5V are shown in Figures 5, 6, 7, and 8 below. The input voltage is 12V.

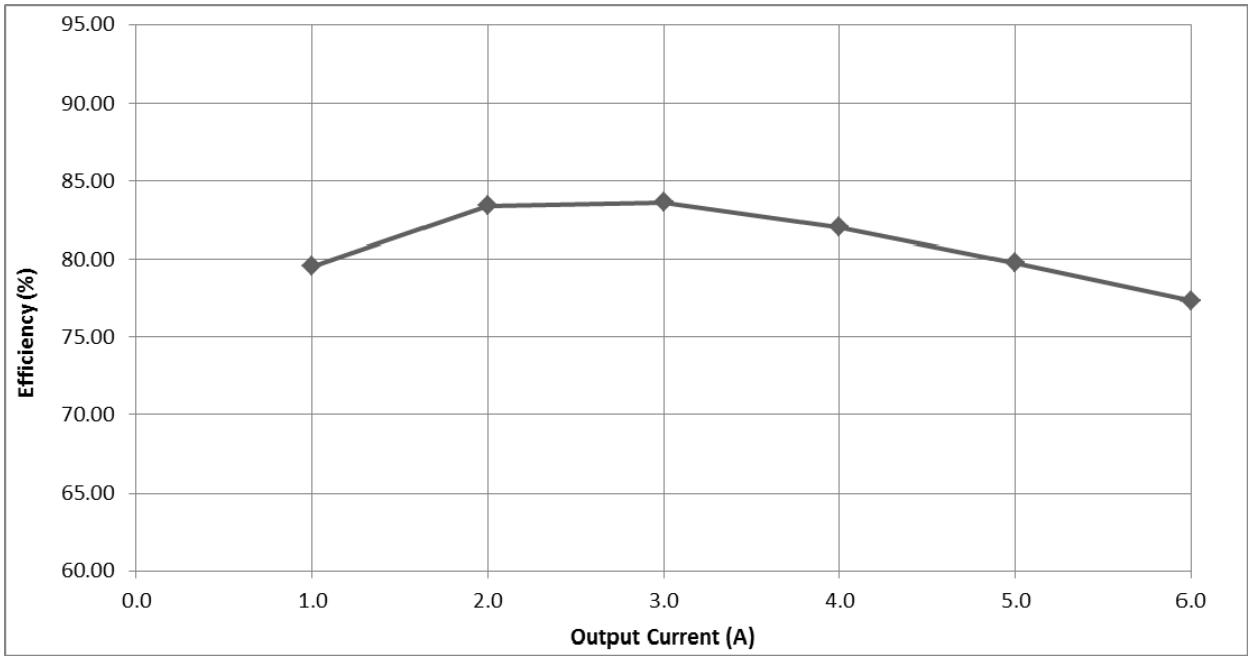


Figure 5: 1.1V Output

VIN (V)	IIN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	Eff (%)
11.91	0.12	1.09	1.0	1.370	1.090	79.58
11.88	0.22	1.09	2.0	2.614	2.180	83.41
11.85	0.33	1.09	3.0	3.911	3.270	83.62
11.81	0.45	1.09	4.0	5.315	4.360	82.04
11.78	0.58	1.09	5.0	6.832	5.450	79.77
11.74	0.72	1.09	6.0	8.453	6.540	77.37

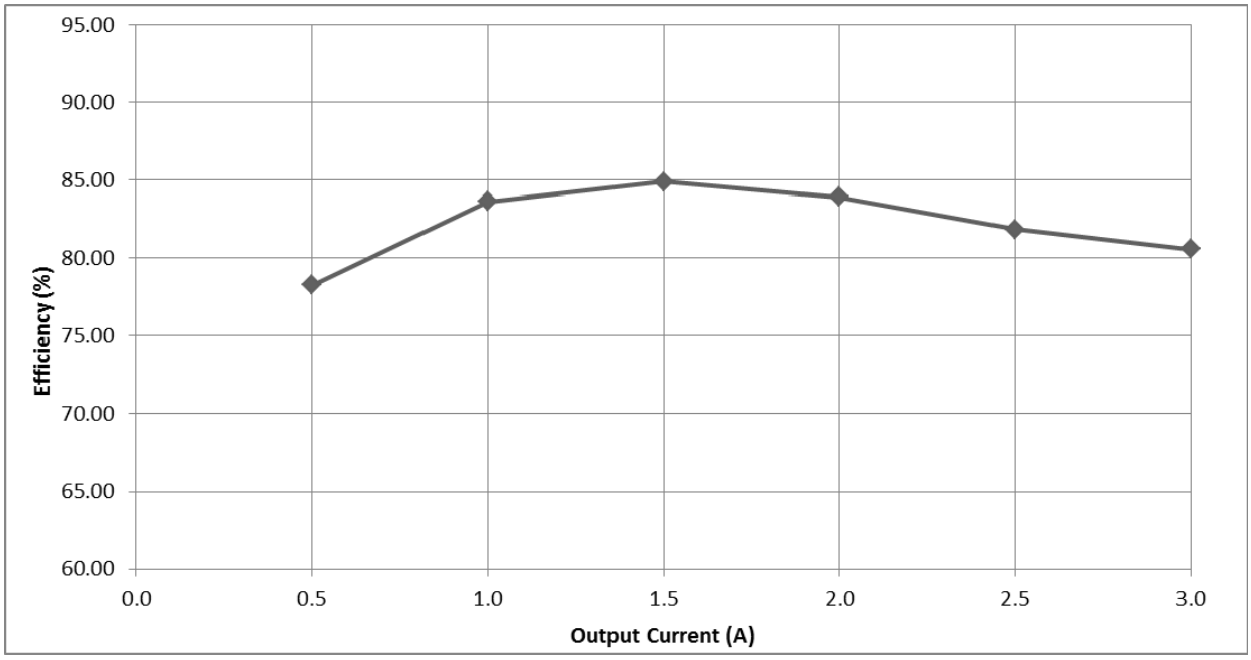


Figure 6: 1.5V Output

VIN (V)	IIN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	Eff (%)
11.98	0.08	1.50	0.5	0.958	0.750	78.26
11.96	0.15	1.50	1.0	1.794	1.500	83.61
11.94	0.22	1.50	1.5	2.651	2.250	84.88
11.92	0.30	1.50	2.0	3.576	3.000	83.89
11.90	0.39	1.50	2.5	4.582	3.750	81.85
11.88	0.47	1.50	3.0	5.584	4.500	80.59

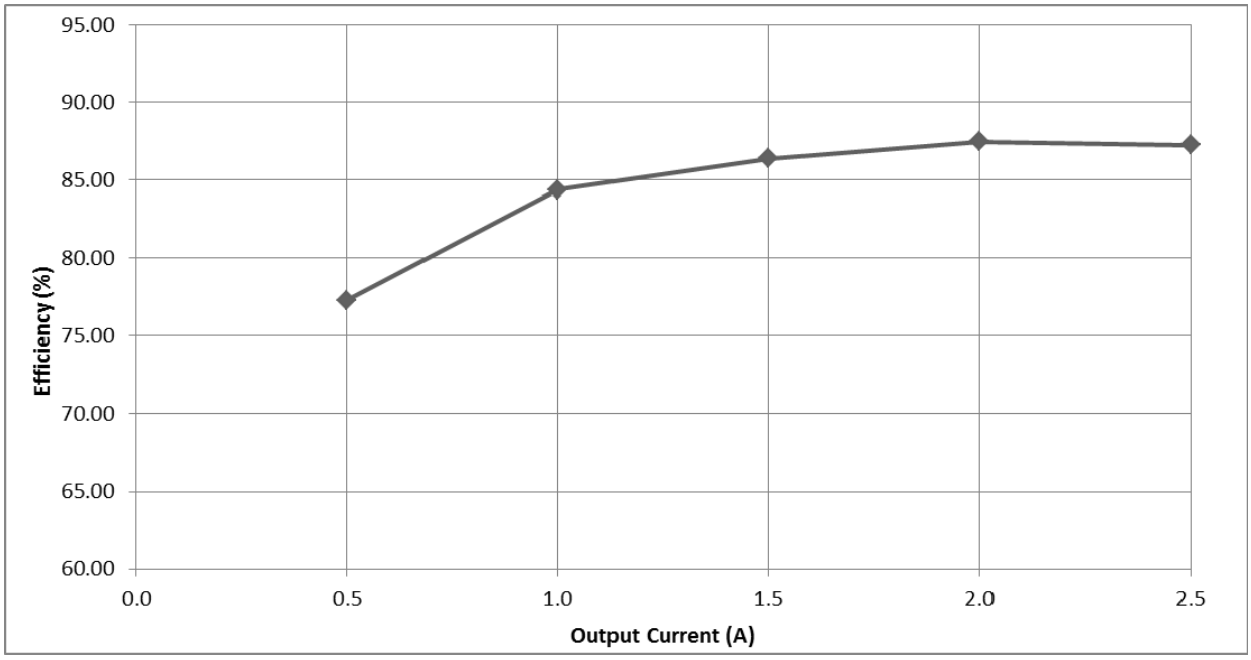


Figure 7: 3.3V Output

VIN (V)	IIN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	Eff (%)
11.89	0.19	3.40	0.5	2.200	1.700	77.29
11.85	0.34	3.40	1.0	4.029	3.400	84.39
11.81	0.50	3.40	1.5	5.905	5.100	86.37
11.78	0.66	3.40	2.0	7.775	6.800	87.46
11.74	0.83	3.40	2.5	9.744	8.500	87.23

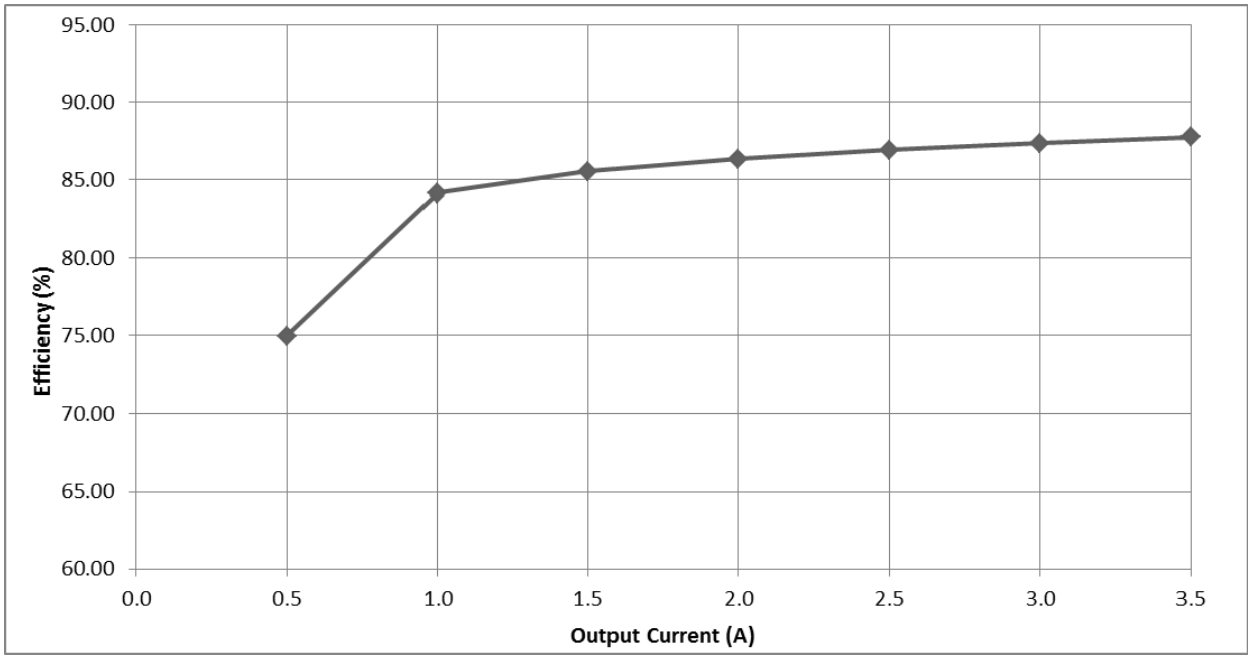
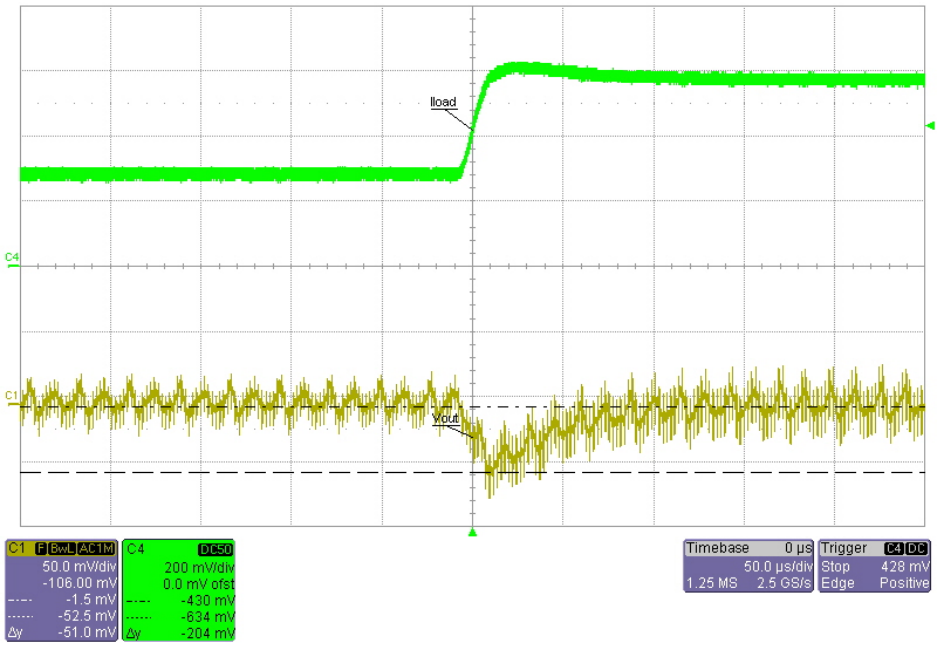


Figure 8: 2.5V Output

VIN (V)	IIN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	Eff (%)
11.91	0.14	2.50	0.5	1.667	1.250	74.97
11.88	0.25	2.50	1.0	2.970	2.500	84.18
11.85	0.37	2.50	1.5	4.385	3.750	85.53
11.82	0.49	2.50	2.0	5.792	5.000	86.33
11.79	0.61	2.50	2.5	7.192	6.250	86.90
11.76	0.73	2.50	3.0	8.585	7.500	87.36
11.73	0.85	2.50	3.5	9.971	8.750	87.76

6. Load Step

The load regulation of the 1.1V output is shown in Figures 9 and 10 below. The input voltage is 12V. The load step increases from 3A to 6A.

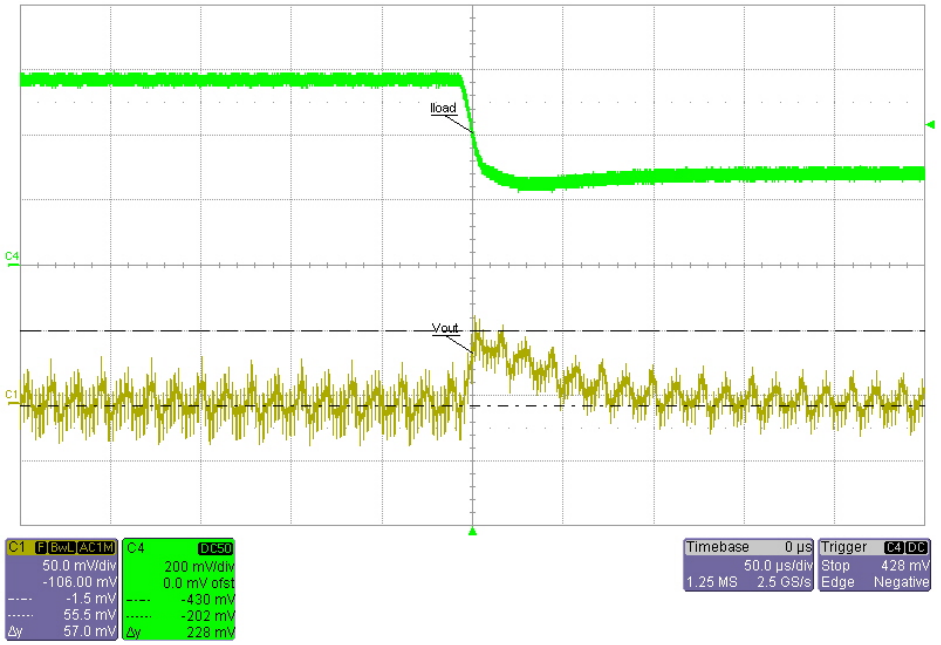


Ch1 => AC coupled output voltage

Ch2 => Output current 1V = 10A

Slope of step: 3A/16.6µs

Figure 9



Ch1 => AC coupled output voltage

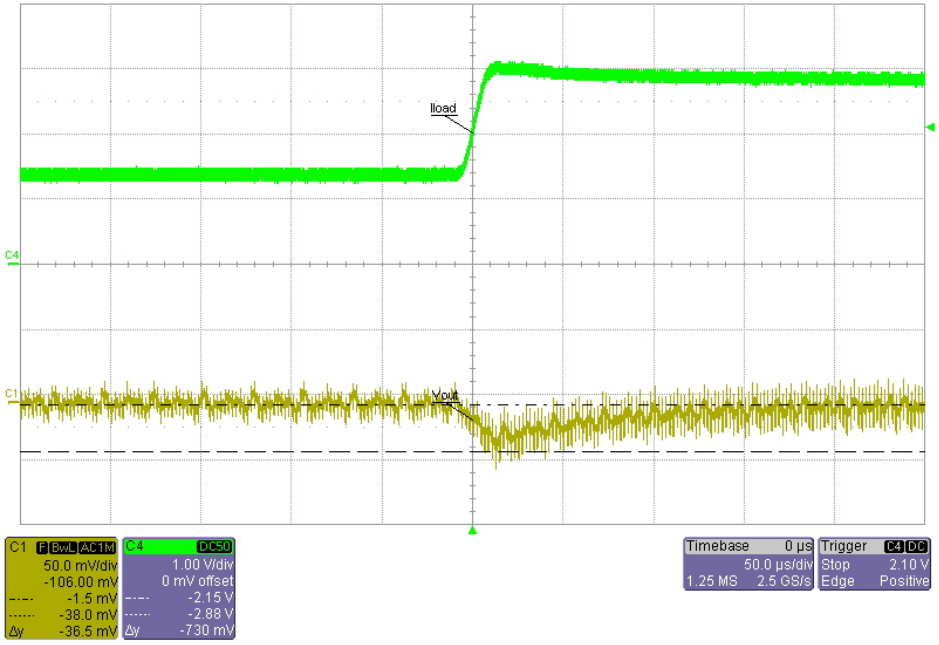
Ch2 => Output current 1V = 10A

Slope of step: 3A/11µs

Figure 10

The load regulation of the 1.5V output is shown in Figures 11 and 12 below. The input

voltage is 12V. The load step increases from 1.5A to 3A.

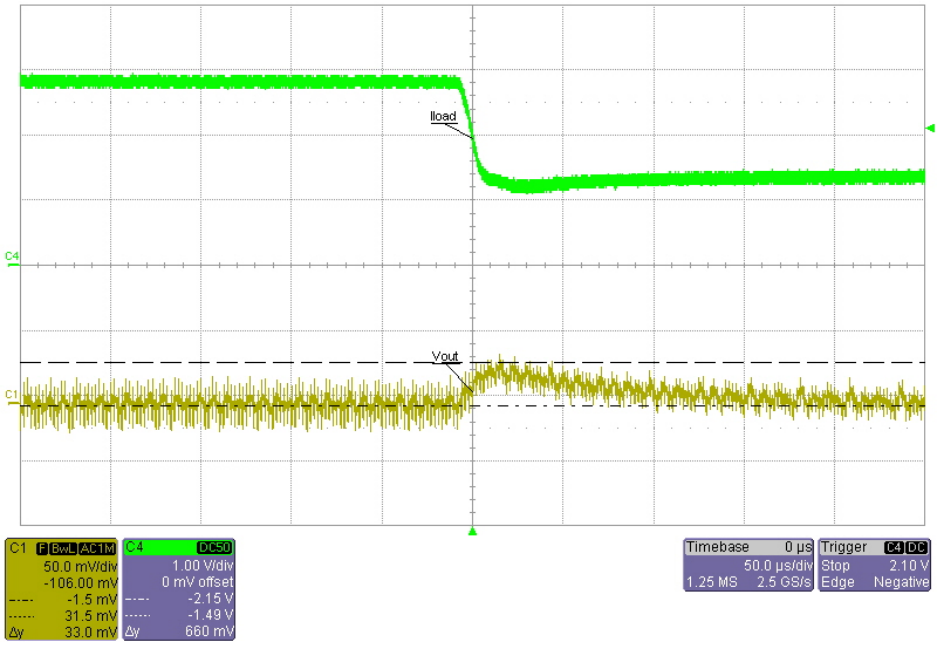


Ch1 => AC coupled output voltage

Ch2 => Output current 1V = 10A

Slope of step: 1.5A/16.3µs

Figure 11



Ch1 => AC coupled output voltage

Ch2 => Output current 1V = 10A

Slope of step: 1.5A/13.7µs

Figure 12

The load regulation of the 3.3V output is shown in Figures 13 and 14 below. The input voltage is 12V. The load step increases from 1.25A to 2.5A.

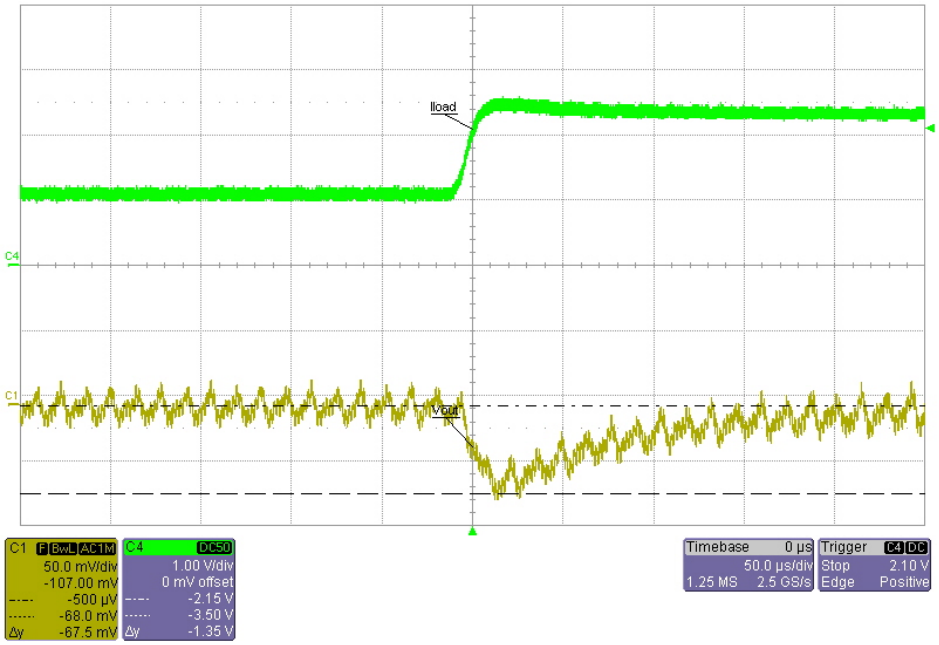


Figure 13

Ch1 => AC coupled output voltage

Ch2 => Output current
1V = 10A

Slope of step:
1.25A/17.1µs

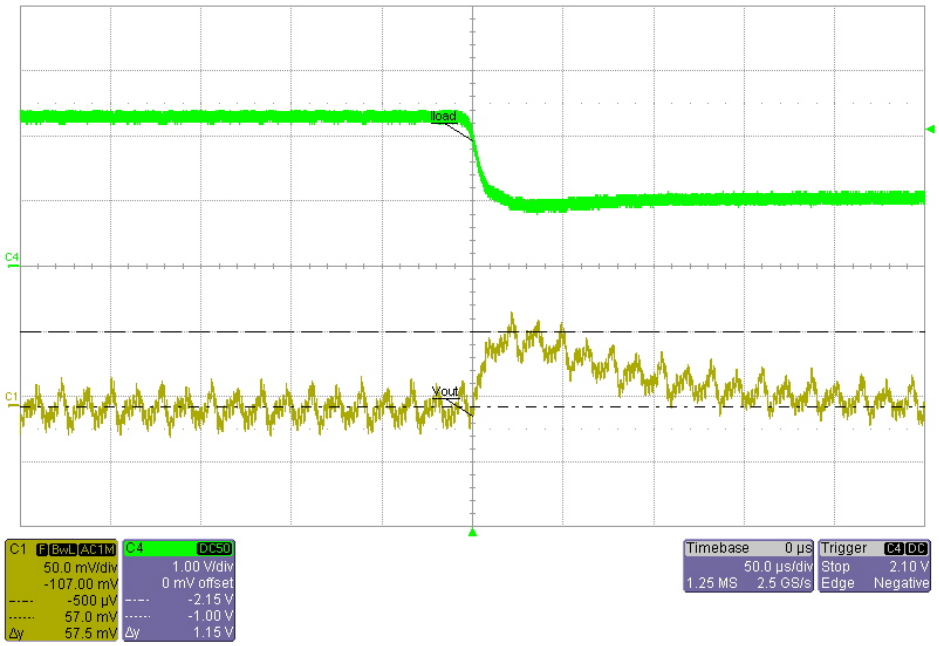


Figure 14

Ch1 => AC coupled output voltage

Ch2 => Output current
1V = 10A

Slope of step:
1.25A/13.3µs

The load regulation of the 2.5V output is shown in the Figures 15 and 16 below. The input voltage is 12V. The load step increases from 1.75A to 3.5A.

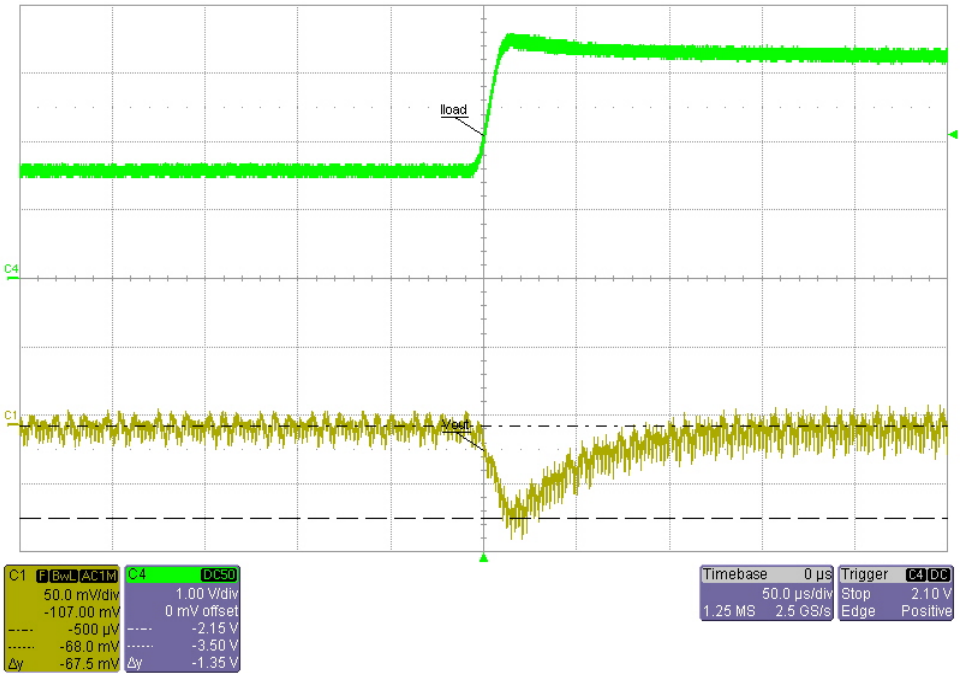


Figure 15

Ch1 => AC coupled output voltage

Ch2 => Output current
1V= 10A

Slope of step:
1.75A/15.8µs

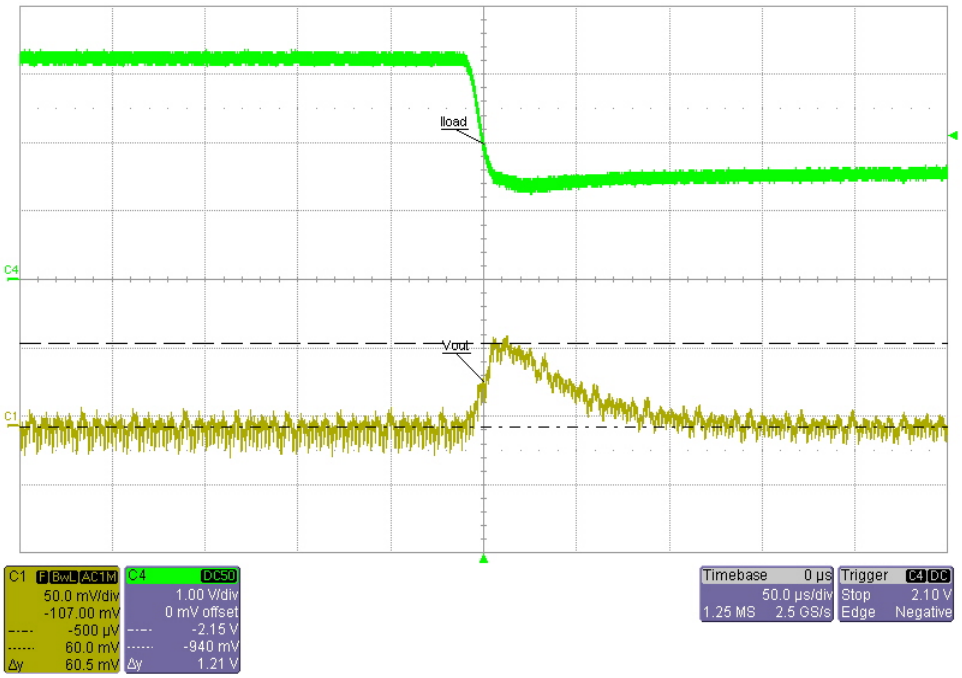


Figure 16

Ch1 => AC coupled output voltage

Ch2 => Output current
1V = 10A

Slope of step:
1.75A/14.2µs

7. Frequency Response

Figure 17 shows the loop response of the 1.1V output with 2A load and 12V input.

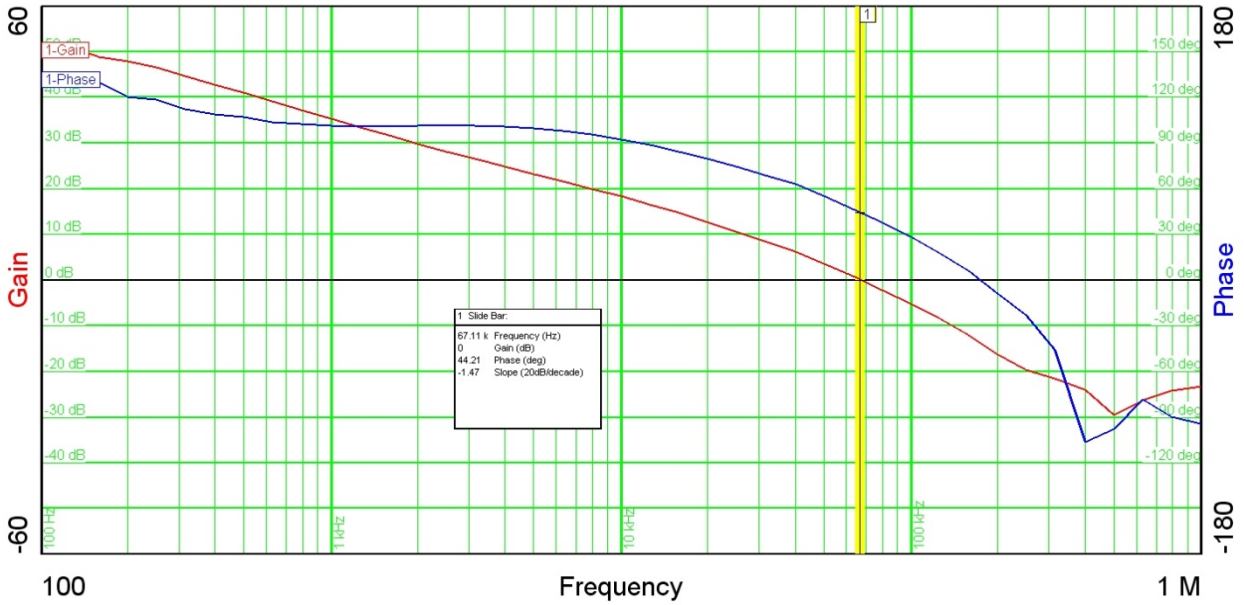


Figure 17

Table 1 summarizes the results from Figure 17.

Bandwidth (kHz)	67.11
Phase Margin	44.21°
Slope (20dB/Decade)	-1.47

Table 1

Figure 18 shows the loop response of the 1.5V output with 2A load and 12V input.

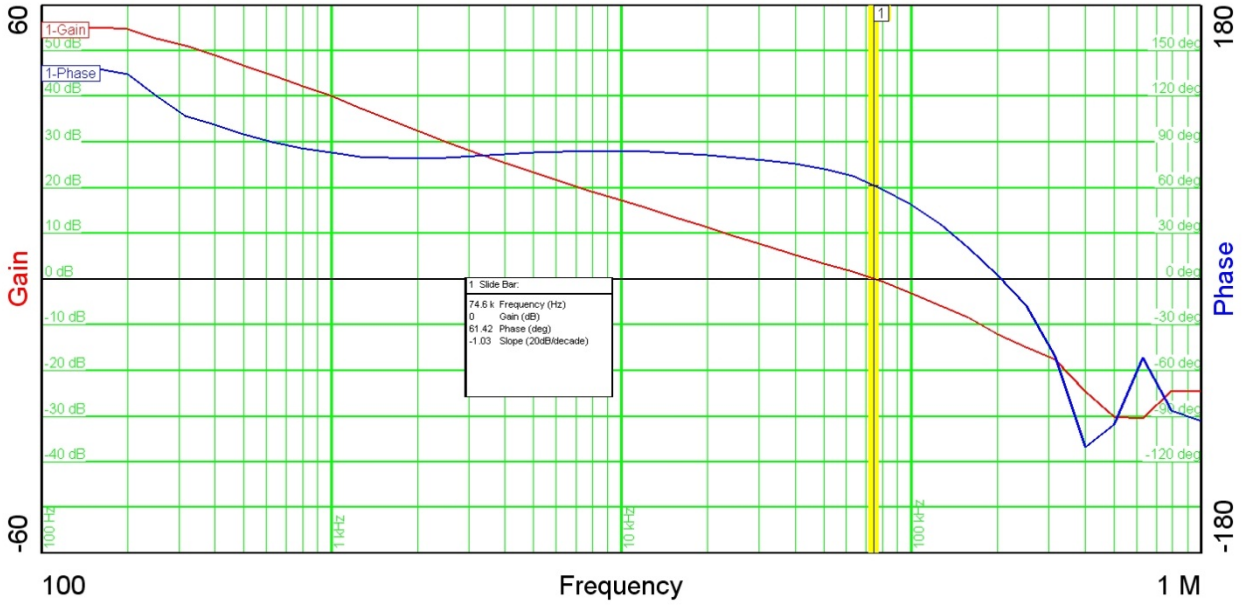


Figure 18

Table 2 summarizes the results from Figure 18.

Bandwidth (kHz)	75.6
Phase Margin	61.42°
Slope (20dB/Decade)	-1.03

Table 2

Figure 19 shows the loop response of the 3.3V output with 2A load and 12V input.

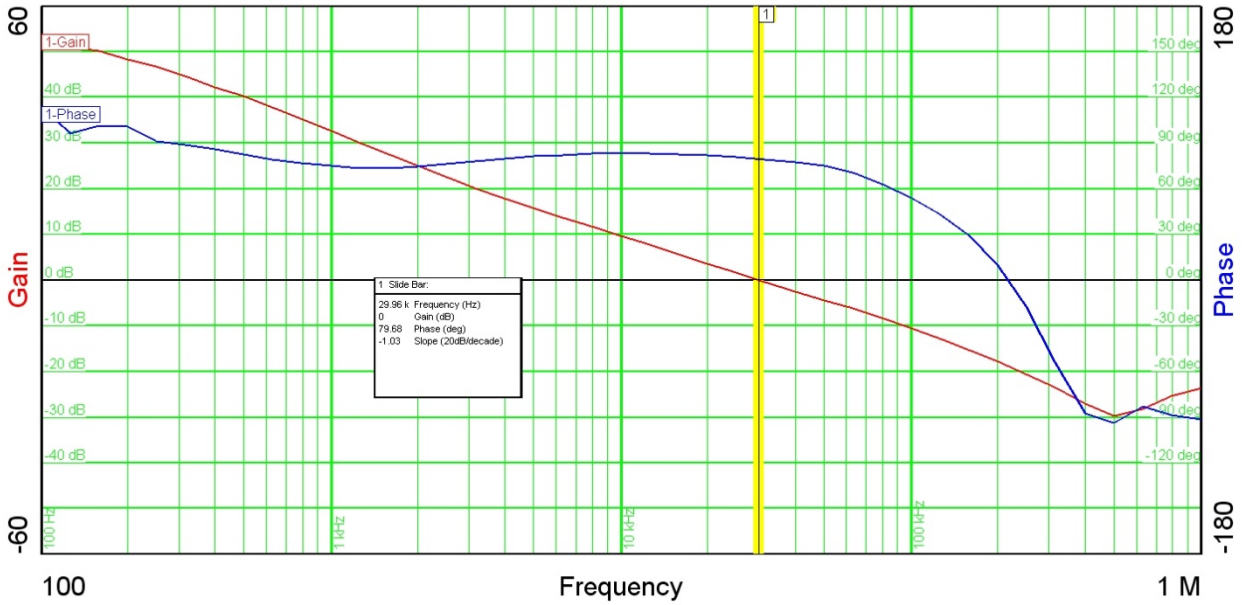


Figure 19

Table 3 summarizes the results from Figure 19.

Bandwidth (kHz)	29.96
Phase Margin	79.68°
Slope (20dB/Decade)	-1.03

Table 3

Figure 20 shows the loop response of the 2.5V output with 2A load and 12V input.

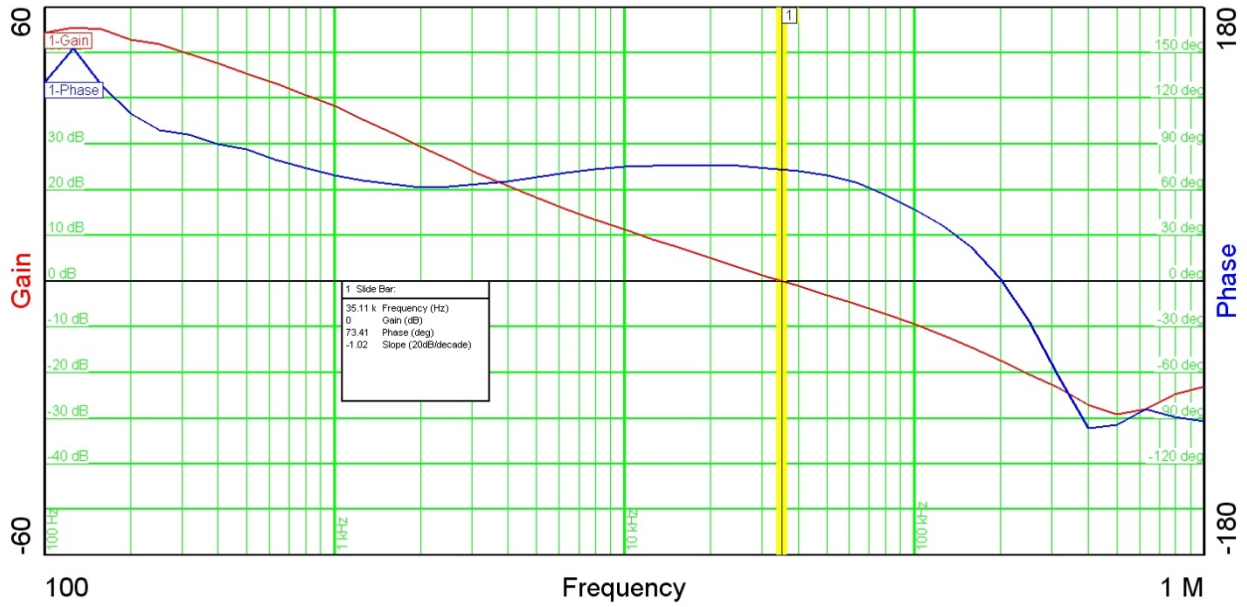


Figure 20

Table 4 summarizes the results from Figure 19.

Bandwidth (kHz)	35.11
Phase Margin	73.41°
Slope (20dB/Decade)	-1.02

Table 4

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