

# TPSM846C23 Power Module Evaluation Module User's Guide



## ABSTRACT

This user's guide contains information for the TPSM846C23EVM-806 evaluation module (PWR806). The document also includes the performance specifications, schematic, bill of materials, and layout of the EVM.

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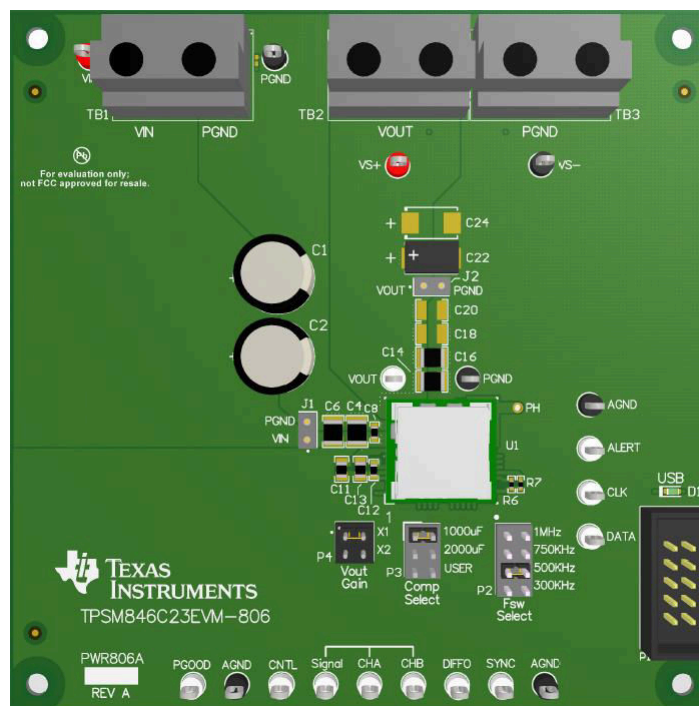
## 1 Description

The TPSM846C23 is a highly integrated, PMBus enabled, synchronous buck power module that combines a 35-A DC/DC converter with power MOSFETs, a shielded inductor, some input and output capacitors, and passives into a low profile package. The input voltage range is 4.5 V to 15 V. The output voltage ranges is 0.35 V to 2 V. The PMBus interface provides for converter configuration as well as monitoring of key parameters including output voltage, output current, and the internal die temperature, as well as many user-programmable configuration options.

This evaluation module is designed to demonstrate the ease-of-use and small printed circuit board area that may be achieved when designing with the TPSM846C23 power module. Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line and load regulation, and transient response. Additionally, control test points are provided for use of the power good, enable control, and synchronization features of the device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

## 2 Getting Started

Figure 2-1 highlights the user interface items associated with the EVM. The polarized input power terminal block (TB1) is used for connection to the host input supply. TB2 allows two terminals for VOUT and TB3 allows two terminals for PGND for connection to the load. These terminal blocks can accept up to 10 AWG wire.



**Figure 2-1. EVM User Interface**

The VIN Monitor (VIN and PGND) test points and VOUT Monitor (VS+ and VS–) test points located near the input terminal block and the output terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure the input and output voltages. Do not use these VIN and VOUT monitoring test points as the input supply or output load connection points. The PCB traces connecting to these test points are not designed to support high currents.

The VIN Scope (J1) and VOUT Scope (J2) test points can be used to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1 inch centers. The scope probe tip should be inserted into the socket labeled VIN or VOUT, and the scope ground lead should be inserted into the hole of the socket labeled PGND.

The test points located along the bottom of the EVM are made available to test the features of the device. Any external connections made to these test points should be referenced to one of the AGND test points. Refer to [Section 3](#) of this guide for more information on the individual control test points.

The PMBus connector (P1) is provided to connect the USB to GPIO interface pod to the EVM. The USB to GPIO interface pod connects the EVM to a computer USB port which allows the TI “Fusion” Graphical User Interface (GUI) to communicate and control the EVM. To download the latest software visit, [http://www.ti.com/tool/fusion\\_digital\\_power\\_designer](http://www.ti.com/tool/fusion_digital_power_designer).

The ALERT, DATA, CLK and CNTL test points are used to monitor the PMBus signals. Reference the [TPSM846C23 4.5-V to 15-V In, 0.35-V to 2-V Out, 35-A PMBus Power Module Data Sheet](#) for details on the supported PMBus commands.

The PMBus address is set by resistors R6 and R7. The PMBus address is 27 (decimal), 1B (hex).

The Vout Gain jumper (P4) is used to set the output voltage range. Select X1 for output voltages between 0.35 V–1.65 V and select X2 for output voltages between 1.65 V–2.0 V. The default loading is the X1 position.

The Comp Select jumper (P3) sets the proper frequency compensation for the total amount of output capacitance present on the  $V_{OUT}$  bus. The EVM is shipped with approximately 1000  $\mu\text{F}$  of output capacitance loaded on the board. Locations are provided on the board to add additional output capacitance (C18–C21, C24, C25). The default Comp Select jumper is loaded in the 1000- $\mu\text{F}$  position which is the correct setting for output capacitance from 1000  $\mu\text{F}$  to 1500  $\mu\text{F}$ . The jumper position labeled 2000  $\mu\text{F}$  selects compensation components for 1500  $\mu\text{F}$  to 3000  $\mu\text{F}$  of output capacitance. The jumper position labeled USER selects compensation components for 3000  $\mu\text{F}$  to 5000  $\mu\text{F}$  of output capacitance. See the [TPSM846C23 4.5-V to 15-V In, 0.35-V to 2-V Out, 35-A PMBus Power Module Data Sheet](#) for more information on selecting compensation components.

The Fsw Select jumper (P2) is used to set the switching frequency. Select from 300 kHz, 500 kHz, 750 kHz, and 1 MHz. The default jumper loading is the 500-kHz position.

### 3 Test Point Descriptions

Wire-loop test points and scope probe test points are provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. A description of each test point follows:

**Table 3-1. Test Points**

VIN	Input voltage monitor. Connect DVM across this point and PGND for measuring efficiency.
VS+	Supply path output voltage monitor. Connect DVM positive lead to this point for line and load regulation.
VS-	Return path output voltage monitor. Connect DVM negative lead to this point for measuring line and load regulation.
VOUT	Output voltage monitor. Connect DVM to this point and PGND for measuring efficiency.
PGND	Input and output voltage monitor grounds. Reference the VIN and VOUT DVMs to these ground points.
VIN MON (J1)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT MON (J2)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
AGND	Analog ground point. Use any of the AGND test points as the ground reference for the control signals.
ALERT	PMBus ALERT line. Used to monitor the ALERT signal.
CLK	PMBus CLK line. Used to monitor the CLK signal.
DATA	PMBus DATA line. Used to monitor the DATA signal.
PGOOD	Monitors the power good signal of the device. This is an open-drain signal that has an on-board 10-k $\Omega$ pullup resistor to 3.3V.
CNTL	Control pin. Pull to GND to stop power conversion. Float or pull to 3.3 V to enable power conversion. An internal 10 k $\Omega$ pullup resistor to 3.3V is present on the EVM.
Signal	Signal injection point for the Bode plot analyzer. Inject from Signal to CHB.
CHA	Input signal monitoring point for the Bode plot analyzer.
CHB	Output signal monitoring point for the Bode plot analyzer
DIFFO	Output of remote sense differential amplifier
SYNC	Connects to the SYNC pin of the device. An external clock signal can be applied to this point to synchronize the device to an appropriate frequency.
PH	Switch node of the TPSM846C23 device. Use an un-hooded scope probe to monitor this point.

#### Note

Refer to the [TPSM846C23 4.5-V to 15-V In, 0.35-V to 2-V Out, 35-A PMBus Power Module Data Sheet](#) for absolute maximum ratings associated with features in Table 3-1.

## 4 Operation Notes

In order to operate the EVM, apply a valid input voltage of 4.5 V to 15 V. The power supply providing the input voltage must be rated for sufficient input current. The under voltage lock out (UVLO) can be programmed using the PMBus commands.

The output voltage is set at the factory to 0.6 V. It can be programmed over the allowable output voltage range by using the PMBus VOUT\_COMMAND.

The TPSM846C23 is a 35-A device. When connecting the EVM to the external load, use wiring capable of safely handling 35 A of output current.

The Power-Good (PGOOD) indicator of the EVM will assert high when the output voltage is within  $\pm 5\%$  of the programmed output voltage value. A 10-k $\Omega$  pullup resistor (R11) is populated between the PGOOD pin and the BP3 pin.

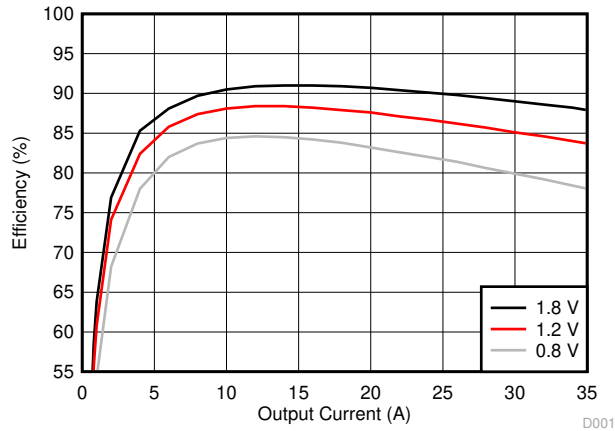
The TPSM846C23 EVM is set-up to operate at 500 kHz, but the switching frequency can be adjusted using the P2 jumper. If an exact switching frequency is required, the device can be synchronized to an external clock over the frequency range of 300 kHz to 1 MHz. Refer to the [TPSM846C23 4.5-V to 15-V In, 0.35-V to 2-V Out, 35-A PMBus Power Module Data Sheet](#) for further information on synchronization.

The TPSM846C23 EVM includes both input and output capacitors. The EVM includes footprints for adding additional input and output capacitors to the EVM. Adding additional capacitance will improve transient response. The actual capacitance required will depend on the input and output voltage conditions of the particular application, along with the desired transient response. Refer to the [TPSM846C23 4.5-V to 15-V In, 0.35-V to 2-V Out, 35-A PMBus Power Module Data Sheet](#) for further information on input and output capacitance and transient response.

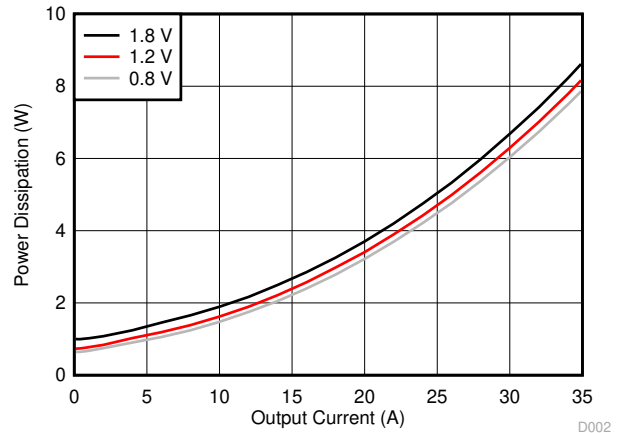
The EVM uses remote sense connections to regulate the output voltage at the output terminals of the EVM. The remote sense connections are made through 0- $\Omega$  resistors, R16 and R18. If remote sense is required at a different point, R16 and R18 can be replaced with 10- $\Omega$  resistors and VS+ and VS- test points can be extended to the new sense point.

## 5 Performance Data

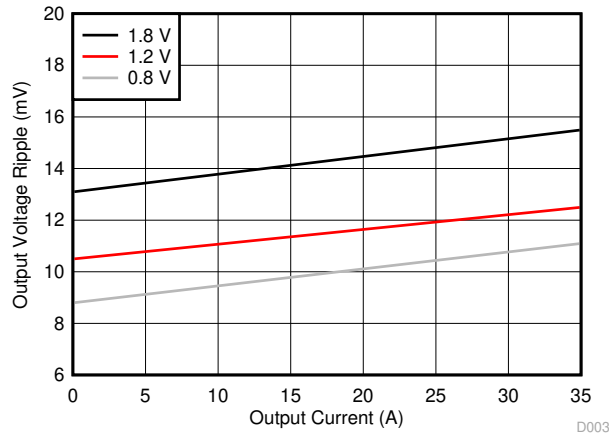
$V_{IN} = 12\text{ V}$ ,  $F_{sw} = 500\text{ kHz}$ ,  $C_{OUT} = 4 \times 47\text{-}\mu\text{F}$  ceramic plus  $2 \times 470\text{-}\mu\text{F}$  polymer



**Figure 5-1. Efficiency**



**Figure 5-2. Power Dissipation**



**Figure 5-3. Output Voltage Ripple**

## 6 Schematic

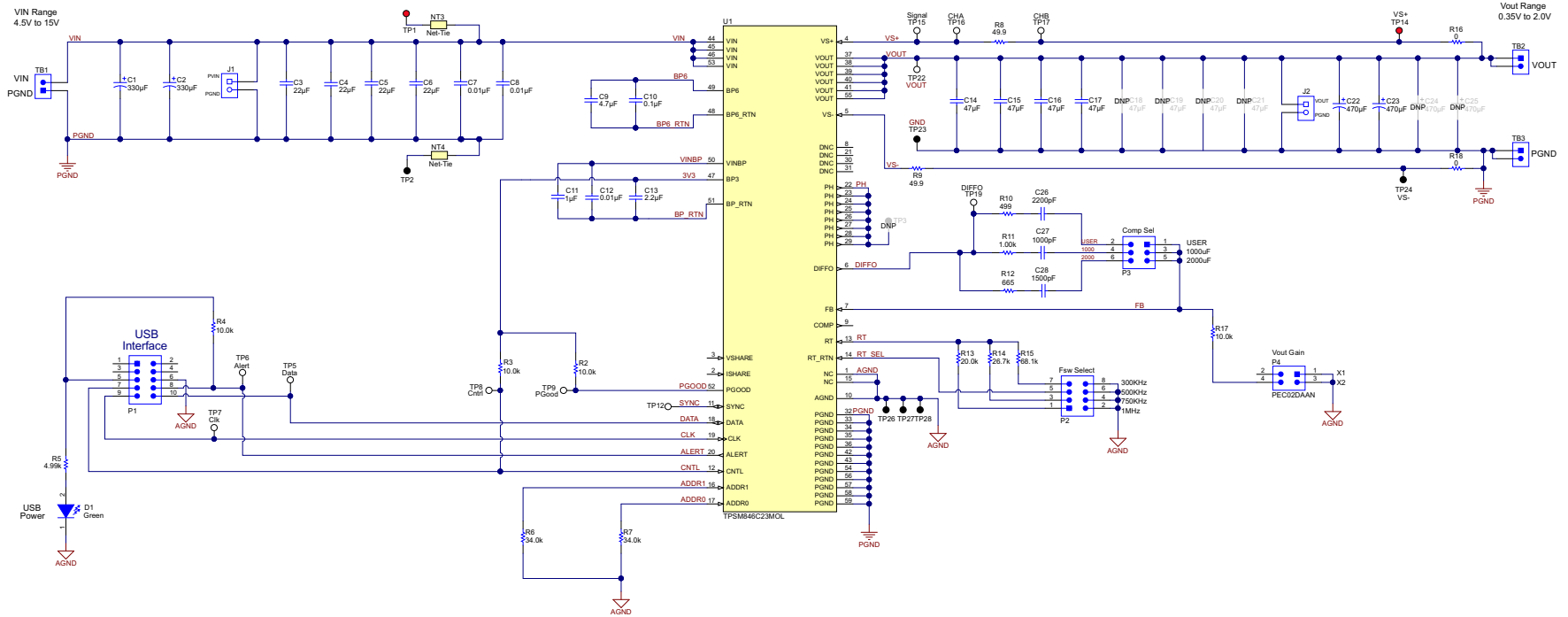


Figure 6-1. TPSM846C23EVM Schematic

## 7 Bill of Material

**Table 7-1. TPSM846C23EVM Bill of Material**

DESIGNATOR	QUANTITY	DESCRIPTION	PART NUMBER	MANUFACTURER
PCB	1	Printed Circuit Board	74-01196	Any
U1	1	TPSM846C23	TPSM846C23MOL	Texas Instruments
C1, C2	2	CAP, AL, 330 $\mu$ F, 25 V, $\pm$ 20%, 0.053 $\Omega$ , TH	25ZL330MEFC10X12.5	Rubycon
C3, C4, C5, C6	4	CAP, CERM, 22 $\mu$ F, 25 V, $\pm$ 10%, X5R, 1210	GRM32ER61E226KE15L	MuRata
C7, C8, C12	3	CAP, CERM, 0.01 $\mu$ F, 50 V, $\pm$ 10%, X7R, 0603	GRM188R71H103KA01D	MuRata
C9	1	CAP, CERM, 4.7 $\mu$ F, 16 V, $\pm$ 10%, X5R, 0805	GRM21BR61C475KA88L	MuRata
C10	1	CAP, CERM, 0.1 $\mu$ F, 16 V, $\pm$ 10%, X7R, 0603	GRM188R71C104KA01D	MuRata
C11	1	CAP, CERM, 1 $\mu$ F, 25 V, $\pm$ 10%, X7R, 0805	GRM21BR71E105KA99L	MuRata
C13	1	CAP, CERM, 2.2 $\mu$ F, 16 V, $\pm$ 10%, X7R, 0805	GRM21BR71C225KA12L	MuRata
C14, C15, C16, C17	4	CAP, CERM, 47 $\mu$ F, 6.3 V, $\pm$ 20%, X5R, 1210	GRM32ER60J476ME20L	MuRata
C18, C19, C20, C21	0	CAP, CERM, 47 $\mu$ F, 6.3 V, $\pm$ 20%, X5R, 1210	GRM32ER60J476ME20L	MuRata
C22, C23	2	CAP, Tantalum Polymer, 470 $\mu$ F, 6.3 V, $\pm$ 20%, 0.01 $\Omega$ , 7343-40 SMD	6TPF470MAH	Panasonic
C24, C25	0	CAP, Tantalum Polymer, 470 $\mu$ F, 6.3 V, $\pm$ 20%, 0.01 $\Omega$ , 7343-40 SMD	6TPF470MAH	Panasonic
C26	1	CAP, CERM, 2200 pF, 50 V, $\pm$ 10%, X7R, 0402	GRM155R71H222KA01D	MuRata
C27	1	CAP, CERM, 1000 pF, 16 V, $\pm$ 10%, X7R, 0402	GRM155R71C102KA01D	MuRata
C28	1	CAP, CERM, 1500 pF, 50 V, $\pm$ 10%, X7R, 0402	GRM155R71H152KA01D	MuRata
D1	1	LED, Green, SMD	150060GS75000	Wurth Elektronik
J1, J2	2	Socket Strip, 2 $\times$ 1, 100 mil, Black, Tin, TH	310-43-102-41-001000	Mill-Max
P1	1	Header, 100 mil, 5 $\times$ 2, Tin, TH	PEC05DAAN	Sullins Connector Solutions
P2	1	Header, 100 mil, 4 $\times$ 2, Tin, TH	PEC04DAAN	Sullins Connector Solutions
P3	1	Header, 100 mil, 3 $\times$ 2, Tin, TH	PEC03DAAN	Sullins Connector Solutions
P4	1	Header, 100 mil, 2 $\times$ 2, Tin, TH	PEC02DAAN	Sullins Connector Solutions
R2, R3, R4, R17	4	RES, 10.0 k, 1%, 0.063 W, 0402	CRCW040210K0FKED	Vishay-Dale
R5	1	RES, 4.99 k, 1%, 0.063 W, 0402	CRCW04024K99FKED	Vishay-Dale
R6, R7	2	RES, 121 k, 1%, 0.063 W, 0402	CRCW0402121KFKED	Vishay-Dale
R8, R9	2	RES, 49.9, 1%, 0.1 W, 0603	CRCW060349R9FKEA	Vishay-Dale
R10	1	RES, 499, 1%, 0.063 W, 0402	CRCW0402499RFKED	Vishay-Dale
R11	1	RES, 1.00 k, 1%, 0.063 W, 0402	CRCW04021K00FKED	Vishay-Dale
R12	1	RES, 665, 1%, 0.063 W, 0402	CRCW0402665RFKED	Vishay-Dale
R13	1	RES, 20.0 k, 1%, 0.063 W, 0402	CRCW040220K0FKED	Vishay-Dale
R14	1	RES, 26.7 k, 1%, 0.063 W, 0402	CRCW040226K7FKED	Vishay-Dale
R15	1	RES, 68.1 k, 1%, 0.063 W, 0402	CRCW040268K1FKED	Vishay-Dale
R16, R18	2	RES, 0, 5%, 0.1 W, 0603	CRCW0603000Z0EA	Vishay-Dale
TB1, TB2, TB3	3	Terminal Block, 30 A, 9.52 mm (.375) Pitch, 2-Pos, TH	OSTT7022150	On-Shore Technology
TP5, TP6, TP7, TP8, TP9, TP12, TP15, TP16, TP17, TP19, TP22	11	Test Point, Multipurpose, White, TH	5012	Keystone
TP2, TP23, TP24, TP26, TP27, TP28	6	Test Point, Multipurpose, Black, TH	5011	Keystone
TP1, TP14	2	Test Point, Multipurpose, Red, TH	5010	Keystone



## 8 PCB Layout

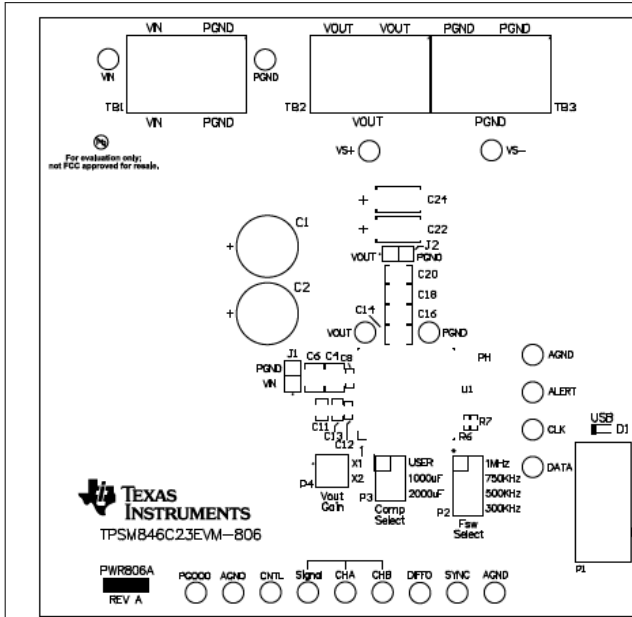


Figure 8-1. Top Components

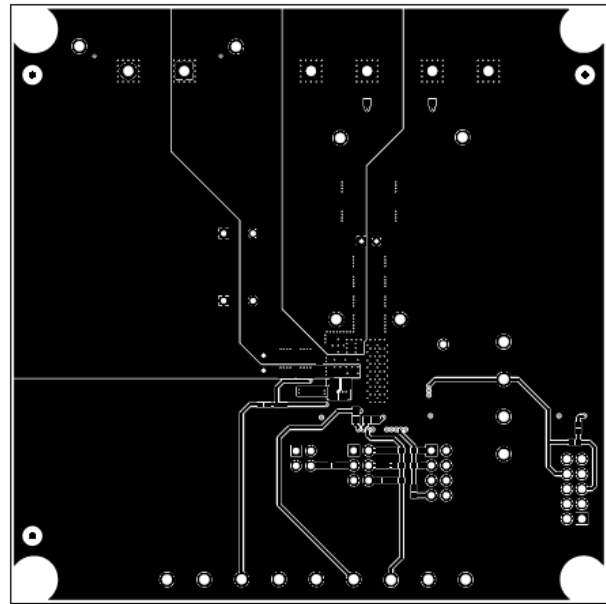


Figure 8-2. Topside Copper

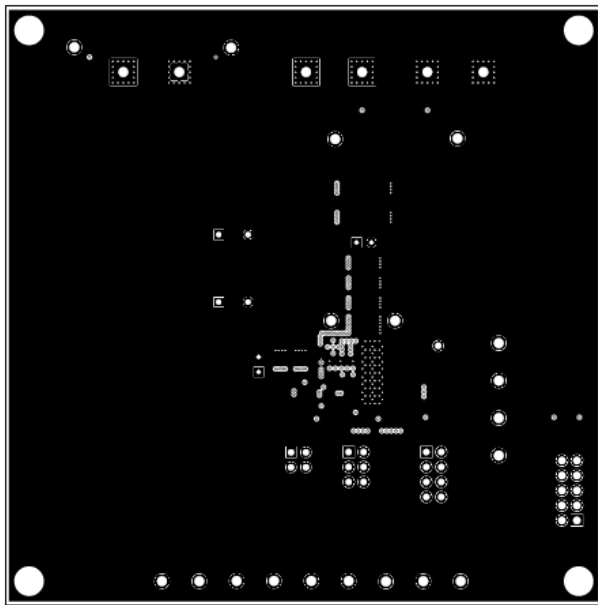


Figure 8-3. Layer 2 Copper

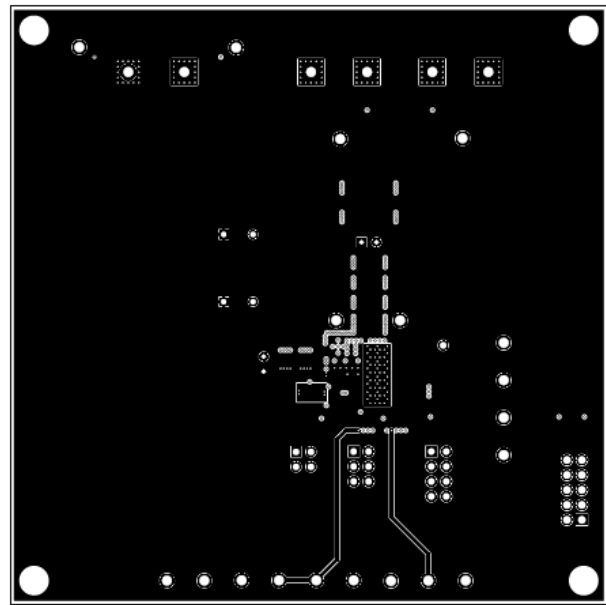


Figure 8-4. Layer 3 Copper

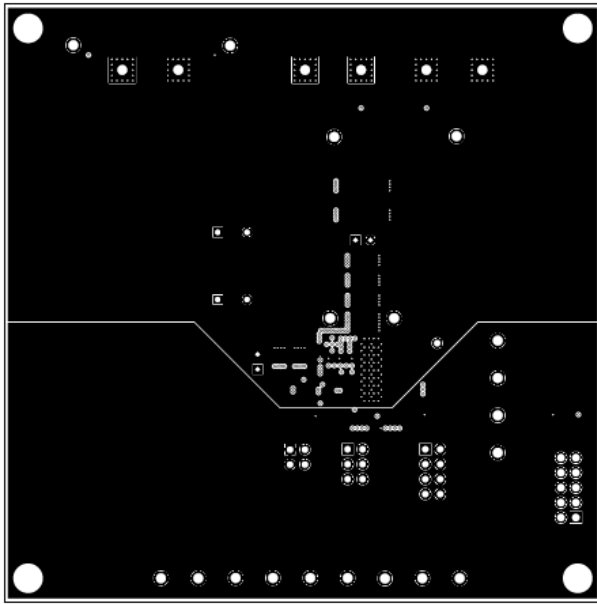


Figure 8-5. Layer 4 Copper

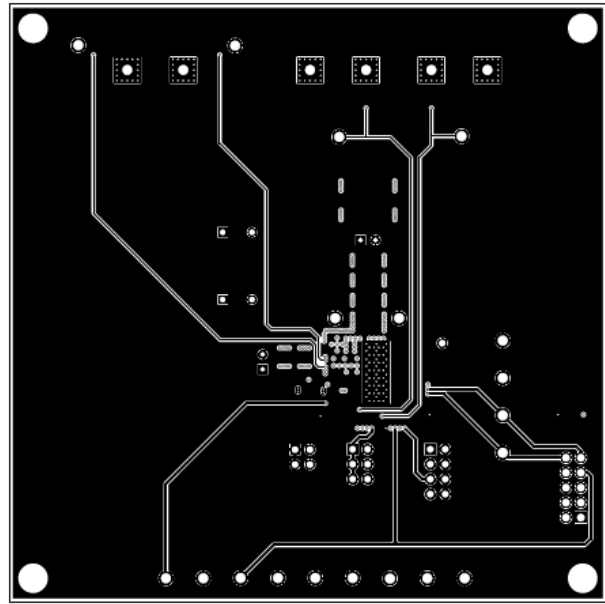


Figure 8-6. Layer 5 Copper

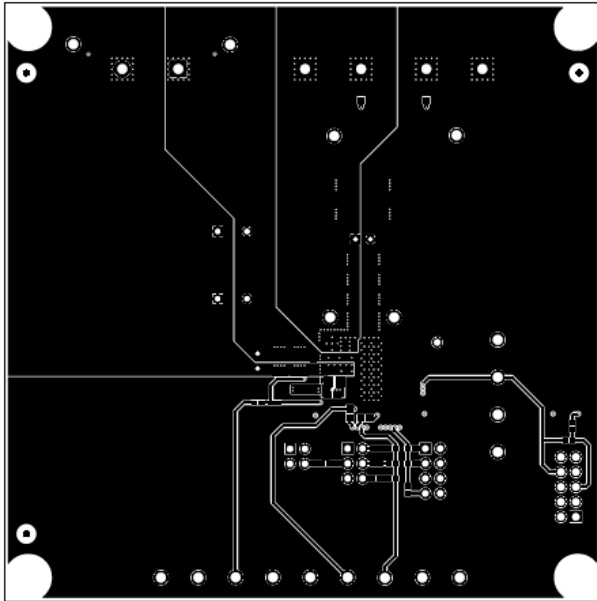


Figure 8-7. Bottom-Side Copper

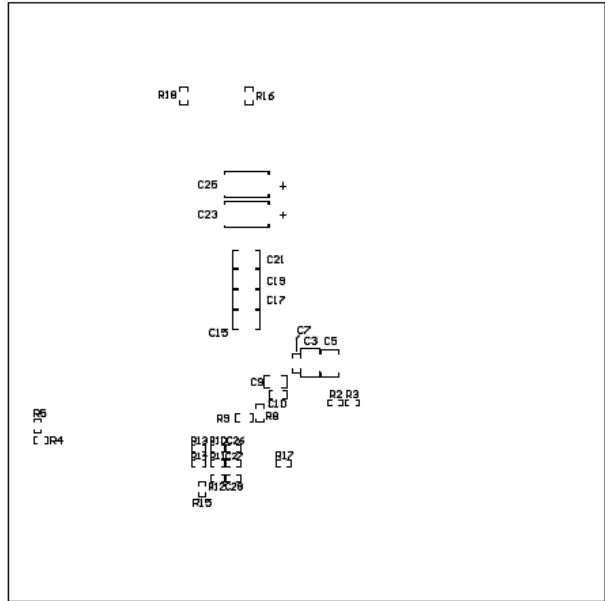


Figure 8-8. Bottom Components

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2017) to Revision B (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document. ....	2
• Updated the updated user's guide .....	2
Changes from Revision * (March 2017) to Revision A (June 2017)	Page
• Changed link to <a href="http://www.ti.com/tool/fusion_digital_power_designer">http://www.ti.com/tool/fusion_digital_power_designer</a> .....	2

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