User's Guide

DRV87xx-Q1EVM & DRV8106-Q1EVM User's Guide

ABSTRACT

This document is provided as a supplement to evaluate the DRV8706x-Q1, DRV8106x-Q1, DRV8705x-Q1, DRV8714x-Q1, & DRV8718x-Q1 customer evaluation modules (EVMs).

These motor drivers are highly integrated H-bridge gate drivers, capable of driving high-side and low-side N-channel power MOSFETs. The ICs generates the proper gate drive voltages using an integrated charge pump for the high-side and a linear regulator for the low-side (doubler for DRV8106x-Q1, DRV8705x-Q1 and DRV8706x-Q1, and configurable doubler/ tripler for DRV8714x-Q1 and DRV8718x-Q1). The device uses a smart gate drive architecture to reduce system cost and improve reliability. The gate driver optimizes dead time to avoid shoot-through conditions, provides control to decreasing electromagnetic interference (EMI) through adjustable gate drive current, and protects against drain to source and gate short conditions with VDS and VGS monitors. A wide common mode shunt amplifier provides inline current sensing to continuously measure motor current even during recirculating windows. The amplifier can be used in low-side or high-side sense configurations if inline sensing is not required.

The motor driver provides an array of protection features to ensure robust system operation. These include under and overvoltage monitors for the power supply and charge pump, VDS overcurrent and VGS gate fault monitors for the external MOSFETs, offline open load and short circuit diagnostics, and internal thermal warning and shutdown protection. The EVM has an H-bridge consisting of fourN-channel MOSFETs that drive motors bi-directionally at up to 15-A RMS, 20-A peak current or eight N-channel MOSFETs that drive motors bi-directionally at up to 30-A RMS, 40-A peak current .

The EVM operates from a single power supply for the analog power and from the USB line for the digital power, which can be customized to be externally supplied. A negative 18 V reverse battery protection circuit, along with a 20-A RMS rated PI filter are provided to clean up the power supply input and protect against reverse polarity battery connections.

More information on the motor drivers featured on this family of EVMs can be found on ti.com:

Device	Datasheet URL
DRV8106-Q1 (half-bridge gate driver)	*DRV8106-Q1 Automotive Half-Bridge Smart Gate Driver With Wide Common Mode Current Sense Amplifier data sheet*
DRV8705-Q1 (H-bridge gate driver)	*DRV8705-Q1 Automotive H-Bridge Smart Gate Driver With Low-Side Current Sense Amplifier*
DRV8706-Q1 (H-bridge gate driver)	*DRV8706-Q1 Automotive Half-Bridge Smart Gate Driver With Wide Common Mode Current Sense Amplifier data sheet*
DRV8714-Q1, DRV8718-Q1 (4- and 8-channel gate driver)	*DRV871x-Q1 Automotive H-Bridge Smart Gate Driver With Wide Common Mode Current Sense Amplifiers*

WARNING

Hot surface

On the DRV8706x-Q1EVM, DRV8106x-Q1EVM, DRV8705x-Q1, DRV8714x-Q1, or DRV8718x-Q1 EVM hot surfaces include the DRV8706x-Q1, DRV8106x-Q1, DRV8705x-Q1, DRV8714x-Q1, & DRV8718x-Q1 devices (U1), the power stage, the reverse battery protection FET and the areas surrounding them.

When operating the DRV8706x-Q1, DRV8106x-Q1, DRV8705x-Q1, DRV8714x-Q1, & DRV8718x-Q1EVM, the device overtemperature warning should be monitored for overtemperature warnings. The nFAULT pin indicates when the device temperature has increased above 140°C and is approaching thermal shutdown. As with any elevated temperatures, normal precautions must be followed to avoid direct contact with the hot surface of the DRV8706x-Q1EVM, DRV8106x-Q1EVM, DRV8705x-Q1EVM, DRV8714x-Q1EVM, or DRV8718x-Q1EVM.

To minimize potential fire hazard, personal injury, or both, externally provided fans may be required to adequately cool customer-provided loads depending on loading conditions.

CAUTION

Do not leave the EVM powered when unattended.

CAUTION

If applying DVDD to the motor driver externally, make sure the 0 ohm, DVDD to MCU resistor is not populated. MSP430F2617 can handle up to 4.2 V. DVDD > 4.2 V can damage the on board MCU.

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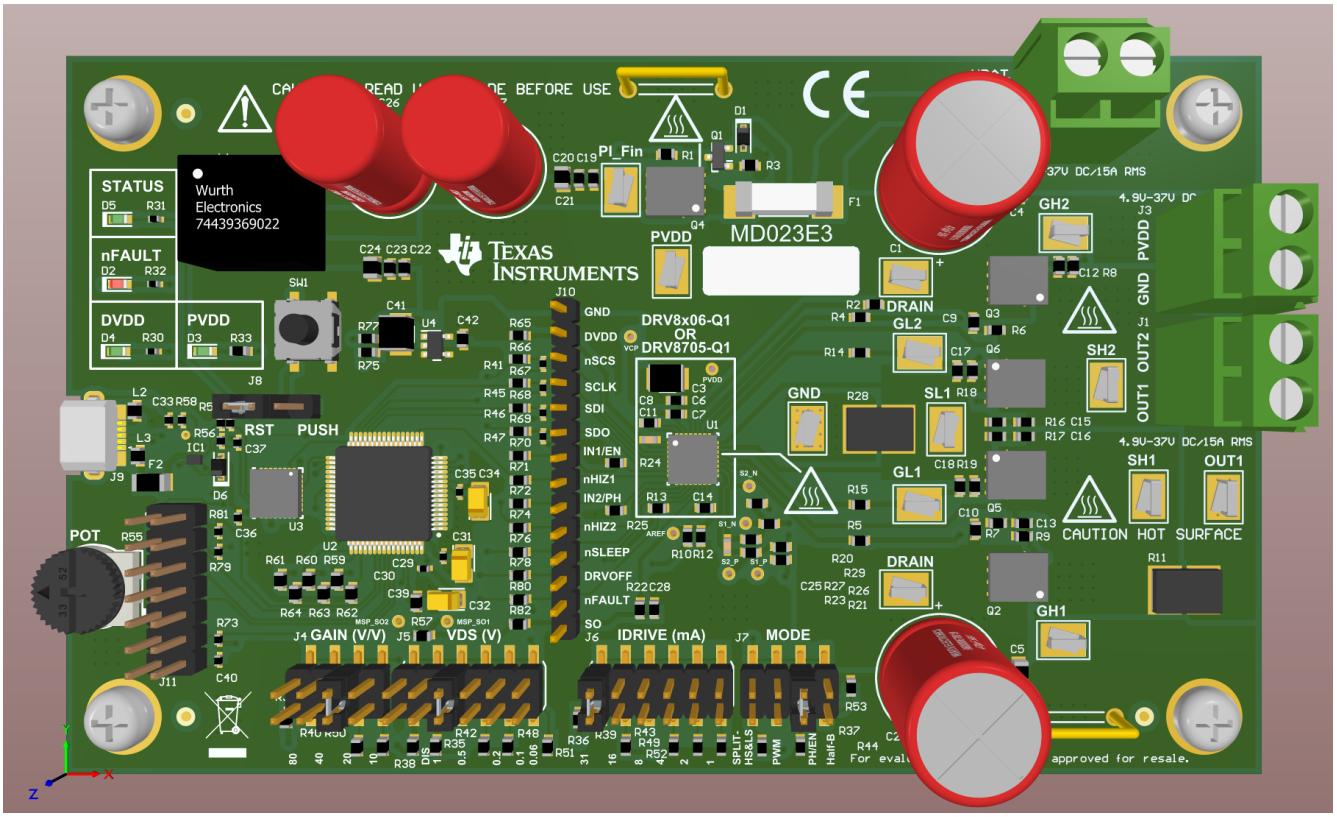

Figure 1-1. DRV8706H-Q1EVM

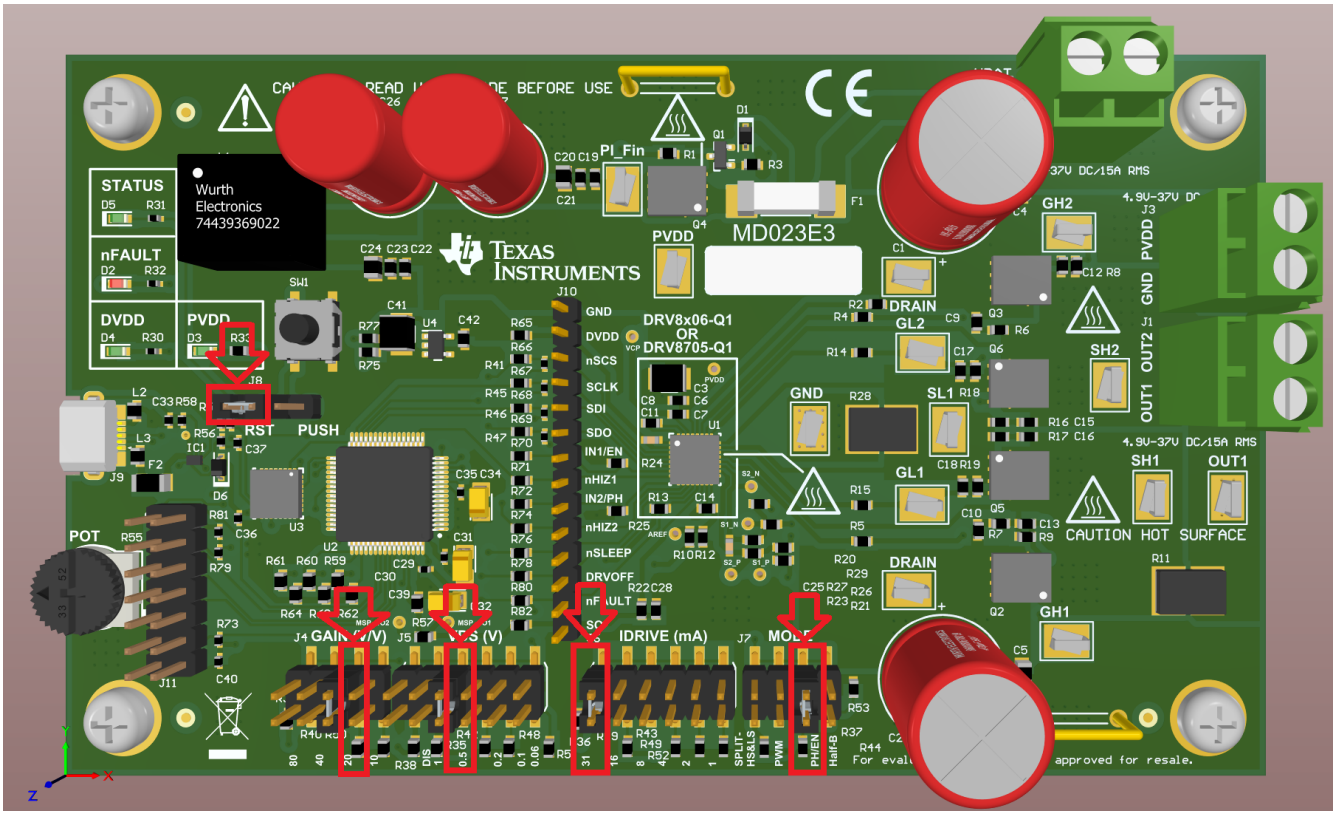

Figure 1-2. DRV8706H-Q1EVM with Default Jumper Locations

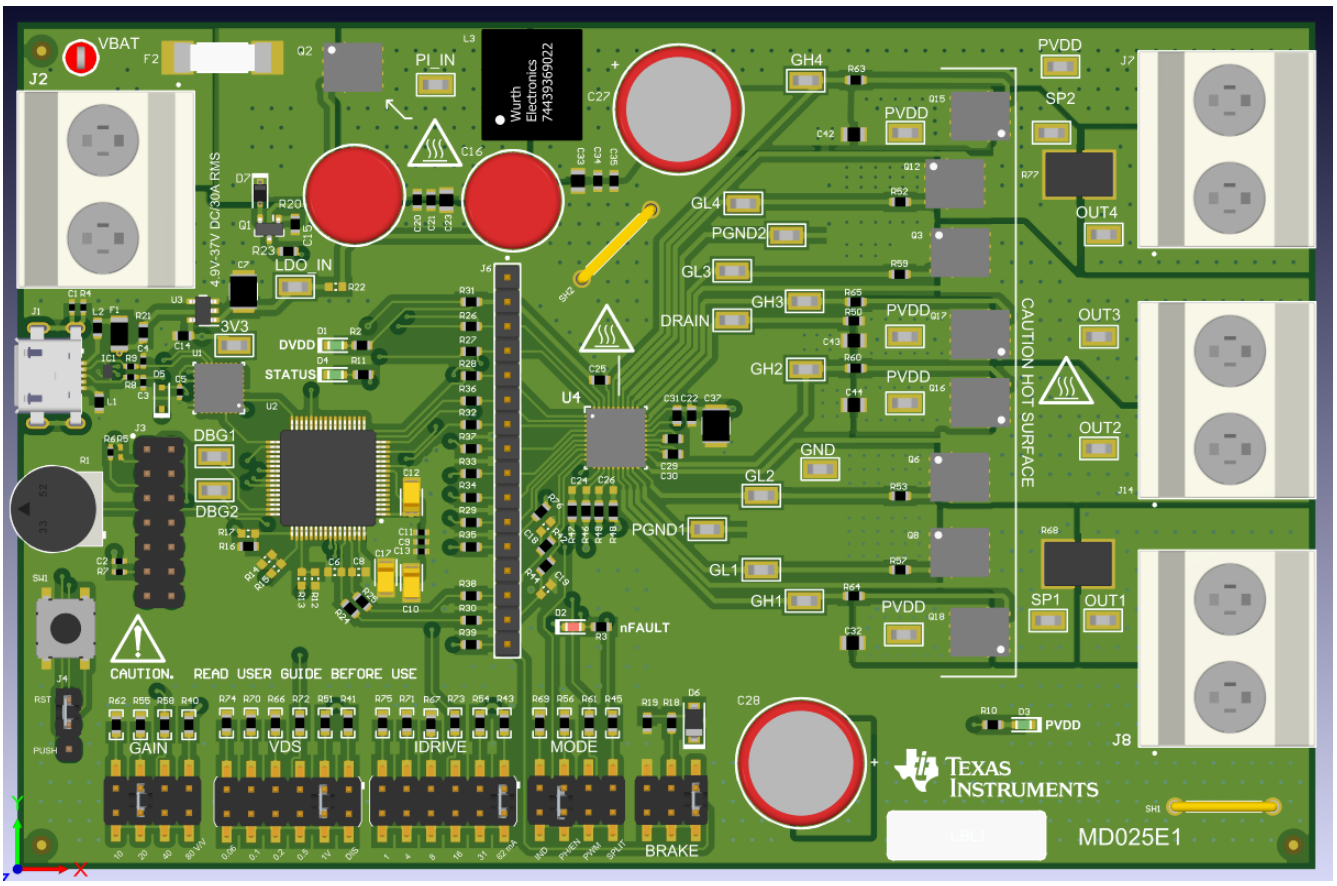

Figure 1-3. DRV8714H-Q1EVM (40-pin 6x6mm RHA package)

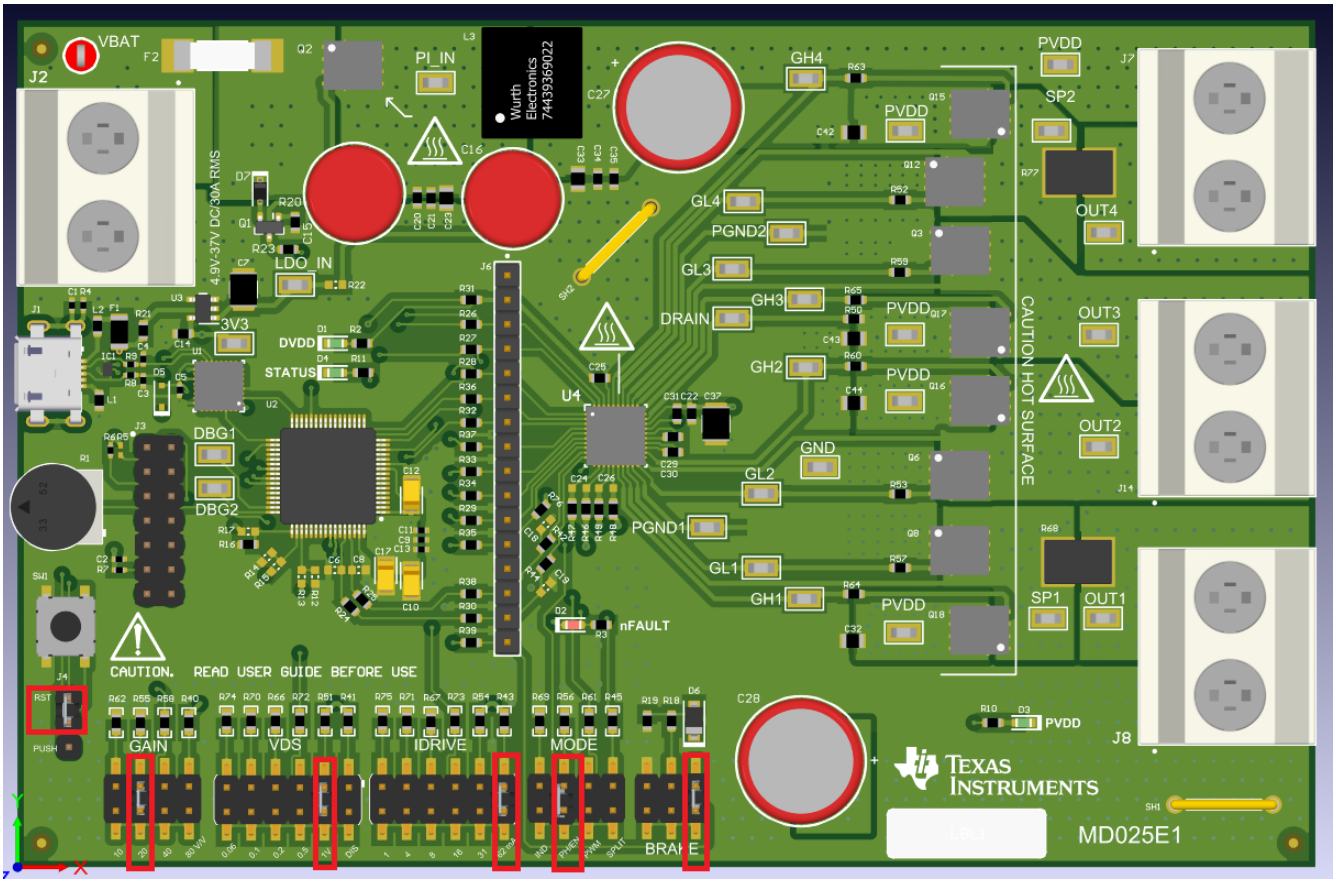

Figure 1-4. DRV8714H-Q1EVM (40-pin 6x6mm RHA package) Default Jumper Locations

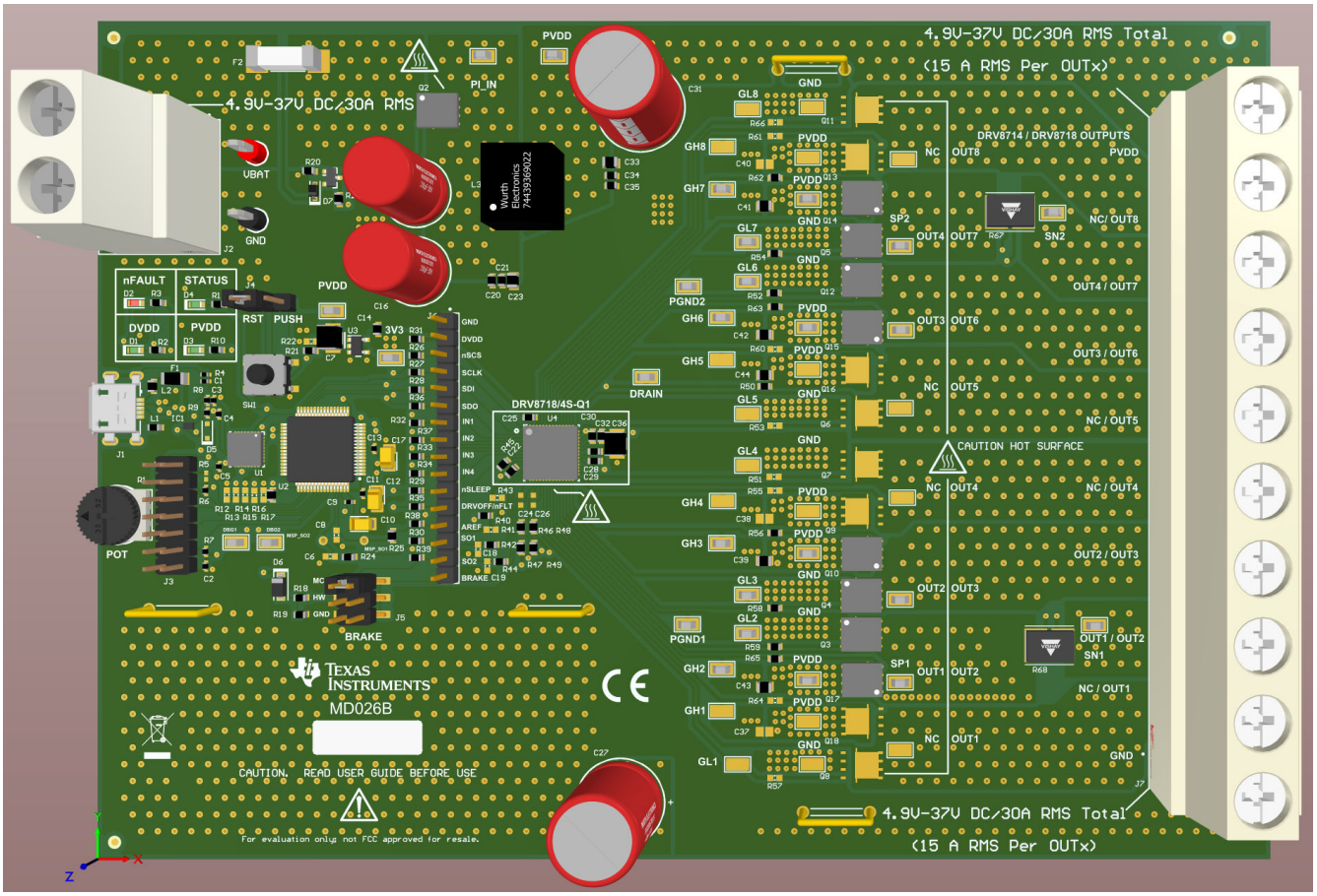

Figure 1-5. DRV8714S-Q1EVM and DRV8718S-Q1EVM (56-pin 8x8mm RVJ package) – DRV8714S-Q1EVM shown

The DRV8714S-Q1 and DRV8718S-Q1 are pin-compatible and use the same PCB fab for the EVM. The only difference is DNP components for unused channels on the DRV8714S-Q1EVM assembly variant. Table 1-1 is provided to communicate output channels electrical mapping of the two DRV8714S-Q1 and DRV8718S-Q1. When designing your board that can accommodate both DRV8714S-Q1 and DRV8718S-Q1 devices, study the pinout in the datasheet carefully to understand how the channels are mapped. Special consideration should be taken when assigning channels that will use the integrated current sense amplifiers. Note: the electrical channel mapping does not carry over to register settings (for example, channel 1 registers map to channel 1 on both devices).

Table 1-1. DRV8718x-Q1 through DRV8714x-Q1 device pin channel mapping

DRV8718S-Q1	DRV8714S-Q1	Notes
1	NC	
2	1	Mapped to CSA 1
3	2	
4	NC	
5	NC	
6	3	
7	4	Mapped to CSA 2
8	NC	

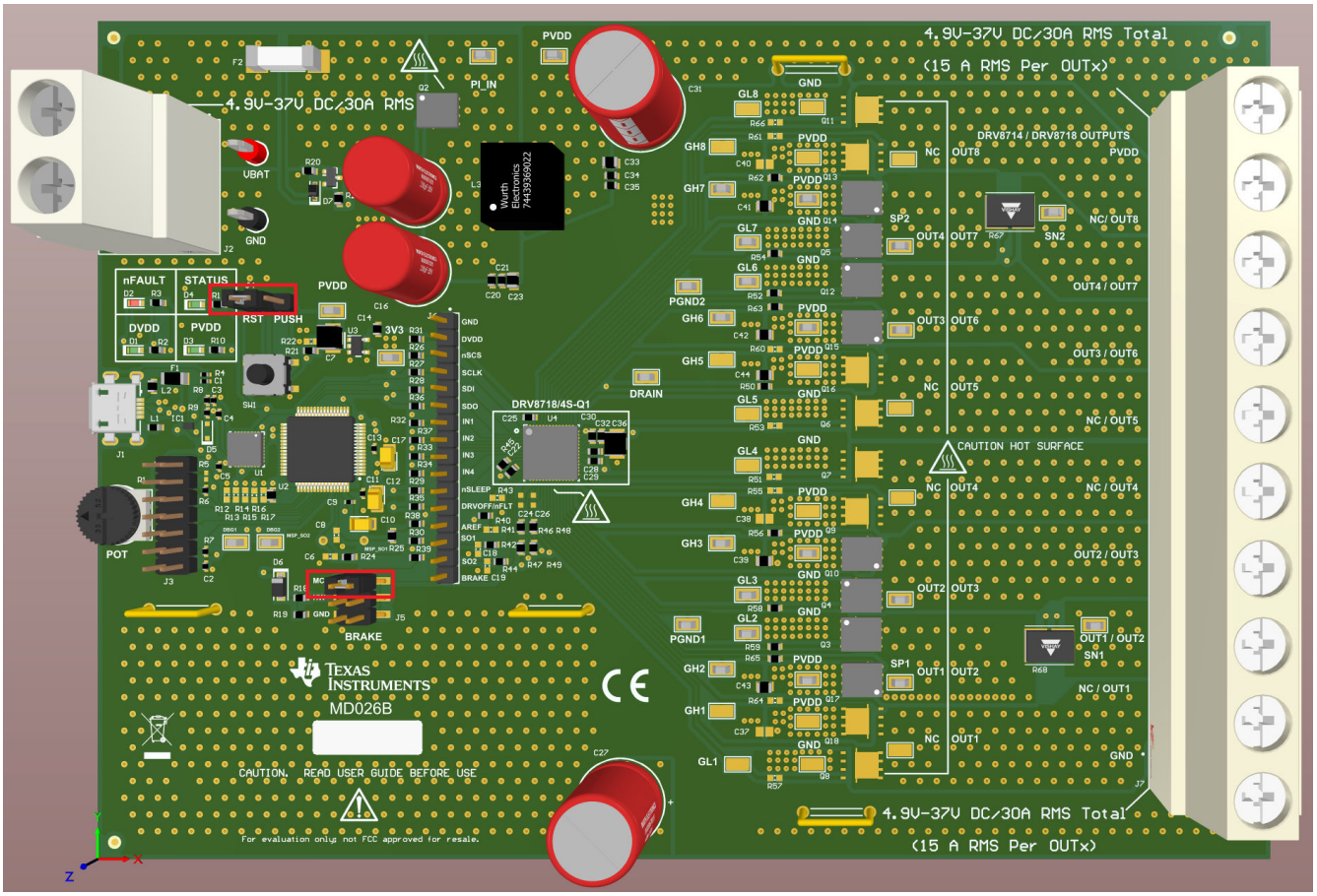

Figure 1-6. DRV8714S-Q1EVM and DRV8718S-Q1EVM (56-pin 8x8mm RVJ package) default jumper locations – DRV8714S-Q1EVM shown

As of the writing of this document, the 56-pin device variant only has an SPI-interface EVM variant, and thus does not have an array of jumpers like the previous evaluation boards. The hardware interface variant is covered by the DRV8714H-Q1EVM in the smaller 6x6mm package.

1.1 Overview

The DRV8106x-Q1, DRV8705x-Q1, DRV8706x-Q1, DRV8714x-Q1, & DRV8718x-Q1 devices are integrated motor gate driver devices, designed to drive one or multiple brushed DC motor(s) across a range of automotive applications.

DRV8106x-Q1 is a single half-bridge gate driver, with integrated wide common-mode input current sense amplifier for inline current sensing. Typical applications are high- or low-side switched loads, such as unidirectional motors, relay coils, or relay replacement.

DRV8705x-Q1 and DRV8706x-Q1 are H-bridge gate drivers, with integrated current sense amplifier (low-side or inline, respectively). These gate drivers can control a bidirectional brushed motor in H-bridge configuration, or two high- or low-side switched loads in independent half-bridge mode.

DRV8714x-Q1 and DRV8718x-Q1 are advanced multi-channel gate drivers (4 and 8 channels, respectively), both including two wide common-mode input current shunt amplifiers (CSA). A mix of H-bridge and half-bridge control is possible with these devices.

Device Evaluation Platform	PWM control inputs	PWM Input Modes	N-Channel MOSFETs	Integrated Current Sensing	Supply Input (DC)	RMS current (Amps)	Peak current (Amps)
DRV8106x-Q1EVM	1	Half-bridge control	2	1x inline CSA	4.9 – 37 V	15 A	20 A
DRV8705x-Q1EVM	2	Half-bridge control Phase/Enable H-bridge PWM H-Bridge Split HS & LS solenoid control	4	1x low-side CSA	4.9 – 37 V	15 A	20 A
DRV8706x-Q1EVM	2		4	1x inline CSA	4.9 – 37 V	15A	20A
DRV8714x-Q1EVM	4		8	2x inline CSA	4.9 – 37 V	15 A/ OUTx 30 A total	30 A/ OUTx 40 A total
DRV8718x-Q1EVM	4		16		4.9 – 37 V	15 A/ OUTx 30 A total	30 A/ OUTx 40A total

The devices in this family use a configurable PWM Mode interface for simple control of the gate driver outputs, consisting of N-channel MOSFETs, and operate across a wide supply input range from 4.9 V to 37 V DC.

The DRV8706x-Q1EVM, DRV8106x-Q1EVM utilize the integrated wide common mode, inline sense amplifier for load current monitoring with the MCU ADC. DRV8714x-Q1EVMs, and DRV8718x-Q1EVMs have two such instances. The DRV8705x-Q1EVMs utilize the low side sense amplifier for load current monitoring.

A low-power sleep mode is provided for very-low quiescent current draw by shutting down much of the internal circuitry when nSLEEP is logic LOW. Internal protection functions are provided for undervoltage lockout, charge pump faults, overcurrent protection, short-circuit protection, open-load and short circuit detection, overtemperature and other faults and/or warnings. Fault conditions are indicated on an nFAULT pin on both SPI and HW interface devices. Devices with SPI offer granular fault and diagnostic information (see device datasheet for more details).

1.2 Purpose and Scope

This document is designed to be used as a startup guide and to supplement your evaluation of the following EVMs:

- DRV8106x-Q1EVM
- DRV8705x-Q1EVM
- DRV8706x-Q1EVM
- DRV8714x-Q1EVM
- DRV8718x-Q1EVM

Additionally, it is intended for the engineers involved in the design, implementation and validation of the following Texas Instruments Smart Gate Drive devices using GUI control:

- DRV8106x-Q1
- DRV8705x-Q1
- DRV8706x-Q1
- DRV8714x-Q1
- DRV8718x-Q1

This document includes guidelines to evaluate these devices using the EVM and GUI, including required hardware (HW) connections. When the HW connections are complete, the user is may install the GUI on their local PC, or use a Chrome-based webbrowser version.

2 Hardware and Software Overview

2.1 Hardware Connections Overview for Single Channel H-Bridge and Half-Bridge EVMs

The major blocks of your EVM includes the DRV8705x-Q1, DRV8706x-Q1 or DRV8106x-Q1 smart gate driver, MSP430F2617 microcontroller (MCU), TPS7B6933 3.3-V LDO regulator, and the USB communication interface.

The DRV8705x-Q1EVM, DRV8706x-Q1EVM and DRV8106x-Q1EVM are designed for an input supply from 4.9 to 37 V DC through the power connector, and up to 15-A RMS or 20-A peak drive current through the load connection terminal(s).

The MCU communicates with the GUI to control the DRV8705x-Q1, DRV8706x-Q1, DRV8106x-Q1, DRV8714x-Q1, & DRV8718x-Q1 devices.

Note

On S variants, PVDD overvoltage is enabled and as a latched fault. To change the setting or the voltage magnitude the PVDD_OV trips at, refer to the datasheet for more information on register configuration settings.

On H variants, PVDD_OV is disabled.

2.1.1 EVM Module Details

DRV8705x-Q1EVM, DRV8706x-Q1EVM and DRV8106x-Q1EVM share a common hardware platform with assembly variations to cover the various differences (inline vs low-side current sensing and H-bridge vs half-bridge).

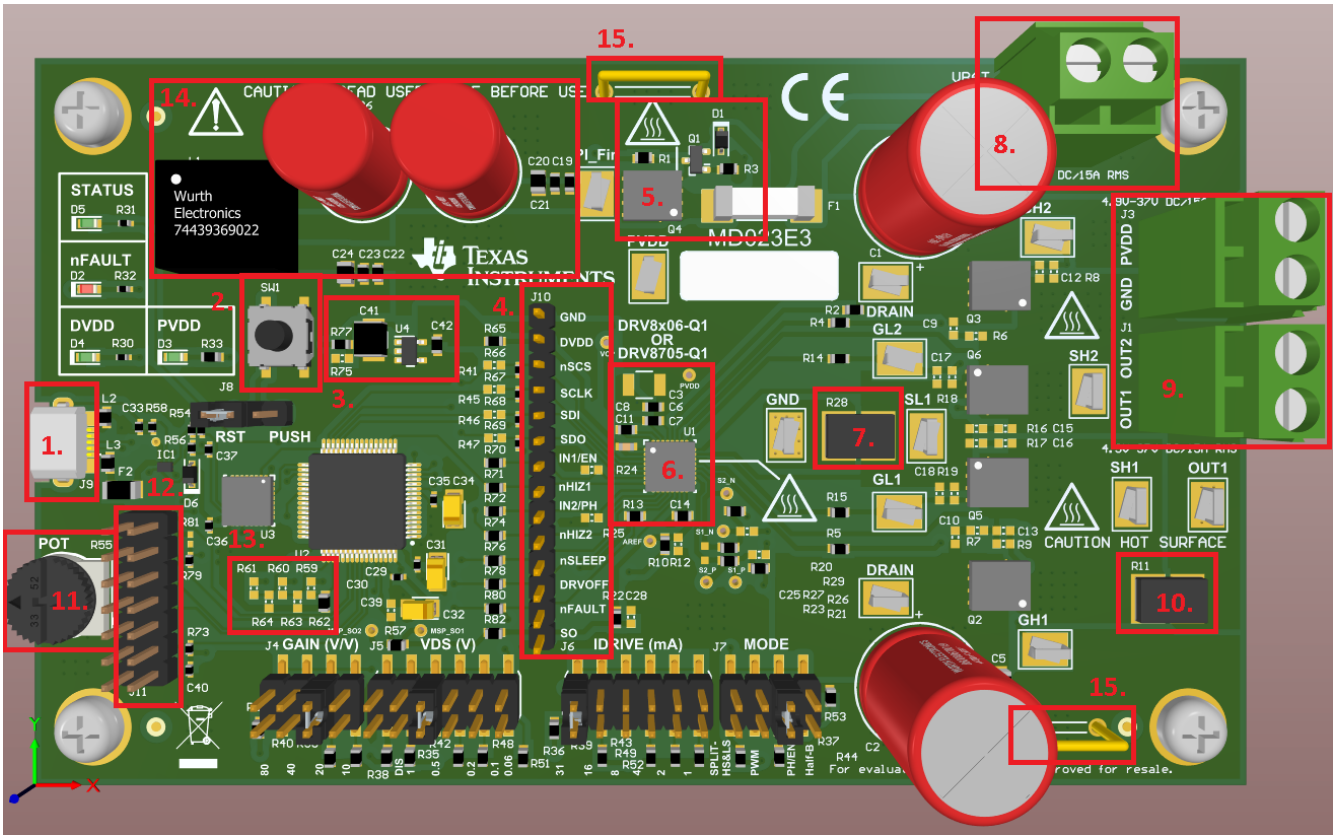

Figure 2-1. DRV8706S-Q1EVM with Highlighted Modules 1

Table 2-1. DRV8706S-Q1EVM with Highlighted Modules 1

Module Number & Name
1. USB Connector
2. RESET (default) / PUSH Button

Table 2-1. DRV8706S-Q1EVM with Highlighted Modules 1 (continued)

Module Number & Name
3. PVDD (default) / USB 5 V to 3.3 V Connector
4. 14 pin MCU to DRV header
5. Reverse Battery Protection Module
6. DRV and Necessary Components (minimum required space of DRV module)
7. Low Side Sense Resistor
8. Power Connector (VBAT and GND)
9. Load Connectors (OUT1 and OUT2, PVDD and GND) Note: OUT2 is not present the on DRV8106x-Q1EVM
10. In Line Sense Resistor
11. Potentiometer
12. MCU Programming Jumper Header for MSP-FET Tool
13. EVM variant identification resistors
14. PI Filter
15. GND Probing Shunts

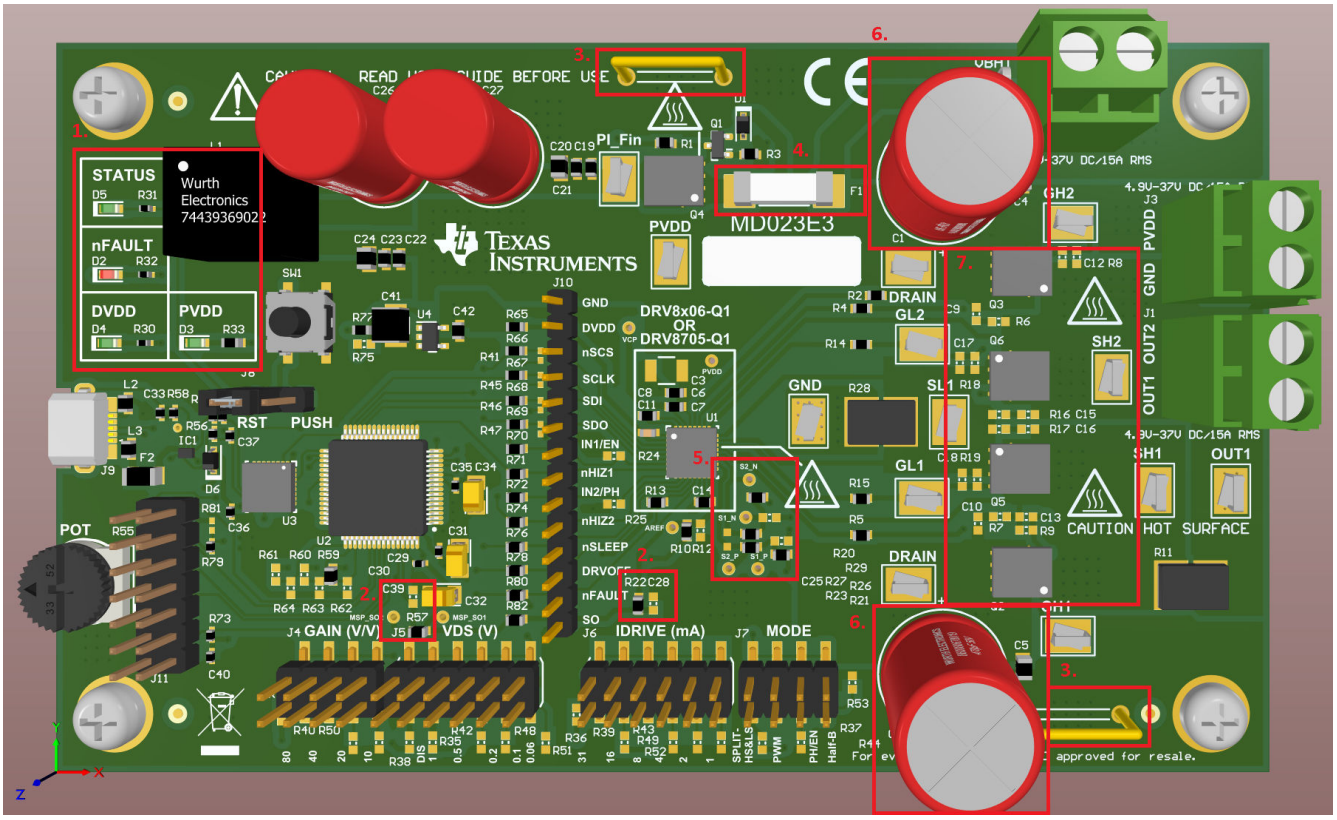

Figure 2-2. DRV8706S-Q1EVM with Highlighted Modules 2 (actual board is subject to change)

Table 2-2. DRV8706S-Q1EVM with Highlighted Modules 2

Module Number & Name
1. LEDs
2. SO RC Filter to MCU and to MCU to DRV Header
3. GND Probing Shunts
4. VBAT Fuse
5. SP and SN RC Filters to In Line and to Low Side Sense Resistors
6. Bulk Capacitors
7. FETs and RC Snubbers

The main power supply terminal (labeled VBAT) is located on the top edge of the EVM. VBAT includes a 20A fuse, a reverse polarity protection circuit and a PI filter to become PVDD, which reaches the motor driver and the FET stage. Digital power to the FTDI chip is provided through the USB's 5 V line. The LDO's power input is PVDD (default) or the USB 5 V line. The LDO's output, 3.3 V, provides power to the MSP430F2617, DVDD, AREF, and it is also the reference voltage of the MCU's ADC.

The power connector J2 is the correct connector for powering the EVM. Connector J3, which has pins PVDD and GND, is designed as one of two connectors for the load(s). Connecting EVM power here will bypass the fuse, reverse battery protection, and the PI filter. The EVM is not tested or designed for receiving power from J3.

The FET H-Bridge stage has RC snubber footprints for each FET's drain to source and gate to source connections. The motor driver's SH2 pin connects to the FETs and to OUT2 of the power connector. The motor driver's SH1 pin connects to the FETs and to the inline sense resistor to connect to OUT1. Finally, the FET stage allows the usage of a low side sense resistor.

The load connectors, one with OUT1 and OUT2 and the other to PVDD and GND, can be connected to one to two motors, inductors, other passive loads or to a latched relay coil. The OUT1 pin can drive one load and the OUT2 pin can drive a second load. If the load is connected to OUT1 and OUT2, bidirectional motor driving can be achieved. If more than one load is meant to be driven, one load can connect to OUT1 and to either PVDD or GND, while the other load can connect to OUT2 and to either PVDD or GND.

Depending on whether the EVM variant is inline or low side sensing, the inline or low side sense resistor will be utilized for SP and SN input, respectively. The sense resistors' two nodes connect to the motor driver's SP and SN pins through 0 ohm resistors. Depending on the sense resistor being utilized (it will have a resistance of 6 or 7 mOhms, depending on commercial availability during EVM manufacturing, while the other sense resistor will be 1 mOhm), the respective 0 ohm resistors connecting it back to the motor driver are populated and the other sense resistor's 0 ohm resistors are DNPed. SP and SN pins have RC filters that include those resistors and in both directions for filtering the input to the motor driver. The RC filter capacitors are not populated for SP, SN, and for SO. AREF of the sense amplifier is configured through a resistor to 3.3 V. The SO connects to an ADC pin of the MCU with an input filter to this pin.

Note

Both AREF and DVDD are tied together via a 0 ohm pull up resistor. AREF also has an unpopulated pull down resistor, making a voltage divider circuit for AREF with respect to DVDD. Therefore, AREF can be set to DVDD or to a smaller value.

There is a 0 ohm resistor tying DVDD (along with AREF) to the power pins of the MCU. The MCU pins are rated to 4.2 V max. Therefore, if evaluation is to be done at DVDD and AREF > 4.2 V with an external MCU, the 0 ohm resistor should not be populated to protect the on-board MCU.

Note

SO saturates to the AREF voltage value (3.3 V). Therefore, the MCU's ADC pin is protected since 3.3 V is less than the electrical specification maximum of the pin.

The MCU can be disconnected from the motor driver in order to drive the latter through an external controller by interfacing with the 14 pin header. To do so, remove the resistors between the MCU and the header that connects the MCU to the motor driver.

H variant EVM's (DRV8706H-Q1EVM, DRV8106H-Q1EVM & DRV8705H-Q1EVM) GAIN, VDS, IDRIVE, and MODE are configured via populating four jumper headers connected to those motor driver pins. Please, study the schematics and datasheet for configuration details.

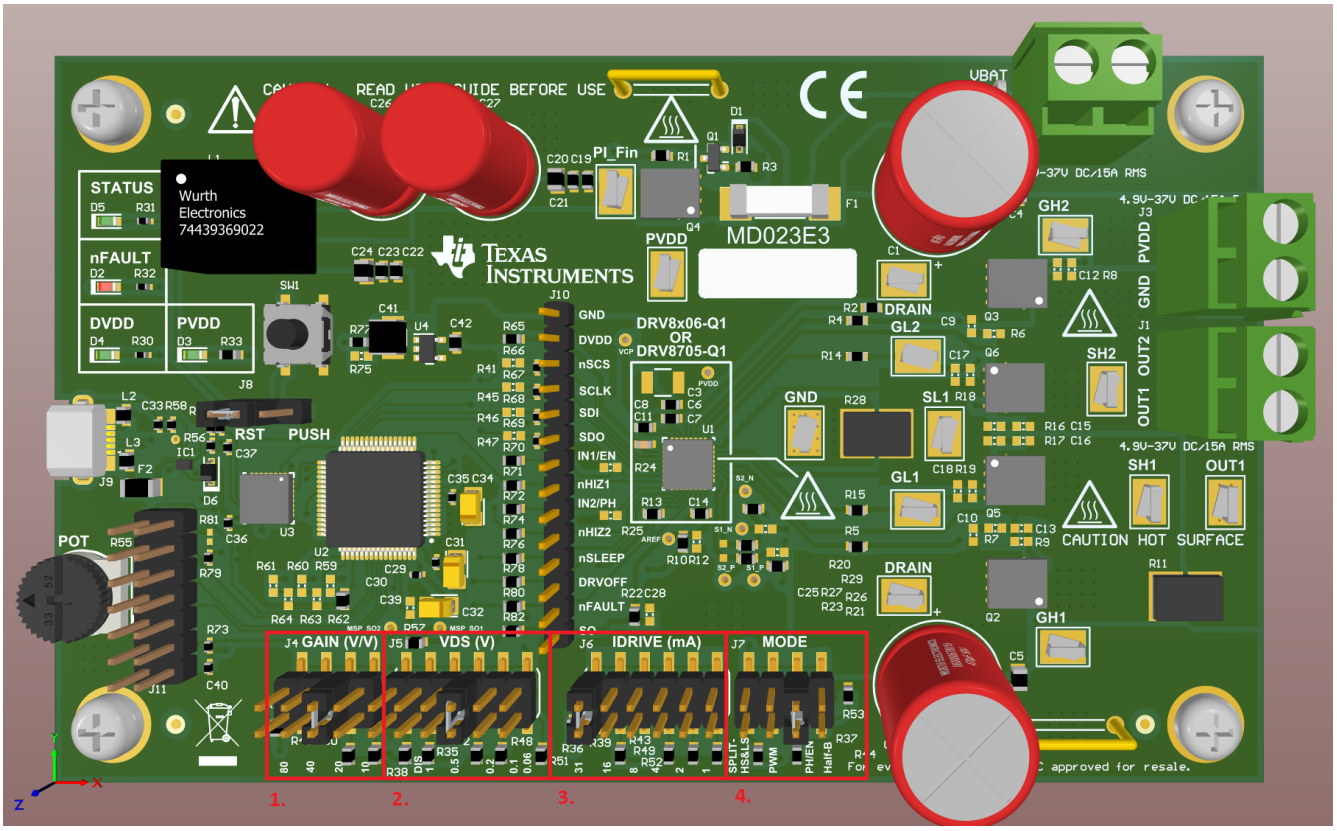

Figure 2-3. DRV8706H-Q1EVM Configuration Jumper Headers

Table 2-3. DRV8706S-Q1EVM with Highlighted Modules 3

Module Number & Name
1. GAIN (default set to 20 V/V)
2. VDS (default set to 0.5 V)
3. IDRIVE (default set to 31 mA/ 31 mA)
4. MODE (default set to PH/EN mode)

The MCU can be programmed with a MSP-FET tool through a jumper header. The programming can be done via the GUI or via Code Composer Studio. In both cases, the micro-USB cable must be connected to the EVM and to the PC, along with the MSP-FET connected to the EVM and to the PC. The MSP-FET tool can be purchased here.

Additionally, the MCU is connected to a potentiometer that interfaces to an ADC pin. The firmware, by default, does not utilize this pin. It is a resource that can be configured for customer modified firmware (for example PWM reference based on the potentiometer voltage). The reference voltage of this potentiometer is 3.3 V. The MCU also has an MCU Reset button, configured by default via a three pin header (pins 1, 2 shorted). Alternatively, this jumper can be moved to short pins 2, 3, and the button becomes a PUSH button for customer modified firmware use.

Finally, there are measurement resources and LED references. Ground shorting plugs across the board are included for ground references and test points for all signals can be found across the Half-Bridge stage. There are large voltage probing via holes for VCP, PVDD, SP, and SN before and after the RC filter, and SO before and after the 14 pin header. The LEDs on the board are Status, PVDD, DVDD and nFAULT.

Table 2-4. Voltage Probing Via Holes

Driver in Name	Silk Name	Note
VCP	VCP	
PVDD	PVDD	

Table 2-4. Voltage Probing Via Holes (continued)

Driver in Name	Silk Name	Note
AREF	AREF	
SP	S1_P	Before RC filter
SP	S2_P	After RC filter
SN	S1_N	Before RC filter
SN	S2_N	After RC filter
SO	SO_1	Before the RC filter to the 14 pin header
SO	SO_2	Before the RC filter to the 14 pin header
SO	MSP_SO1	After the RC filter to the MCU
SO	MSP_SO2	After the RC filter to the 14 MCU

2.2 Hardware Connections Overview for DRV8714x-Q1EVM (40-pin RHA package) 4-channel smart gate driver

The major blocks of your EVM includes the DRV8714x-Q1 4-channel smart gate driver in the 6x6mm 40-pin RHA package, MSP430F2617 microcontroller (MCU), TPS7B6933 3.3-V LDO regulator, and the USB communication interface. This EVM is a close relative the to DRV8714S-Q1EVM and DRV8718S-Q1EVM, however has been redesigned around the smaller 6mm x 6mm 40-pin package (RHA) and supports the hardware configuration interface for those that do not need or desire SPI control and configuration, advanced gate drive control and fault/ diagnostic information.

The DRV8714H-Q1EVM is designed for an input supply from 4.9 to 37 V through the power connector and up to 30A RMS, 40-A peak drive current through the load connectors.

The MCU communicates with the GUI to control the DRV8714-Q1 device.

Note

On S variants, PVDD overvoltage is enabled and as a latched fault. To change the setting or the voltage magnitude the PVDD_OV trips at, refer to the datasheet for more information on register configuration settings.

On H variants, PVDD_OV is disabled.

2.2.1 EVM Module Details

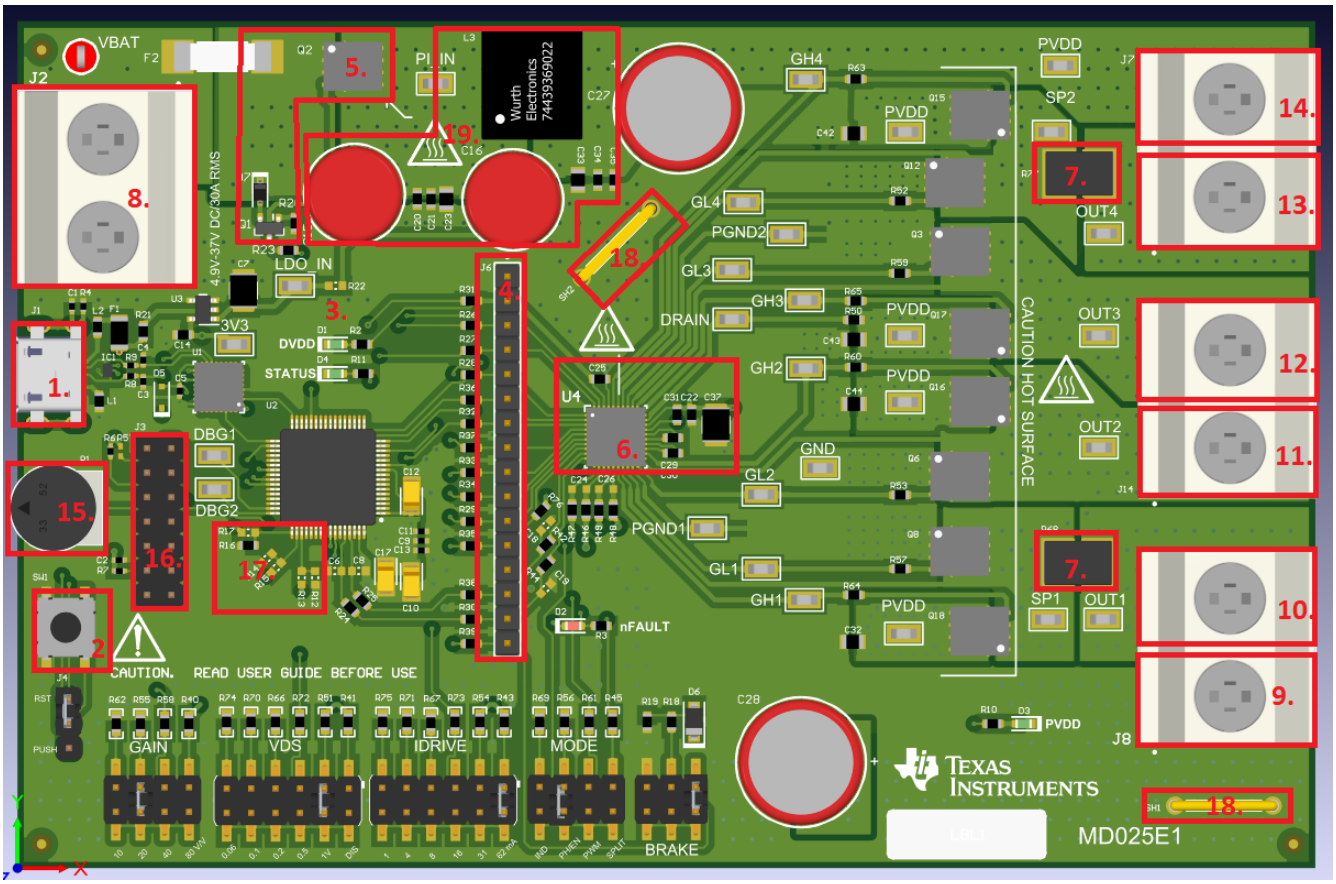

Figure 2-4. DRV8714-Q1EVM (RHA) with Highlighted Modules 1 (actual board is subject to change)

Table 2-5. DRV8714-Q1EVM (RHA) with Highlighted Modules 1

Module Number & Name
1. USB Connector
2. RESET (default) / PUSH Button
3. PVDD (default) / USB 5 V to 3.3 V Connector
4. 14 pin MCU to DRV header
5. Reverse Battery Protection Module
6. DRV and Necessary Components (minimum required space of DRV module)
7. Inline Sense Resistors (OUT1 and OUT4)
8. Power Connector (VBAT and GND)
9. Load Connector (GND)
10. Load Connector (OUT1)
11. Load Connector (OUT2)
12. Load Connector (OUT3)
13. Load Connector (OUT4)
14. Load Connector (PVDD)
15. Potentiometer
16. MCU Programming Jumper Header for MSP-FET Tool
17. EVM variant identification resistors
18. GND Probing Shunts
19. PI Filter

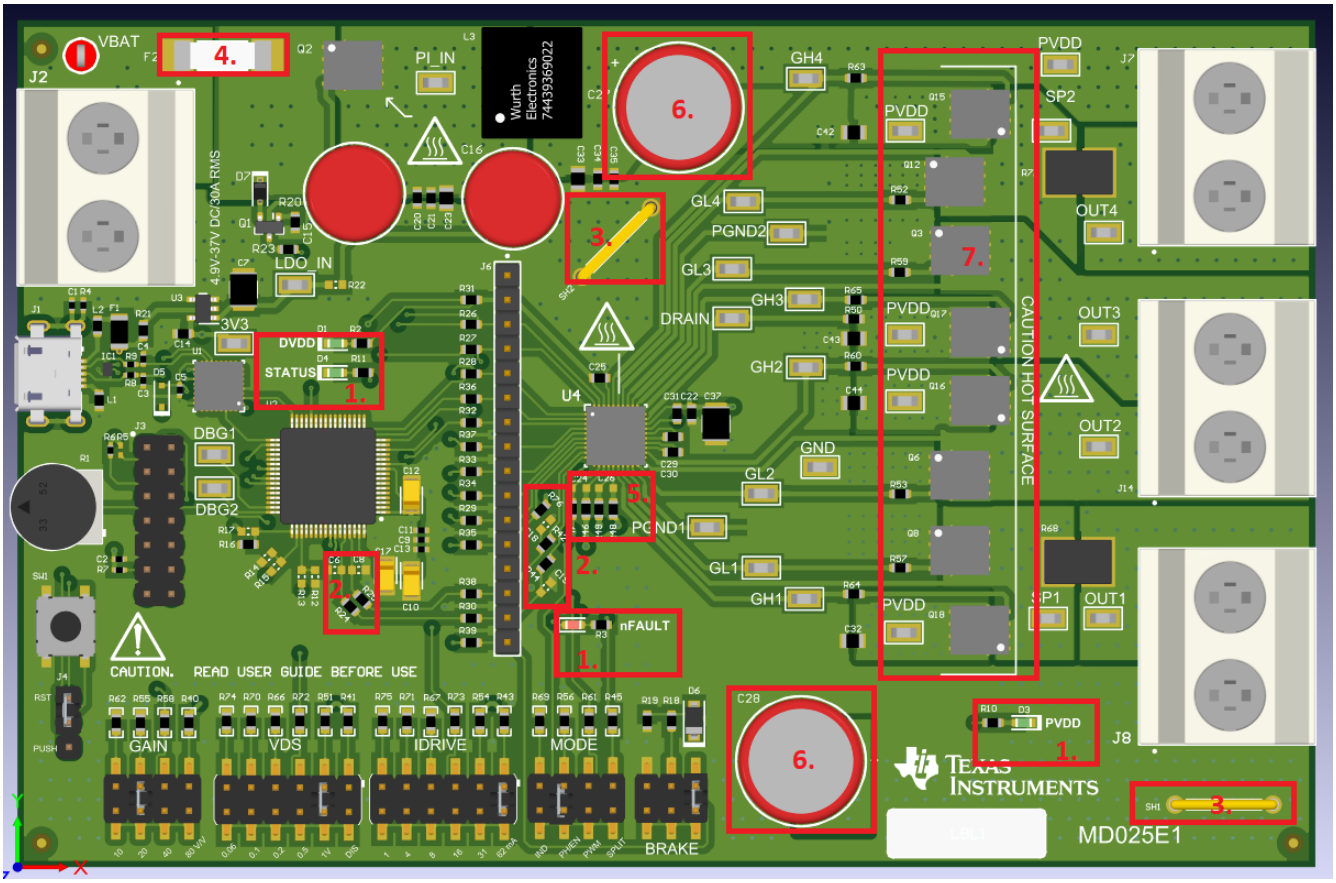

Figure 2-5. DRV8714-Q1EVM (RHA) with Highlighted Modules 2 (actual board is subject to change)

Table 2-6. DRV8714-Q1EVM (RHA) with Highlighted Modules 2

Module Number & Name
1. LEDs
2. SO RC Filter to MCU and to MCU to DRV Header
3. GND Probing Shunts
4. VBAT Fuse
5. SP and SN RC Filters to In Line Sense Resistors
6. Bulk Capacitors
7. FETs and RC Snubbers

The power connector is where the supply voltage connects to. VBAT goes through 20 A fuse, a reverse battery protection circuit and a PI filter to become PVDD, which reaches the motor driver and the FET stage. Digital power to the FTDI chip is provided through the USB's 5 V line. The LDO's power input is PVDD (default) or the USB 5 V line. The LDO's output, 3.3 V, provides power to the MSP430F2617, DVDD, AREF, and it is also the reference voltage of the MCU's ADC.

> The power connector J2 is the correct connector for powering the EVM. Connector J3, which has pins PVDD and GND, is designed as one of two connectors for the load(s). Connecting EVM power here will bypass the fuse, reverse battery protection, and the PI filter. The EVM is not tested or designed for receiving power from J7 and J8.

The FET H-Bridge stage has RC snubber footprints for each FET's drain to source and gate to source connections.

OUTx, PVDD and GND on the high-current load connectors can be connected to a combination of motors (four unidirectional or two bidirectional), inductors, other passive loads or latched relay coils. Bidirectional loads should be connected across OUT1, OUT2 and OUT3, OUT4. High-side or low-side switched loads can be connected to the OUTx terminals and either PVDD or GND.

The EVM has inline sense resistors installed on the OUT1 and OUT4 channels. The installed sense resistor will have a value between 6 to 7 mOhms, depending on commercial availability during EVM manufacturing (the GUI has an option to set this value). SP and SN pins have RC filters that include those resistors and in both directions for filtering the input to the motor driver. The RC filter capacitors are not populated for SP, SN, and for SO. AREF of the sense amplifier is configured through a resistor to 3.3 V. The SO connects to an ADC pin of the MCU with an input filter to this pin.

Note

Both AREF and DVDD are tied together via a 0 ohm pull up resistor. AREF also has an unpopulated pull down resistor, making a voltage divider circuit for AREF with respect to DVDD. Therefore, AREF can be set to DVDD or to a smaller value.

There is a 0 ohm resistor tying DVDD (along with AREF) to the power pins of the MCU. The MCU pins are rated to 4.2 V max. Therefore, if evaluation is to be done at DVDD and AREF > 4.2 V with an external MCU, the 0 ohm resistor should not be populated to protect the on-board MCU.

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SO saturates to the AREF voltage value (3.3 V). Therefore, the MCU's ADC pin is protected since 3.3 V is less than the electrical specification maximum of the pin

The MCU can be disconnected from the motor driver in order to drive the latter through an external controller by interfacing with the 14 pin header. To do so, remove the resistors between the MCU and the header that connects the MCU to the motor driver.

H variant EVM's (DRV8714H-Q1EVM) GAIN, VDS, IDRIVE, and MODE are configured via populating four jumper headers connected to those motor driver pins. Please, study the schematics and datasheet for configuration details.

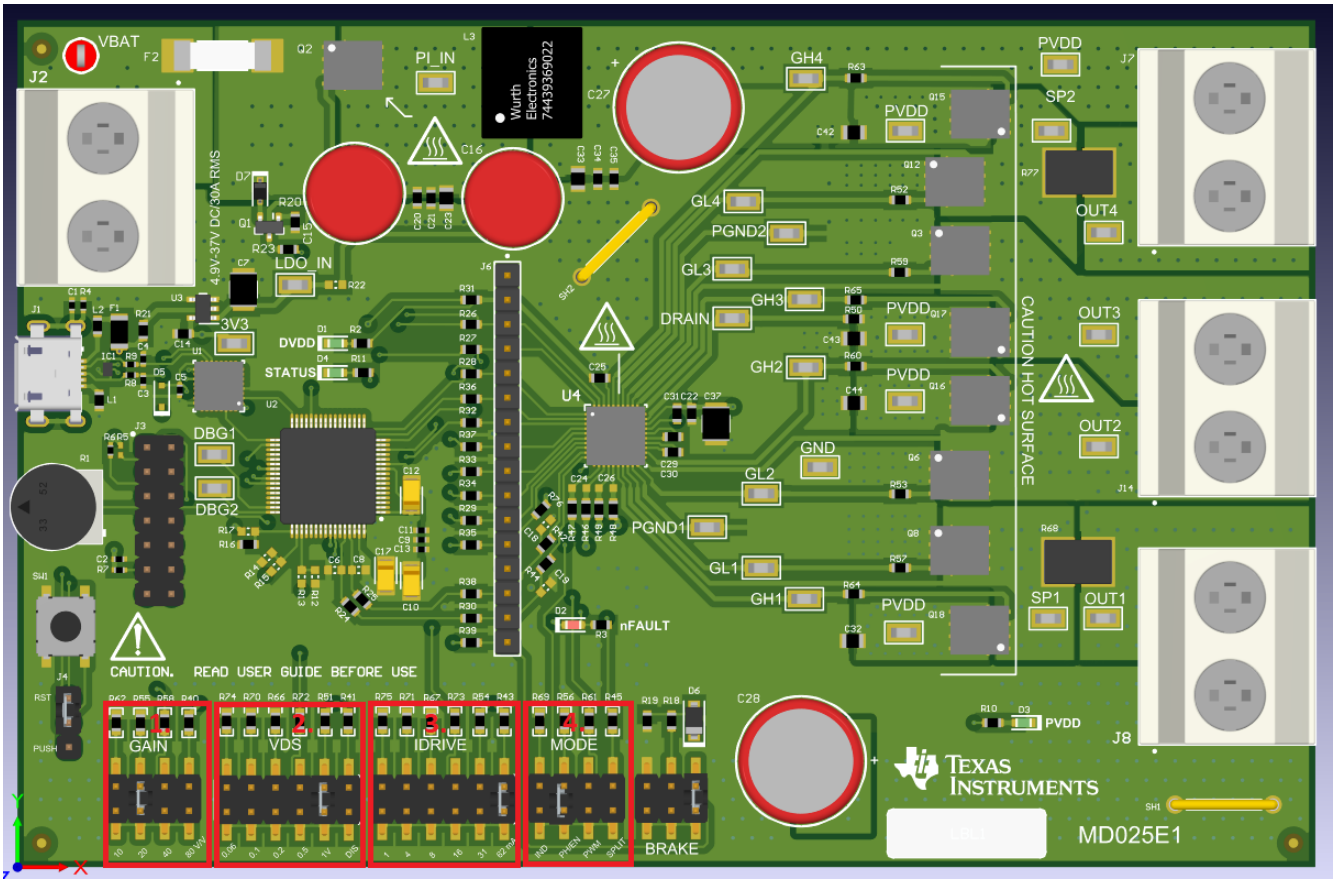

Figure 2-6. DRV8714H-Q1EVM Configuration Jumper Headers (actual board is subject to change)

Table 2-7. DRV8714H-Q1EVM with Highlighted Modules 3

Module Number & Name
1. GAIN (default set to 20 V/V)
2. VDS (default set to 1.0 V)
3. IDRIVE (default set to 62 mA/ 62 mA)
4. MODE (default set to PH/EN mode)

The MCU can be programmed with a MSP-FET tool through a jumper header. The programming can be done via the GUI or via Code Composer Studio. In both cases, the micro-USB cable must be connected to the EVM and to the PC, along with the MSP-FET connected to the EVM and to the PC. The MSP-FET tool can be purchased here

Additionally, the MCU is connected to a potentiometer that interfaces to an ADC pin. The firmware, by default, does not utilize this pin. It is a resource that can be configured for customer modified firmware (for example PWM reference based on the potentiometer voltage). The reference voltage of this potentiometer is 3.3 V. The MCU also has an MCU Reset button, and it is configured by default via a three-pin header, to the Reset pin of the MCU. If three pin header jumper is placed in its other two pin configuration, the button becomes a PUSH button for customer modified firmware use.

2.3 Hardware Connections Overview for DRV8714S-Q1EVM and DRV8718S-Q1EVM (56-pin RVJ package) 4-channel and 8-channel Smart Gate Drivers

The major blocks of your EVM includes the DRV8714S-Q1 or DRV8718S-Q1 multichannel smart gate driver in the 8x8mm 56-pin RVJ package, MSP430F2617 microcontroller (MCU), TPS7B6933 3.3-V LDO regulator, and the USB communication interface.

The DRV871x-Q1EVM is designed for an input supply from 4.9 to 37 V through the power connector and up to 30A RMS, 40-A peak drive current through the load connectors.

The MCU communicates with the GUI to control the DRV871x-Q1 device.

Note

PVDD overvoltage is enabled and as a latched fault. To change the setting or the voltage magnitude the PVDD_OV trips at, refer to the datasheet for more information on register configuration settings.

2.3.1 EVM Module Details

Note: the following figures apply to both DRV8718S-Q1EVM and DRV8714S-Q1EVM. The DRV8714S-Q1EVM part number has been omitted for simplicity.

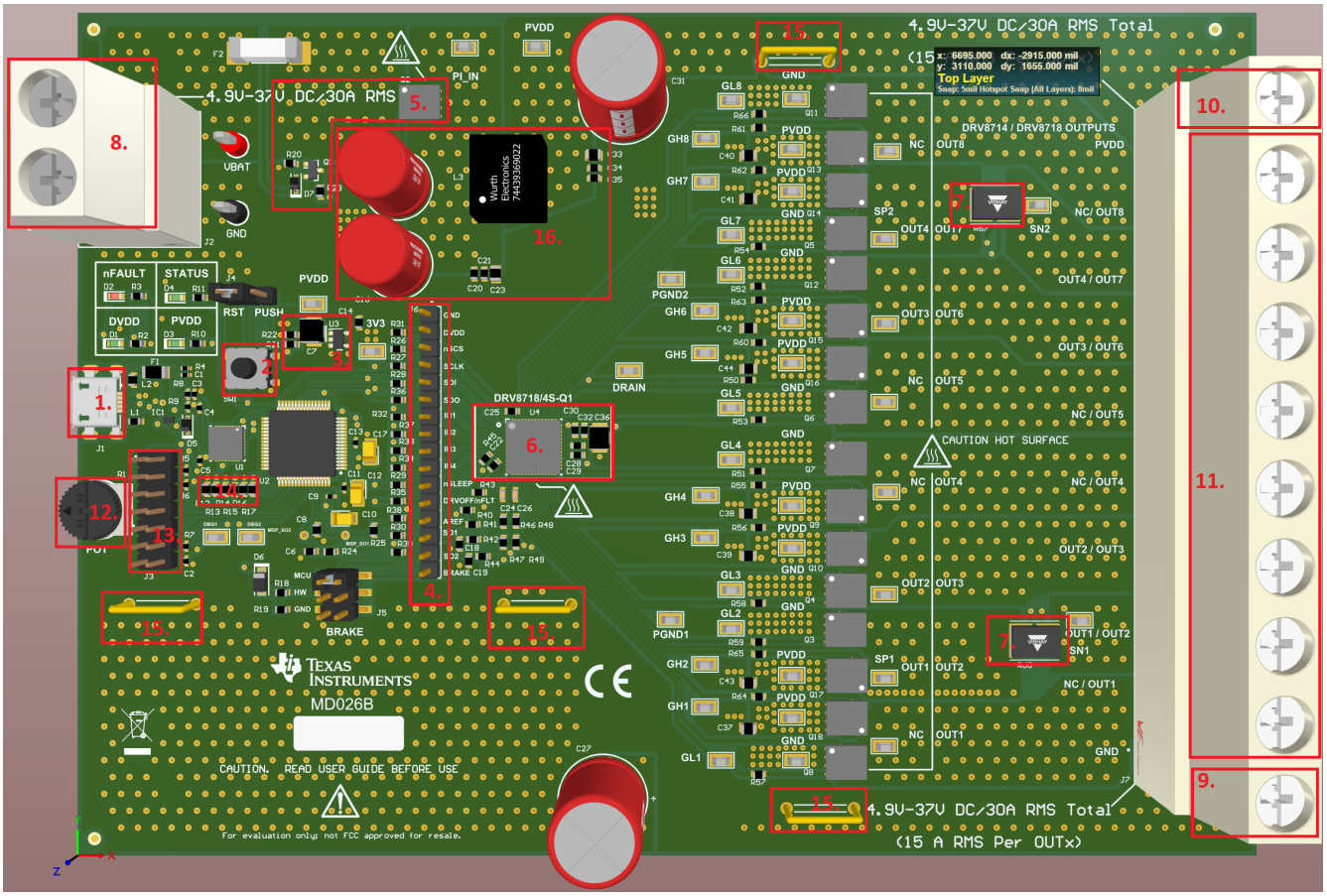

Figure 2-7. DRV8718S-Q1EVM (RVJ) with Highlighted Modules 1 (actual board subject to change)

Table 2-8. DRV8718S-Q1EVM (RVJ) with Highlighted Modules 1

Module Number & Name
1. USB Connector
2. RESET (default) / PUSH Button
3. PVDD (default) / USB 5 V to 3.3 V Connector
4. 14 pin MCU to DRV header
5. Reverse Battery Protection Module
6. DRV and Necessary Components (minimum required space of DRV module)
7. Inline Sense Resistors (DRV8714S-Q1EVM: OUT1 and OUT4; DRV8718S-Q1EVM: OUT2 and OUT7)
8. Power Connector (VBAT and GND)
9. Load Connector (GND)

Table 2-8. DRV8718S-Q1EVM (RVJ) with Highlighted Modules 1 (continued)

Module Number & Name
10. Load Connector (PVDD)
11. Load Connectors (OUTx)
12. Potentiometer
13. MCU Programming Jumper Header for MSP-FET Tool
14. EVM variant identification resistors
15. GND Probing Shunts
16. PI Filter

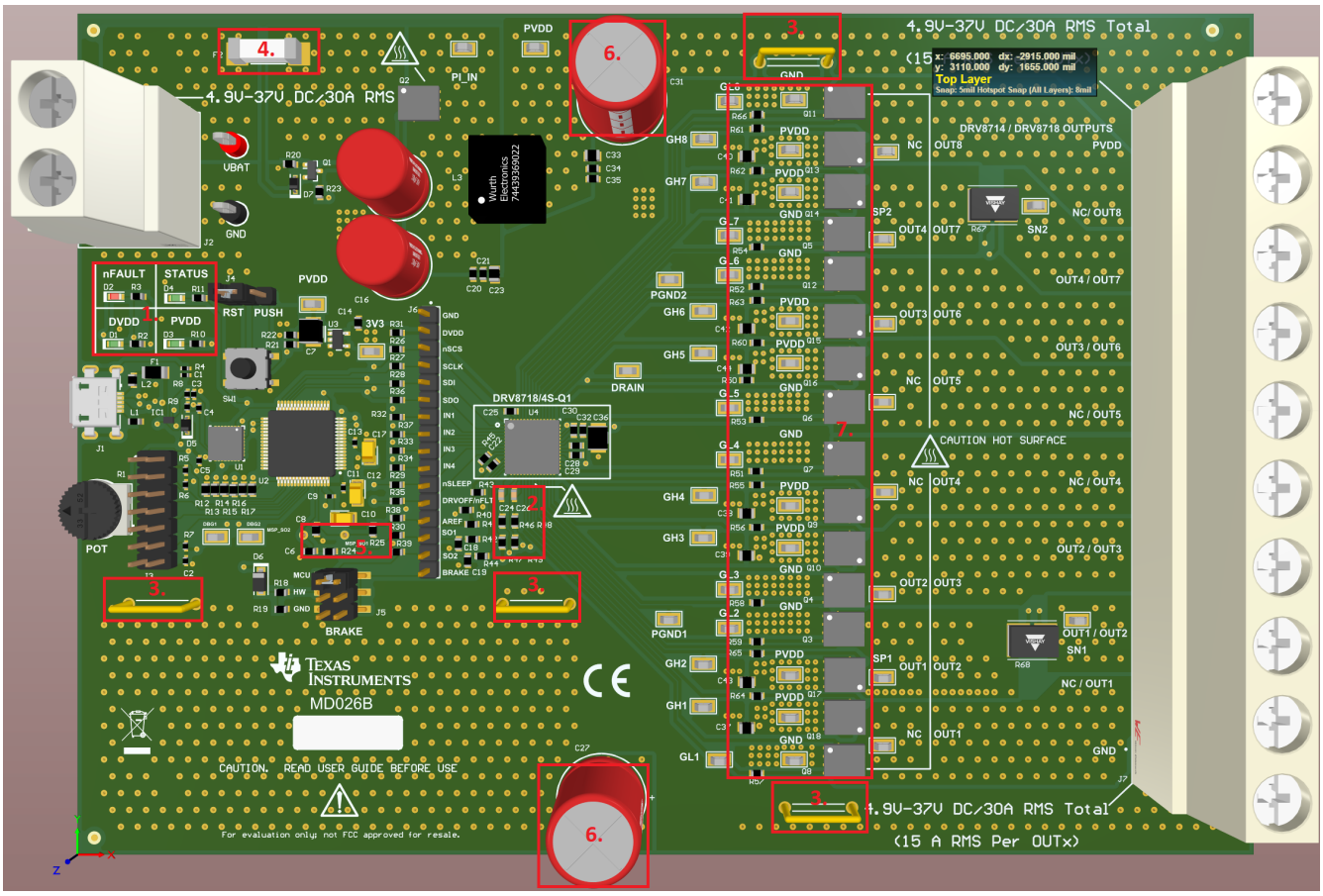

Figure 2-8. DRV8718S-Q1EVM (RVJ) with Highlighted Modules 2 (actual board subject to change)

Table 2-9. DRV8718S-Q1EVM (RVJ) with Highlighted Modules 2

Module Number & Name
1. LEDs
2. SO RC Filter to MCU and to MCU to DRV Header
3. GND Probing Shunts
4. VBAT Fuse
5. SP and SN RC Filters to In Line Sense Resistors
6. Bulk Capacitors
7. FETs and RC Snubbers (Note: components related to unmapped DRV8714S-Q1 channels are DNP)

The power connector is where the supply voltage connects to. VBAT goes through 20 A fuse, a reverse battery protection circuit and a PI filter to become PVDD, which reaches the motor driver and the FET stage. Digital power to the FTDI chip is provided through the USB's 5 V line. The LDO's power input is PVDD (default) or the

USB 5 V line. The LDO's output, 3.3 V, provides power to the MSP430F2617, DVDD, AREF, and it is also the reference voltage of the MCU's ADC.

The power connector J2 is the correct connector for powering the EVM. Connector J7, which has pins PVDD and GND, is designed as one of two connectors for the load(s). Connecting EVM power here will bypass the fuse, reverse battery protection, and the PI filter. The EVM is not tested or designed for receiving power from J7.

The FET H-Bridge stage has RC snubber footprints for each FET's drain to source and gate to source connections.

OUTx, PVDD and GND on the high-current load connectors can be connected to a combination of motors (unidirectional or bidirectional), inductors, other passive loads or latched relay coils. Bidirectional loads should be connected across adjacent pairs (e.g. OUT1, OUT2 and OUT3, OUT4, etc). For your own designs that include assembly variants with either DRV8714x-Q1 or DRV8718x-Q1 populated, refer to the device pinout in the datasheet to understand the channel mapping. High-side or low-side switched loads can be connected to the OUTx terminals and either PVDD or GND.

The EVM has inline sense resistors installed on OUT1 and OUT4 channels for DRV8714S-Q1EVM and OUT2 and OUT7 for DRV8718S-E1EVM. Note these are physically routed back to the same OUTx pin on the gate driver, however electrically these are different channels (and correspondingly different registers). This illustrates the cautionary note in the previous paragraph about understanding the channel mapping. The installed sense resistor will have a value between 6 to 7 mOhms, depending on commercial availability during EVM manufacturing (the GUI has an option to set this value). SP and SN pins have RC filters that include those resistors and in both directions for filtering the input to the motor driver. The RC filter capacitors are not populated for SP, SN, and for SO. AREF of the sense amplifier is configured through a resistor to 3.3 V. The SO connects to an ADC pin of the MCU with an input filter to this pin.

Note

Both AREF and DVDD are tied together via a 0 ohm pull up resistor. AREF also has an unpopulated pull down resistor, making a voltage divider circuit for AREF with respect to DVDD. Therefore, AREF can be set to DVDD or to a smaller value.

There is a 0 ohm resistor tying DVDD (along with AREF) to the power pins of the MCU. The MCU pins are rated to 4.2 V max. Therefore, if evaluation is to be done at DVDD and AREF > 4.2 V with an external MCU, the 0 ohm resistor should not be populated to protect the on-board MCU.

Note

SO saturates to the AREF voltage value (3.3 V). Therefore, the MCU's ADC pin is protected since 3.3 V is less than the electrical specification maximum of the pin.

The MCU can be disconnected from the motor driver in order to drive the latter through an external controller by interfacing with the 14 pin header. To do so, remove the resistors between the MCU and the header that connects the MCU to the motor driver.

The MCU can be programmed with a MSP-FET tool through a jumper header. The programming can be done via the GUI or via Code Composer Studio. In both cases, the micro-USB cable must be connected to the EVM and to the PC, along with the MSP-FET connected to the EVM and to the PC. The MSP-FET tool can be purchased here

Additionally, the MCU is connected to a potentiometer that interfaces to an ADC pin. The firmware, by default, does not utilize this pin. It is a resource that can be configured for customer modified firmware (for example PWM reference based on the potentiometer voltage). The reference voltage of this potentiometer is 3.3 V.

MCU also has an MCU Reset button, and it is configured by default via a three-pin header, to the Reset pin of the MCU. If three pin header jumper is placed in its other two pin configuration, the button becomes a PUSH button for customer modified firmware use.

Finally, there are measurement resources and LED references. Ground shorting plugs across the board are included for ground references and test points for all signals can be found across the Half-Bridge stage. There are large voltage probing via holes for VCP, PVDD, SP, and SN before and after the RC filter, and SO before and after the 14 pin header. The LEDs on the board are Status, PVDD, DVDD and nFAULT.

Table 2-10. Fabricated Test Point Via Locations

Driver in Name	Silk Name	Note
VCP	VCP	
PVDD	PVDD	
AREF	AREF	
SP	S1_P	Before RC filter
SP	S2_P	After RC filter
SN	S1_N	Before RC filter
SN	S2_N	After RC filter
SO	SO_1	Before the RC filter to the 14 pin header
SO	SO_2	Before the RC filter to the 14 pin header
SO	MSP_SO1	After the RC filter to the MCU
SO	MSP_SO2	After the RC filter to the MCU

2.4 Running the EVM

1. Connect the power supply to the J2 connector and set it to the operational voltage the evaluation will be conducted at (4.9 V to 37 V DC).
2. Attach zero motor/loads, or one to multiple brushed DC motors or resistive/inductive loads to the correct output connector pins PVDD, GND, OUT1, and/or OUT2.
3. Enable the power supply.
4. Connect the micro-USB cable from the EVM to the PC.

3 GUI Application

The GUI is used to control the DRV8706x-Q1EVM, DRV8106x-Q1EVM, DRV8705x-Q1EVM, DRV8714x-Q1EVM, & DRV8718x-Q1EVM through USB commands. The commands are sent from the computer to the FTDI FT233RL device, which converts USB commands to UART commands. The UART commands are received by the MSP430F2617 MCU.

Note that the GUI works with GUI Composer Runtime version v8 or greater. The Runtime will be downloaded automatically during the installation process.

3.1 Installation

The links are provided below to run the EVM control GUI from a Chrome-based web browser, or the offline installer. These links are also provided in the EVM tool folder.

Launching the GUI from your Chrome-based browser is a single step:

1. In a Chrome-based browser, open this URL to launch the latest version of the GUI: https://dev.ti.com/gallery/view/MotorDriversBSM/DRV87xx_DRV8106-Q1EVM-GUI

If you are looking for a specific version of the GUI, or the latest offline installer, visit the following URL and select the desired version:

https://dev.ti.com/gallery/info/MotorDriversBSM/DRV87xx_DRV8106-Q1EVM-GUI

Follow these steps to install the GUI application to the computer:

1. Extract the *DRV87xx_DRV8106-Q1EVM-GUIl*_x.y.z_installer_win zip file's contents. The x.y.z values shown may change as the GUI is updated.
2. In the newly extracted folder, double click on the *DRV87xx_DRV8106-Q1EVM-GUI-y.y.y.setup-win_8.0.0.exe* file.
3. Click the *Next* button in the *Setup - DRV87xx_DRV8106-Q1EVM-GUI Window* to continue.
4. *Review* the *license agreement*.
5. Click the *I accept the agreement* radio button if accepted and then click the *Next* button.
6. Select the installation directory. TI recommends using the *default installation directory*. Click the *Next* button when the directory is determined.
7. If another version of the GUI (or the same version) is installed, the installation process will prompt for the new installation. Select *Yes* or *No* to continue or finish the installation. If *Yes* is clicked, the installed GUI will be uninstalled, along with the GUI Composer Runtime version installed.
8. Click the *Next* button in the *Select Installation Folders* window to begin the installation.
9. In the *GUI Composer Runtime* window, be default *Download from Web* is selected. If PC the GUI is being installed on has a Runtime executable on it, it can be selected from the *Install from file* option. Click *Next* when finished determining the method to install the Runtime.
10. The GUI installation process will begin the Runtime and GUI installations, sequentially and without prompt.
11. In the *Completing the DRV87xx_DRV8106-Q1EVM-GUI Setup Wizard* window, checkmark the shortcuts desired, the read me and launching the GUI individually after finishing the installation.

To launch the GUI from the desktop, search for DRV87xx_DRV8106-Q1EVM-GUI on the start menu search bar and click on the DRV87xx_DRV8106-Q1EVM-GUI search hit or, if the creation of the shortcut(s) was selected, click on the GUI shortcut on the desktop or navigate to the Windows Start Menu shortcut and click *All Programs*. Navigate to the Texas Instruments folder and select the DRV87xx_DRV8106-Q1EVM-GUI icon.

As for a GUI guide, refer to the *DRV87xx-Q1EVM & DRV8106-Q1EVM GUI User's Guide*.

4 REACH

REACH Compliance

In compliance with the Article 33 provision of the EU REACH regulation we are notifying you that this EVM includes component(s) containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are:

Component Manufacturer	Component type	Component part number	SVHC Substance	SVHC CAS (when available)
Littelfuse	Power fuse	0463020.ER	Lead	7439-92-1

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