TEXAS INSTRUMENTS

# APPLICATION NOTE
# BUILDING A QAM MODULATOR USING A GC2011 DIGITAL FILTER CHIP

October 6, 1994

## 1.0 INTRODUCTION

This report describes how one can use the GC2011 Digital Filter chip to build digital modulators for most BPSK, QPSK, and QAM radio signals. The modulator described here will accept a data stream with a symbol rate equal to B (standing for baud) and will output a modulated QAM signal centered at an IF frequency equal to the symbol rate or twice the symbol rate (B or 2B). A typical application would be a 5 MBaud (5 million symbols per second) 64 QAM modulator for a digital television transmitter. The modulator will Nyquist filter[1] the QAM signal, mix it up to be centered at either 5 MHz or 10 MHz and output an analog signal ready to be mixed up to a final carrier frequency.

## 2.0 THE BASIC MODULATOR

The basic functions of a QAM modulator are shown in Figure 1 below:

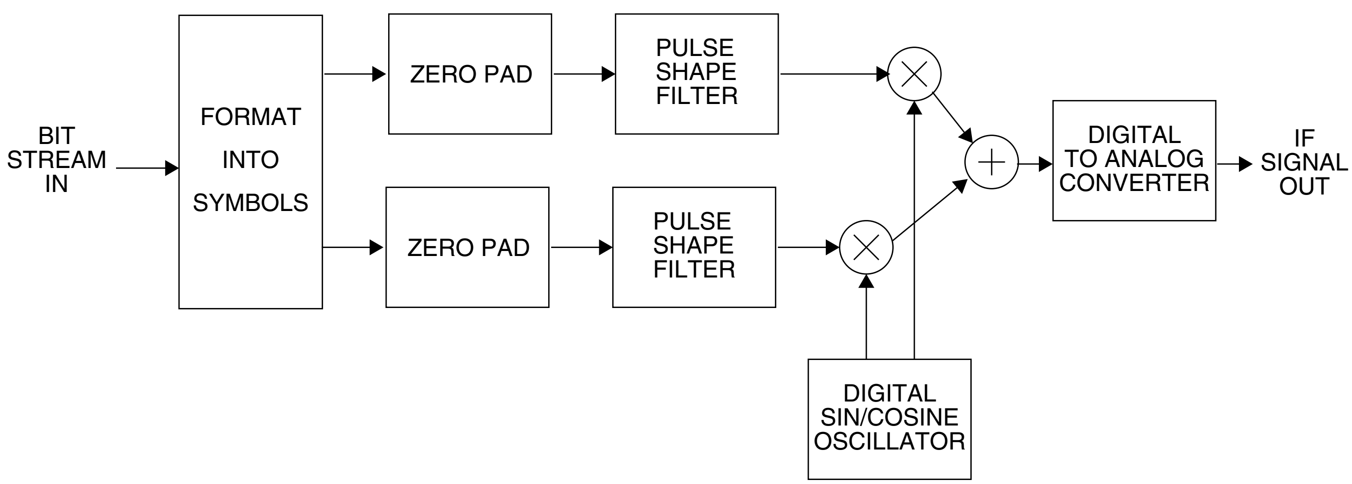


Figure 1. BASIC MODULATOR

The bit stream is formatted into symbols consisting of I and Q words. A QPSK symbol uses a pair of input bits to identify each symbol. The first bit in the pair selects ±1 for the I word and the second bit selects ±1 for the Q word. A 16 QAM symbol uses four input bits per symbol. Two bits select ±1 or ±3 for the I word and 2 bits select ±1 or ±3 for the Q words. A 64 QAM symbol uses 6 input bits per symbol, 3 bits

1. The transmitter's pulse shaping filter is called a Nyquist filter.

for the I and 3 bits for the Q. The I and Q values for 64 QAM are ±1, ±3, ± 5 and ±7. A 256 QAM signal uses 8 input bits per symbol and selects between 16 values of I and 16 values of Q.

The symbols are zero padded to generate a data stream at the desired sample rate for the final digital to analog converter (DAC). The desired sample rate is a function of the IF signal frequency and its bandwidth. If the excess bandwidth of the Nyquist filter is $\alpha$, and the IF signal's center frequency is F, then the DAC frequency must be at least twice (F + (1+$\alpha$)B/2). This means that the DAC frequency must be greater than (2F + (1+$\alpha$)B). If the IF is centered at the symbol rate B, then a DAC frequency of 4B is adequate. If the IF center frequency is 2B, then a DAC frequency of 8B is adequate. If the DAC frequency is chosen as 4B, then the zero pad circuit must insert 3 zeroes between each symbol. If the DAC frequency is 8B, then 7 zeroes must be inserted between each symbol.

The pulse shape filter is typically the raised cosine pulse defined as:

$$p(t) = \left(\frac{\sin\left(\frac{\pi t}{2}\right)}{\frac{\pi t}{T}}\right)\left(\frac{\cos\left(\frac{\alpha\pi t}{T}\right)}{1-\left(\frac{2\alpha t}{T}\right)^2}\right) \qquad \text{EQ 2.0}$$

Where $\alpha$ sets the excess bandwidth of the pulse and $T$ is the symbol time spacing (B = 1/$T$). If the DAC frequency is 4B, then the pulse filter will use the impulse response h(k) = p(kT/4) for k= -N to +N. The length of the filter is 2N+1. The value of N, and hence the length of the filter, is set so that the value of p(t) in EQ 2.0 is sufficiently close to zero for k > N. If the DAC frequency is 8B, then h(k) = p(kT/8). Typically N is less than 30 for a DAC frequency of 4B and is less than 60 for a DAC frequency of 8B.

The I/Q signal coming from the pulse shape filters is mixed up to the desired IF center frequency as shown in Figure 1. The real part of the mixer output is retained and sent to the DAC. The DAC output is smoothed by a lowpass filter. The lowpass filter's passband extends from 0 to (F + (1+$\alpha$)B/2) and its stopband starts at $F_{DAC}$ minus (F + (1+$\alpha$)B/2).

If the DAC frequency is 4B and the IF is B, or if the DAC frequency is 8B and the IF is 2B, then the mixer frequency is $e^{j(\pi/4)n}$ which is simply the sequence (1, j, -1, -j,...). This means that the mixer only needs to make sign changes and to multiplex between the I and Q filter outputs.

## 3.0 THE GC2011 FILTER CHIP

The GC2011 Filter chip has a complex to real upconvert mode. In this mode the chip accepts I and Q input samples at half the clock rate, inserts zeroes between every input to double the rate, filters the I and Q signals with 127 tap filters, mixes the signal up using the sequence (1, j, -1, -j...), and outputs real data at the clock rate. The real signal will be centered at one-fourth the clock rate. This mode of the GC2011 Filter chip can be used in the QAM modulator as described in the next Section.

## 4.0 THE SUGGESTED ARCHITECTURE

A PSK or QAM modulator architecture using the GC2011 chip is shown in Figure 2.

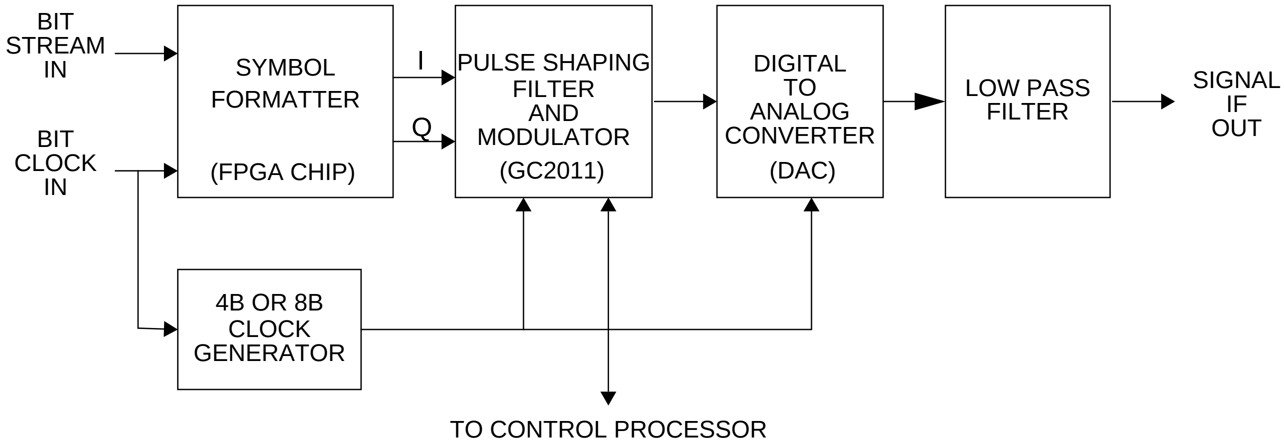


Figure 2. THE GC2011 MODULATOR

In this architecture the Symbol formatter chip accepts the input bit stream, formats it into symbols, and generates a symbol stream which has been "zero padded" to be at a sample rate which is equal to 2B or 4B. If the IF signal is to be centered at B, then the formatter should output samples at a 2B rate by inserting a zero between each symbol. If the IF signal is to be centered at 2B, then the formatter should insert three zeroes between each symbol.

The clock generator must synthesize a clock for the GC2011 chip and the DAC chip which is at either 4B or 8B, depending upon whether the desired IF is B or 2B.

The GC2011 chip, operating in the complex to real upconvert mode, accepts the zero padded input symbols, zero pads them by another factor of two, filters the I/Q stream by the pulse shaping filter, mixes the data up by one-fourth the clock rate, and then outputs a real data stream at the clock rate. If the chip is clocked at 4B, then the real output will be centered at an IF equal to B, if the clock rate is 8B, then the IF will be 2B.

The GC2011's output is converted to an analog signal by the DAC and then low pass filtered. If the IF is B, then the low pass filter has a passband extending from 0 to $(B + (1+\alpha)B/2)$ and a stopband starting at $(3B - (1+\alpha)B/2)$. If the IF is 2B, then the low pass filter has a passband extending from 0 to $(2B + (1+\alpha)B/2)$ and a stopband starting at $(6B - (1+\alpha)B/2)$.

## 5.0 DIGITAL TELEVISION EXAMPLE

A proposed digital TV modulation standard is to transmit the TV signal using a 5 Mega-baud, 64 QAM modulator. In this example the modulator will output the signal at an IF equal to the symbol rate of 5 MHz. The Symbol format chip in Figure 2 accepts a 30 mega-bit data stream and a 30 MHz clock. The chip outputs a 10 mega-word I/Q stream consisting of 3 bit I-words and 3 bit Q-words. The stream is generated by blocking the bit-stream into 6 bit words at a 5 mega-word rate and then inserting zeroes between the words to increase the rate to 10 MHz. The upper 3 bits of the 6 bit words are taken as the I-word, and the lower 3 bits are taken as the Q-word.[1]

The GC2011 and DAC chips are clocked at 20 MHz. A simple clock generator can be implemented within the Symbol formatter FPGA by using the 30 MHz bit stream clock to repetitively output a one followed by two zeroes. The resulting sequence (100100100100100100....) is effectively a phase locked 20 MHz clock.

The filter coefficients are generated using EQ 2.0 with $t$ equal to kT/4 where k ranges from -62 to +62 (a 127 tap filter) and $\alpha$ equal to 0.2 (for 20% excess bandwidth). The GC2011 chip is configured into the complex to real mode and the coefficients are loaded into the chip as described in the GC2011 datasheet[2].

The low pass filter following the DAC chip is designed to pass signals below 8 MHz and reject signals above 12 MHz. The output QAM signal will be centered at 5 MHz with a lower band edge at 2 MHZ and an upper band edge at 8 MHz.

An alternative approach, which involves running the GC2011 and DAC chips at 40 MHz, is to center the output signal at twice the baud rate (10MHz). The higher output center frequency may make the analog IF to RF conversion easier, and relaxes the lowpass filter specifications. The low pass filter would have a passband from 0 to 13 MHz and a stopband starting at 27 MHz. The disadvantage, besides the extra power consumption of running at 40 MHz, is that a clock synthesizer chip would need to be used to generate a 40 MHz clock which is locked to the 30 MHz bit stream clock. In addition, the Symbol Formatter chip will have to output data at a 20 MHz rate (one I/Q pair and then 3 zeroes) which is awkward to generate from the 30 MHz bit stream clock.

---

1. The GC2011 inputs are 12 bits. The 3 bit words should be used as the most significant bits (MSBs), with the fourth bit set to a “1” and the remaining bits set to zero.
2. The coefficients need to be scaled to be 14 bit numbers for the GC2011 chip.

GRAYCHIP
DSP CHIPS AND SYSTEMS
(415) 323-2955
FAX (415) 323-0206
2314 Ramona St. Palo Alto, CA. 94301

# GRAYCHIP APPLICATION NOTES:

## BUILDING A QAM MODULATOR USING A GC2011 DIGITAL FILTER CHIP

*October 6, 1994*

Joseph H. Gray

## IMPORTANT NOTICE



Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Clocks and Timers | www.ti.com/clocks | Digital Control | www.ti.com/digitalcontrol |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Telephony | www.ti.com/telephony |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265