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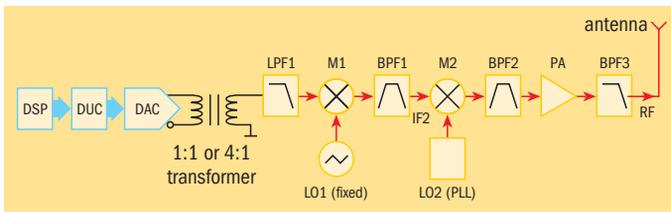


Fig. 1. Traditional base-station transmitter architectures employ two intermediate frequency (IF) stages and many RF components.

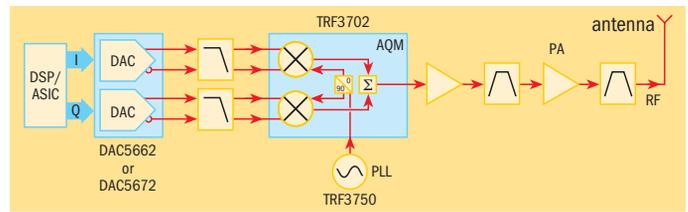


Fig. 2. A direct up-conversion transmitter architecture does not involve any intermediate frequencies and involves fewer RF components than dual IF designs.

Direct up-conversion lowers base-station costs

Matthias Feulner explains why direct up-conversion transmitter architectures represent the future for high-performance, low-cost base-station transceivers.

A minimal cost of implementation is an important – if not the ultimate – criterion for a viable base-station transceiver design. This applies to both 2G systems – where designers are squeezing out the last vestiges of excess costs – and 3G systems.

W-CDMA equipment is moving from the development stage to an early commercial phase and cost is a crucial design parameter. Of course price has always been a factor in the 3G infrastructure business thanks to the high cost of UMTS licences coupled with consumers who expect competitive wireless services. However, 3G networks must deliver reliable coverage and higher data rates to attract subscribers; designers are loath to sacrifice performance so are looking at clever system implementations for the optimum compromise between cost and performance.

There are two fundamental base-station transmitter architecture types to choose from. Multistage implementations use more low-cost basic components, whereas single-stage (zero IF) architectures use far fewer – but technically very advanced – devices.

Early multistage architectures – some of which are still in use today – convert baseband signals to the required radio frequency (RF) using analogue circuitry (see figure 1). Two mixer stages and two intermediate frequencies (IFs) are employed, with the ratio between the two IFs and the RF being a factor of about 10 to ease the filtering of undesired mixing components.

The advantage of this architecture is that only one digital-to-analogue converter (DAC) is required in the transmitter chain because the quadrature modulation of the in-phase (I) and quadrature (Q) channels is done in the digital domain. However, the requirements on the DAC are more demanding because the device must deliver the analogue signal at higher IF frequencies and perfect I/Q gain matching must be achieved in the digital domain. This approach requires many local oscillators (LOs), filters and amplifiers in the IF stages, which is expensive.

The ultimate goal for transmitter implementation is a direct up-conversion architecture that eliminates the need for IF stages

(see figure 2). An I/Q quadrature modulator takes the baseband (or low IF) input signal and up-converts it directly to the desired RF frequency. This eliminates the need for IF components such as filters, amplifiers, mixers and LOs. The design challenge lies in choosing the few remaining components carefully to obtain optimum performance.

Modulator noise

In direct up-conversion architectures the noise performance of the modulator plays a crucial role in meeting system noise limits. If successful, a suitable modulator may replace an entire array of active and passive components.

Modulator noise limits are specified at certain offsets from the carrier by the respective standards. In GSM systems for example, a 6 MHz offset is defined. In Release 6 of the 3GPP specifications, a tolerable modulator noise floor of -148 dBc/Hz was derived from 3GPP specifications for the noise limit at the PA output for a typical GSM system. Texas Instruments' TRF3701 modulator is an example of a suitable modulator for the 900 MHz GSM band, as it achieves a noise spectral density of -150 dBm/Hz at 6 MHz offset from the carrier with a 0 dBm output. As a result it can achieve a noise floor of -150 dBc/Hz and is suitable for direct up-conversion GSM systems.

The TRF3702 modulator, which operates at output frequencies of up to 2.5 GHz output, can achieve similar performance levels in the GSM 1800 and 1900 MHz bands. The TRF3702 is also appropriate for cdma2000 and W-CDMA applications. The critical offset frequency for W-CDMA is located at ± 60 MHz from the carrier frequency.

The adjacent channel power ratio (ACPR) measures interference with nearby channels and is a critical parameter for a quadrature modulator in multicarrier systems. The ACPR describes the power ratio between a carrier signal and its inter-modulation products. In a W-CDMA setting, this is measured at 5 and 10 MHz

offset from the carrier frequency at the modulator output.

The UMTS standard requires an ACPR at the antenna of 45 dBc at 5 MHz offset and 50 dBc at 10 MHz offset. The corresponding ACPR requirement at the modulator is 60 dBc or higher. The TRF3702 can be used to process a single W-CDMA carrier at 2.14 GHz signal frequency. The resulting ACPR (at the output of the device) at 5 MHz offset is about -71.2 dBc, which is well within the limits defined by the UMTS standard.

The requirements placed on DACs are relaxed considerably in direct up-conversion architectures. The output frequency is usually low and the sampling rates are generally lower than with other configurations, thus standard non-interpolating DACs may be used. Nevertheless there are key performance parameters that remain critical. These include spurious-free dynamic range (SFDR) and the ACPR, which is particularly important for W-CDMA applications. A new generation of dual DACs now offers outstanding cost-to-performance ratio.

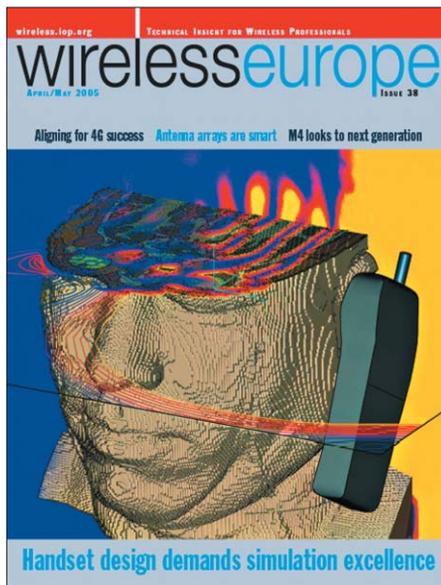
The 12-bit DAC5662 is a member of the new family of pin-compatible non-interpolating dual DACs from Texas Instruments and is suitable for applications where the ACPR and SFDR must be better than 65 dBc and 70 dBc respectively. It offers an ACPR of 72 dBc at 30.72 MHz intermediate frequency (IF) and an SFDR of 85 dBc at 5 MHz IF. Update rates of up to 200 Msample/s match well with popular sampling rates of 76.8, 128.88 and 153.6 Msample/s. A performance upgrade is available with the DAC5672 – a corresponding pin-compat-

ible 14-bit DAC with a SFDR of 84 dBc at 5 MHz IF and an ACPR of 75 dB at 15.36 MHz IF.

While not directly part of the transmit chain, the noise introduced by the local oscillator (LO) synthesizer may be limited by the RF phase-locked loop (PLL) and thus degrade the VCO phase noise characteristics. The transmitter LO phase noise requirements are usually not as stringent as those imposed by the receiver. An integer-N PLL like TI's TRF3750 is appropriate for transmitter LO generation and could even serve the more demanding receiver LO generation in GSM systems. It offers a phase noise of -91 dBc/Hz in the 900 MHz band, -84 dBc/Hz in the 1900 MHz band and -83 dBc/Hz in the 2200 MHz band.

The elimination of the IF frequency stages in base-station transceivers can bring large savings in component costs. Indeed savings of more than 50% can be made by changing from a dual IF transmitter architecture to direct up-conversion. The implementation of a direct up-conversion architecture also increases the reliability of the system by reducing the number of components that could fail – assuming that complexity and associated failure rate of individual components remains constant. Another key benefit of direct up-conversion is that it reduces the size of base-station equipment, which makes it particularly suitable for picocellular applications with stringent space constraints. ■

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