User's Guide

TSW14J58 JESD204C Data Capture and Pattern Generator Card

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TSW14J58EVM JESD204C high-speed data capture and pattern generator card. Throughout this user's guide, the abbreviations *EVM*, and the term *evaluation module* are synonymous with the TSW14J58EVM, unless otherwise noted.

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Trademarks

1 Introduction

The TI TSW14J58 evaluation module (EVM) is a next-generation pattern generator and data capture card used to evaluate performances of the new TI JESD204C_B device family of high-speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC). For an ADC, by capturing the sampled data over a JESD204C_B interface when using a high-quality, low-jitter clock, and a high-quality input frequency, the TSW14J58 can be used to demonstrate data sheet performance specifications. Using the Xilinx® JESD204C IP core, the TSW14J58 can be dynamically configurable to support lane speeds from 1 Gbps to 24.5 Gbps, from 1 to 16 lanes. Together with the accompanying High-Speed Data Converter Pro Graphic User Interface (GUI), it is a complete system that captures and evaluates data samples from ADC EVMs, generates and sends desired test patterns to DAC EVMs, and perform both tasks at the same time with AFE EVMs (transceiver mode).

2 Functionality

The TSW14J58EVM has a single industry standard FMC+ connector that interfaces directly with TI JESD204B ADC, DAC, and AFE EVMs. The FMC+ carrier connector is compatible with the FMC mezzanine connector. When used with an ADC EVM, high-speed serial data is captured, deserialized and formatted by a Xilinx® Kintex® UltraScale® + FPGA. The data is then stored into an external DDR4 memory bank, enabling the TSW14J58 to store up to 1.536G, 16-bit data samples. To acquire data on a host PC, the FPGA reads the data from memory and transmits it on a high-speed 16-bit parallel interface. An onboard high-speed USB 3.0 to parallel converter bridges the FPGA interface to the host PC and GUI.

In pattern generator mode, the TSW14J58 generates the desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J58. The FPGA stores the data received into the board DDR4 memory module. The data from memory is then read by the FPGA and transmitted to a DAC EVM across the FMC+ interface connector. The board contains a 200-MHz oscillator used to generate the DDR4 reference clock and a general purpose clock. shows the TI TSW14J58 evaluation module.

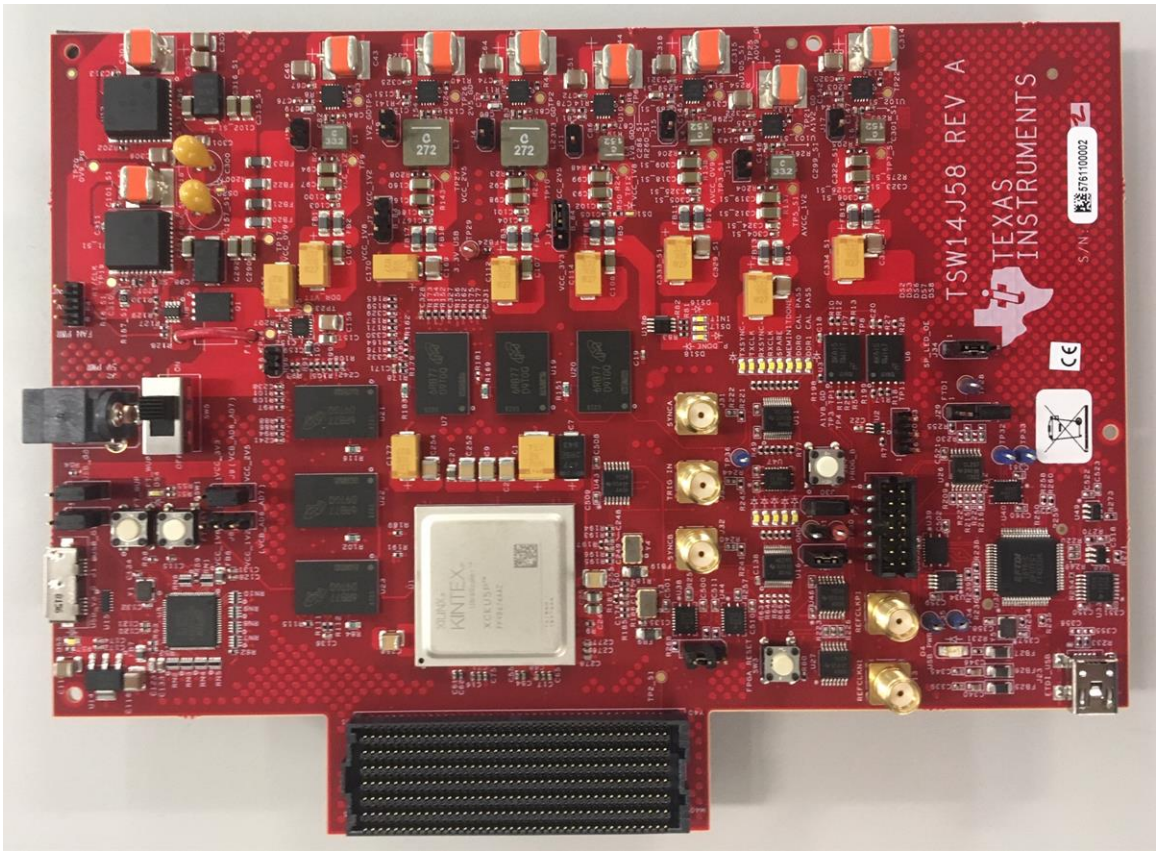

Figure 2-1. TSW14J58EVM

The major features of the TSW14J58 are:

- Backward-compatible with JESD204B (Subclasses: 0 1, 2)
- Support for deterministic latency
- Serial lanes speeds up to 24.5 Gbps
- 16 routed transceiver channels
- 24Gb DDR4 SDRAM (split into two banks of 3 independent 256 × 16, 4Gb SDRAMs). Quarter rate DDR4 controllers supporting up to 1200-MHz operation
- 1.536G of 16-bit samples of onboard memory
- Supports 1.8-V CMOS IO standard for spare FMC+ signals
- General purpose 200-MHz oscillator
- Onboard FTDI FT601Q-B USB 3.0 device for parallel interface to the FPGA

- Onboard FTDI FT4232H USB 2.0 device for FPGA JTAG interface (downloading firmware) and general purpose I/O interface to onboard functions and FMC+
- Reference clocking for transceivers available through FMC+ port or SMAs
- Supported by TI HSDC PRO software
- FPGA firmware developed with Xilinx Vivado development tool.
  - JESD RX IP core with support for:
    - USB and JTAG reconfigurable JESD core parameters: L, M, K, F, HD, S, and more
    - ILA configuration data accessible through USB and JTAG
    - Lane alignment and character replacement enabled or disabled through USB and JTAG
  - JESD TX IP core with support for:
    - USB and JTAG reconfigurable JESD core parameters: L, M, K, F, HD, S, and more
    - ILA configuration data accessible through USB and JTAG
    - Dynamically reconfigurable Transceiver data rate.
  - Serial lane operating range from 1 to 24.5 Gbps

Figure 2-2 shows a block diagram of the TSW14J58 EVM.

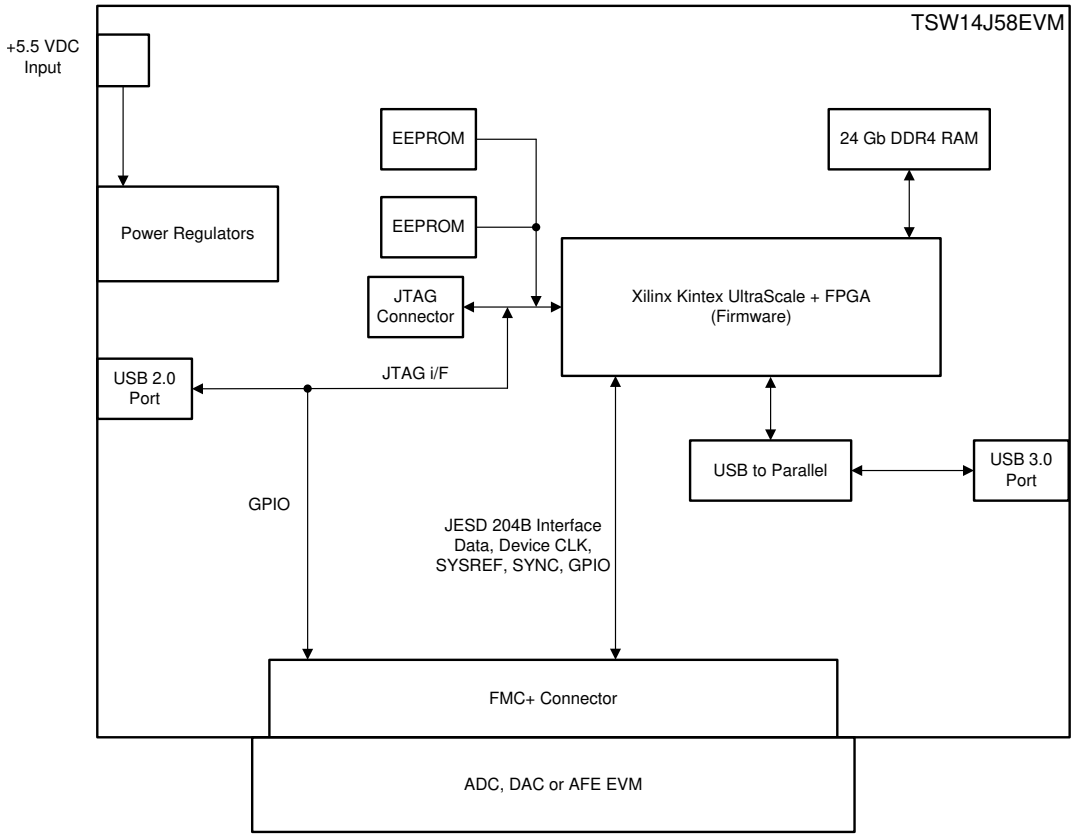

Figure 2-2. TSW14J58EVM Block Diagram

2.1 ADC EVM Data Capture

New TI high-speed ADCs and DACs now have high-speed serial data that meets the JESD204C_B standard. These devices are generally available on an EVM that connects directly to the TSW14J58EVM. The common connector between the EVMs and the TSW14J58EVM is a Samtec high-speed, high-density FMC+ connector (ASP-184329-01) suitable for high-speed differential pairs up to 32.5 Gbps. A common pinout for the connector across a family of EVMs has been established. At present, the interface between the EVMs and the TSW14J58EVM has defined connections for 32 high-speed differential data pairs (16 RX and 16 TX), 23 single-ended signals, a single-ended SYNC, 5 differential spares, a differential SYNC and SYSREF, and four device clock pairs (FPGA reference clock). The board has 10 spare USB2.0 interface signals, two FPGA reference clock SMAs, three SYNC output SMAs, one external input trigger SMA, four reset switches, and 13 status LEDs.

The data format for JESD204C_B ADCs and DACs is a serialized format, where individual bits of the data are presented on the serial pairs commonly referred to as lanes. Devices designed around the JESD204C_B specification can have up to 16 lanes for transmitting or receiving data. The firmware in the FPGA on the TSW14J58 is designed to accommodate any of TI's ADC or DAC operating with any number of lanes from 1 to 16.

The HSDC Pro GUI loads the FPGA with the appropriate firmware and a specific JESD204C_B configuration, based on the ADC device selected in the device drop down window. Each ADC device that appears in this window has an initialization file (.ini) associated to it. This .ini file contains JESD information, such as number of lanes, number of converters, octets per frame, and other parameters. This information is loaded into the FPGA registers after the user clicks on the capture button. After the parameters are loaded, synchronization is established between the data converter and FPGA and valid data is then captured into the onboard memory. See the *High-Speed Data Capture Pro GUI Software User's Guide* under the Technical Documents section for more information. Several .ini files are available to allow the user to load predetermined ADC JESD204C_B interfaces.

The TSW14J58 device can capture up to 1.536G 16-bit samples at a maximum line rate of 24 Gbps that are stored inside the onboard DDR4 memory. The data size the user sets in the HSDC Pro GUI must be entered as multiples of 480. To acquire data on a host PC, the FPGA reads the data from memory and transmits parallel data to the onboard high-speed parallel-to-USB3.0 converter.

2.2 DAC EVM Pattern Generator

In pattern generator mode, the TSW14J58EVM generates desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J58. The FPGA stores the data received into the onboard DDR4 memory. The data from the memory is then read by the FPGA, converted to JESD204C_B serial format, then transmitted to a DAC EVM. The TSW14J58 can generate patterns up to 1.536G 16-bit samples at a line rate up to 24.5 Gbps.

There are GUIs available that come with several existing test patterns that can be download immediately. Like the ADC capture mode, the DAC pattern generator mode uses .ini files to load predetermined JESD204C_B interface information to the FPGA.

3 Hardware Configuration

This section describes the various portions of the TSW14J58EVM hardware.

3.1 Power Connections

The TSW14J58EVM hardware is designed to operate from a single supply voltage of +5.5 V DC. The power input is controlled by the on and off switch, SW5. Make sure this switch is in the off position before inserting the provided power cable. Insert the connector end of the power cable into J2 of the EVM. Connect the positive red wire end of the power cable to +5.5 V DC output of a power supply rated for at least 5 Amps. Connect the negative black wire to the RETURN or GND of the power supply. The board can also be powered up by providing +5.5 V DC to the red test point, TP18, and the return to any black GND test point. As an example, the TSW14J58 draws approximately 0.6 A at power-up and 3 A when capturing 8 lanes of data from an AFE at a line rate of 24.33 Gpbs.

Note

The typical power supply range for the TSW14J58EVM is 5.5V with a power consumption of about 16.5W. It is recommended that at least a 5 A rated supply be provided to the TSW14J58EVM due to the current consumption increase when data is being captured by HSDC Pro.

3.2 Switches, Jumpers, and LEDs

3.2.1 Switches and Push-Buttons

The TSW14J58 contains several switches and push-buttons that enable certain functions on the board. The description of the switches is found in Table 3-1.

Table 3-1. Switch Description of the TSW14J58 Device

Component	Description
SW1	USB 2.0 reset
SW2	USB 3.0 reset
SW3	FPGA hardware reset
SW4	Force FPGA firmware load from selected EEPROM
SW5	Board main power switch

3.2.2 Jumpers

The TSW14J58 contains several jumpers (JP) and solder jumpers (SJP) that enable certain functions on the board. The description of the jumpers is found in Table 3-2.

Table 3-2. Jumper Description of the TSW14J58 Device

Component	Description	Default
J4	Disables VCCO_3V3 supply when installed	Open
J5	USB3.0 GPIO0 configuration. With shunt on pins 1–2, sets this high. Shunt on 2–3 sets this low	Open
J6	USB3.0 GPIO1 configuration. With shunt on pins 1–2, sets this high. Shunt on 2–3 sets this low	Open
J10	Disables VCCO_1V2 supply when installed	Open
J11	Disables VCCO_1V8 supply when installed	Open
J15	Disables MGTAVCC_0V9 supply when installed	Open
J16	Disables MGTAVTT_1V2 supply when installed	Open
J17	Disables MGTAVCCAUX_1V2 supply when installed	Open
J19	Disables VCCO_2V5 supply when installed	Open
J21	Output SYNCA/B/C and input TRIG_IN translator voltage level select. With shunt on pins 1–2, voltage is 3.3V. With shunt on pins 2–3, voltage is controlled by TP30.	1 to 2
J28	Buffers U38, U44, U46 enable. With shunt on pins 1–2, U44 is enabled and U38 and U46 are disabled. With shunt on pins 2–3, U44 is disabled and U38 and U46 are enabled.	1 to 2

Table 3-2. Jumper Description of the TSW14J58 Device (continued)

Component	Description	Default
J29	USB2.0 JTAG MUX enable. With shunt on pins 1–2, MUX is enabled. With shunt on pins 2–3, MUX enable is controlled by USB2.0 device.	2 to 3
J30	U47 buffer enable. With shunt on pins 1–2, U47 is disabled. With shunt on pins 2–3, U47 is enabled.	1 to 2
J34	Status LEDs enable. With shunt on pins 1–2, LEDs are disabled. With shunt on pins 2–3, LEDs are enabled.	1 to 2
J35	EPROM select. With shunt on pins 2–3, select is controlled by USB2.0. With shunt on pins 1–2, U3 is selected. With shunt removed, U6 is selected.	2 to 3

3.3 LEDs

3.3.1 Power and Configuration LEDs

Several LEDs are on the TSW14J58 EVM to indicate the presence of power and the state of the FPGA. The description of these LEDs is found in Table 3-3.

Table 3-3. Power and Configuration LED Description of the TSW14J58 Device

Component	Description
D4	On if USB2.0 device is powered up
DS4	USB3.0 FT601 device wakeup
DS5	On if USB3.0 cable is connected between EVM and host PC
D16	On if firmware has been loaded into FPGA
D17	On after power up and after firmware has been loaded
DS20	On if 5.5 V is present and power switch is turned on
TXSYNC	On when EVM powers up
RXSYNC	Not used
TX Active	Not used
RX Active	On when EVM powers up. Off when firmware is loaded
GT_Pwr Good	On when EVM powers up. Off when firmware is loaded
SYSREFT Done	Not used
DDR Calib	On when EVM powers up and when firmware is loaded
PLL Lock	On when EVM powers up and when firmware is loaded

3.3.2 Spare LEDs

The TSW14J58EVM has five spare LEDs on the TSW14J58EVM. These are disabled by default.

DS2 – SYNCA

D2S3 – SYNCB

DS6 – TRIG_IN

DS7 – CAL TRIG

DS8 – CAL STAT

To enable the LEDs, place the shunt on J34 to pin 2–3.

3.3.3 Connectors

3.3.3.1 SMA Connectors

The TSW14J58 has 5 SMA connectors. Table 3-4 defines the connectors:

Table 3-4. SMA Connectors

Component	Connector	Description
J12	REFCLKP1	Spare external FPGA reference clock+. Must install C527 and remove C552 to use this input. This connects to FPGA clock input ball H7
J13	REFCLKN1	Spare external FPGA reference clock–. Must install C528 and remove C553 to use this input. This connects to FPGA clock input ball H6
J31	SYNCA	3V3 CMOS logic SYNC output. J21 must have shunt installed between pins 1–2 to enable this output. This signal is sourced by FPGA ball J15. A shunt on pins 2–3 of J34 enables SYNCA LED.
J32	SYNCB	3V3 CMOS logic SYNC output. J21 must have shunt installed between pins 1–2 to enable this output. This signal is sourced by FPGA ball G14. A shunt on pins 2–3 of J34 enables SYNCB LED.
J36	SYNCC	3V3 CMOS logic SYNC output. J21 must have shunt installed between pins 1–2 to enable this output. This signal is sourced by FPGA ball G19.
J33	TRIG IN	3V3 CMOS logic trigger input to FPGA pin G12. A shunt on pins 2–3 of J34 enables TRIG IN LED.

Note

SYNCA, SYNCB, and SYNCC SMAs are used to provide external SYNC signals from the FPGA. The cables of each SYNC signal should have equal length to ensure the signal arrives at the same time for all boards using these SYNCs. The TRIG IN SMA connector can be used to trigger the FPGA from an external source. All four SMAs use 3V3 logic CMOS signals. The EVM has onboard translators to set these inputs/outputs to the correct voltage levels for the FPGA.

3.3.3.2 FPGA Mezzanine Card (FMC+) Connector

The TSW14J58 EVM has one connector to allow for the direct plug in of TI JESD204C_B serial interface ADC and DAC EVMs. The specifications for this connector are mostly derived from the ANSI/VITA 57.4 FPGA Mezzanine Card (FMC+) Standard. This standard describes the compliance requirements for a low-overhead protocol bridge between the IO of a mezzanine card and an FPGA processing device on a carrier card. This specification is being used by FPGA vendors on their development platforms.

The FMC+ connector, J3, provides the interface between the TSW14J58EVM and the ADC or DAC EVM under test. This 560-pin Samtec high-speed, high-density connector (part number ASP-184329-01) is suitable for high-speed differential pairs up to 32.5 Gbps.

In addition to the JESD204B/C standard signals, several CMOS single-ended signals and LVDS differential signals are connected between the FMC+ and FPGA. In the future, these signals may allow the HSDC Pro GUI to control the SPI serial programming of ADC and DAC EVMs that support this feature. The connector pinout description is shown in Table 3-5.

Table 3-5. FMC+ Connector Description of the TSW14J58

FMC+ Signal Name	FMC+ Pin	Standard JESD204 Application Mapping	Description
RXP/N0_0	C6 and C7	Lane 0± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N1_0	A2 and A3	Lane 1± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N2_0	A6 and A7	Lane 2± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N3_0	A10 and A11	Lane 3± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N0_1	A14 and A15	Lane 4± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N1_1	A18 and A19	Lane 5± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N2_1	B16 and B17	Lane 6± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N3_1	B12 and B13	Lane 7± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N0_2	B8 and B9	Lane 8± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N1_2	B4 and B5	Lane 9± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N2_2	Y10 and Y11	Lane 10± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N3_2	Z12 and Z13	Lane 11± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N0_3	Y14 and Y15	Lane 12± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N1_3	Z16 and Z17	Lane 13± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N2_3	Y18 and Y19	Lane 14± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
RXP/N3_3	Y22 and Y23	Lane 15± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
TXP/N0_0	C2 and C3	Lane 0± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N1_0	A22 and A23	Lane 1± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N2_0	A26 and A27	Lane 2± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N3_0	A30 and A31	Lane 3± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N0_1	A34 and A35	Lane 4± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N1_1	A38 and A39	Lane 5± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N2_1	B36 and B37	Lane 6± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N3_1	B32 and B33	Lane 7± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N0_2	B28 and B29	Lane 8± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N1_2	B24 and B25	Lane 9± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N2_2	Z24 and Z25	Lane 10± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N3_2	Y26 and Y27	Lane 11± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N0_3	Z28 and Z29	Lane 12± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine

Table 3-5. FMC+ Connector Description of the TSW14J58 (continued)

FMC+ Signal Name	FMC+ Pin	Standard JESD204 Application Mapping	Description
TXP/N1_3	Y30 and Y31	Lane 13± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N2_3	Z8 and Z9	Lane 14± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
TXP/N3_3	Y6 and Y7	Lane 15± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
J3_REFCLKP/N0_0	D4 and D5	DEVCLKA± (M → C)	Primary carrier-bound reference clock required for FPGA giga-bit transceivers. Equivalent to device clock.
J3_REFCLKP/N1_0	B20 and B21	Alt. DEVCLKA± (M → C)	Alternate Primary Carrier-bound reference clock required for FPGA giga-bit transceivers. For use when DEVCLKA (M → C) is not available
J3_REFCLKP/N1_1	Z20 and Z21	Alt. DEVCLKA+ (M → C)	Alternate Primary Carrier-bound reference clock required for FPGA giga-bit transceivers. For use when DEVCLKA (M → C) is not available
Device Clock, SYSREF, and SYNC			
GPIO_DIFF_P/N<9>	G6 and G7	DEVCLKB± (M → C)	Secondary carrier-bound device clock. Used for special FPGA functions such as sampling SYSREF
GPIO_DIFF_P/N<3>	G9 and G10	SYSREF± (M → C)	Carrier-bound SYSREF signal
GPIO_DIFF_P/N<2>	G12 and G13	SYNC± (C → M)	ADC mezzanine-bound SYNC signal for use in class 0/1/2 JESD204 systems
AC14_P/N	F10 and F11	DAC SYNC± (M → C)	Carrier-bound SYNC signal for use in class 0/1/2 JESD204B systems
GPIO_DIFF_P/N<9>	F19 and F20	Alt. DAC SYNC± (M → C)	Alternate carrier-bound SYNC signal for use in class 0/1/2 JESD204B systems
GPIO_DIFF_P/N<9>	H31 and H32	Alt. SYNC± (C → M)	Alternate ADC mezzanine-bound SYNC signal. For use when SYNC (C → M) is not available
Special Purpose I/O			
GPIO_C6	F1		Spare from FPGA pin G25
GPIO_C3	K10		Spare from FPGA pin U24
GPIO_C5	K14		Spare from FPGA pin AF13
GPIO_C10	K7		Spare from FPGA pin AF15
GPIO_B25	K13		Spare from FPGA pin AE13
GPIO_B26	K11		Spare from FPGA pin Y23
GPIO_D15	K8		Spare from FPGA pin Y16
ACLK	D11		Spare from FPGA pin W12
ASDIO	D12		Spare from FPGA pin W13
PRESENT	H2	Present	USB2.0 input. Indicates if a mezzanine card is present
ASDO	D26		Spare from FPGA pin G11
ASEN	D27		Spare from FPGA pin G9
PRESENT_Z1	Z1	Present	USB2.0 input. Indicates if a mezzanine card is present.
K4_P/K4_N	K4 and K5		REFCLKP1_3 to FPGA pin H7 and H6
CSB_ADC	D17		Spare from FPGA pin AA13
CSB_LMK	D18		Spare from FPGA pin AF13
CSB_LMX	D20		Spare from FPGA pin AF14
SCLK	C22		Spare from FPGA pin W12
SDI	C23		Spare from FPGA pin W13
SDO_ADC	C26		Spare from FPGA pin Y13
SDO_LMK	C27		Spare from FPGA pin AE13
SCL	C30		Spare USB2.0 I/F
SDA	C31		Spare USB2.0 I/F
NCOA0	J18		Spare from FPGA pin AF15
NCOA1	J19		Spare from FPGA pin Y16
NCOB0	J21		Spare from FPGA pin G22
NCOB1	J22		Spare from FPGA pin F22
CDBUS2-5	G27, G28, G33, G34		Spare USB2.0 I/O's
DDBUS0-3	G21, G22, G36, G37		Spare USB2.0 I/O's

3.3.3.3 JTAG Connectors

The TSW14J58EVM includes one industry-standard JTAG connector, P2, that connects to the JTAG port of the FPGA. The USB 2.0 interface on the TSW14J58EVM allows for the FPGA to be programmed from the JTAG connector or the USB 2.0 interface. The USB 2.0 interface allows the FPGA to be programmed using the HSDC Pro software GUI. Every time the TSW14J58EVM is powered-down, the FPGA configuration is removed. The user must program the FPGA through the GUI after every time the board is powered-up. The FPGA can also be configured using the two on-board flash devices, U3 and U6.

FLASH DEVICES The TSW14J58EVM includes two serial flash programming EEPROMS that can load FPGA firmware. From the factory, U3 is loaded with a file called JESD204B_1p4.mcs which will configure the FPGA to operate in JESD204B mode. U6 is loaded with a file called JESD204C_1p4.mcs which will configure the FPGA to operate in JESD204C mode. Jumper J35 determines which EEPROM will configure the FPGA when switch SW4 is pressed. After power up, pressing SW4 will load the FPGA with the factory pre-programmed flash device U3 if J35 has a shunt between pins 1-2 and U6 if the shunt is between pins 2-3 or removed.

Program the Memory Device

To program U3 and U6 with new files, use the following steps:

Note

Install Vivado® version 2018.3 or later (Lab Edition)

1. Connect the TSW14J58 Capture card to the PC through a JTAG Xilinx Programmer cable. This will be the JTAG connect P2.
2. Open the Vivado Installation:
   - Double click “Open Hardware Manager”.
3. In the Hardware Manager, left click on “Open target” and select “Auto Connect”.
4. This will list all the FPGAs connected to the PC through JTAG Programmer cables.
5. Right click on “xcku5p_0” -> click on “Add Configuration Memory Device”.

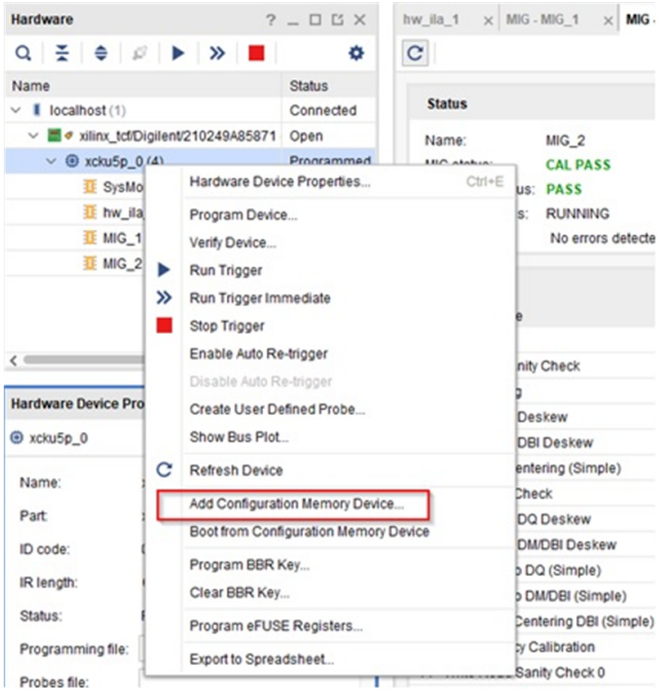

Figure 3-1. Add Configuration Memory Device

6. In the pop-up window, search for the “mt25qu256-spi-x1_x2_x4” component. Click the *OK* button.

7. Right click on device “mt25qu256-spi-x1_x2_x4”, and click on “Program Configuration Memory Device” (see Figure 3-2).

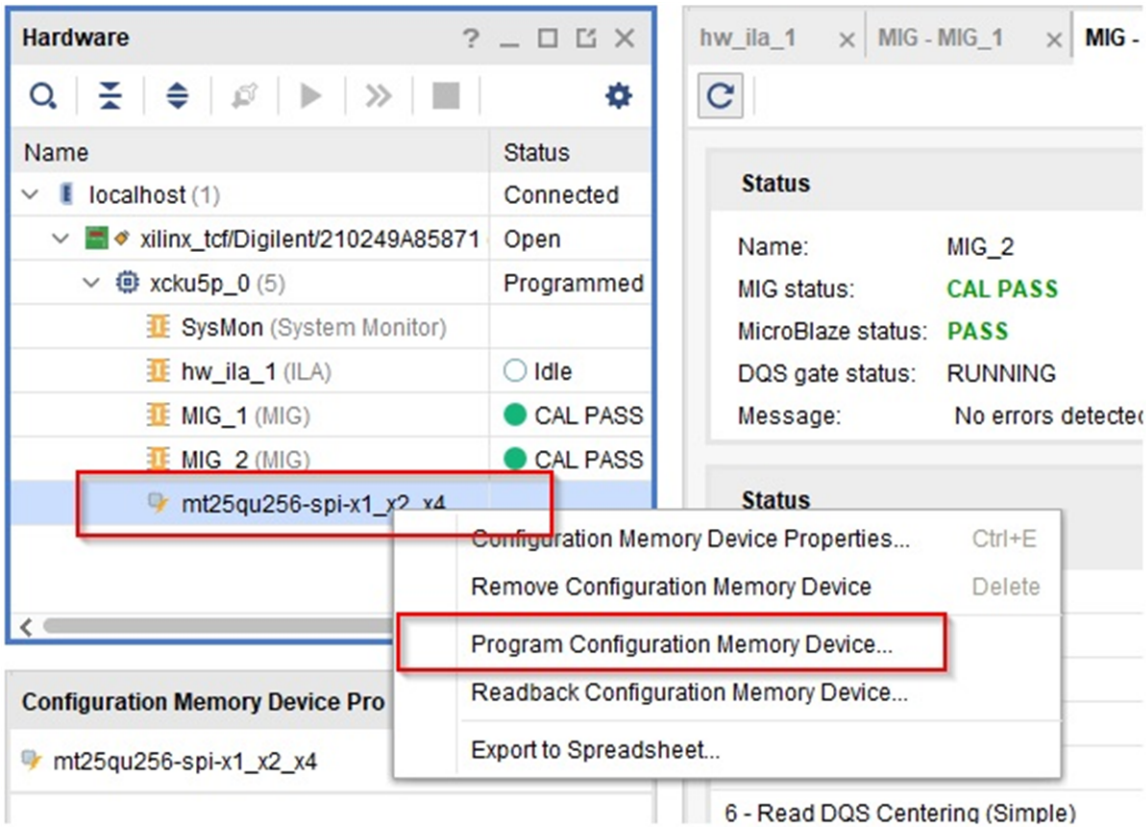

Figure 3-2. Programming Memory Device

8. With J35 = 1–2, open up the new “xx.mcs” file to be loaded, and check the following setup in the programming. Click the *OK* button when completed. Figure 3-3 illustrates the configuration file to be loaded.

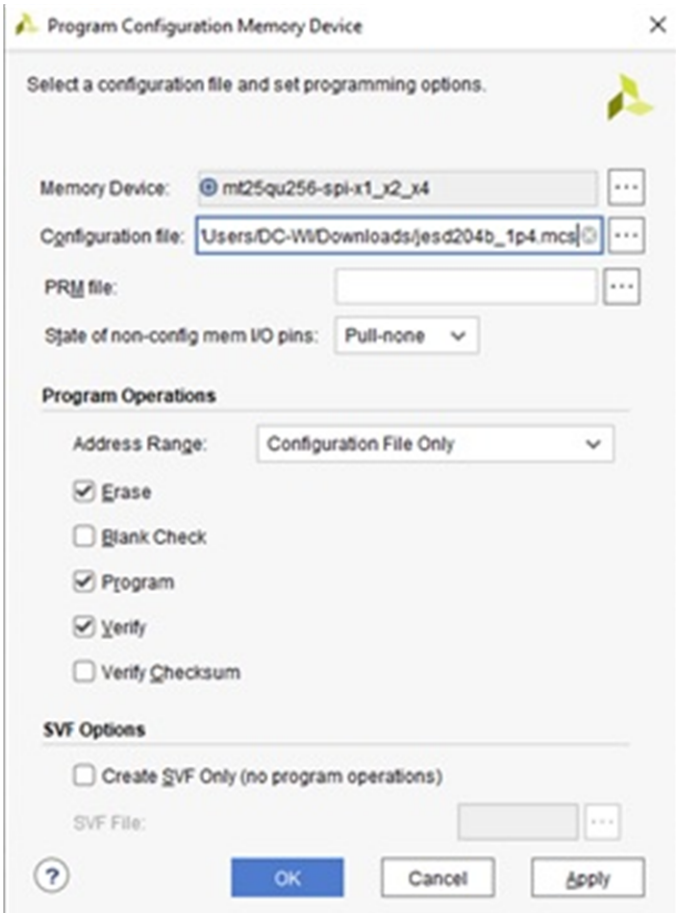

Figure 3-3. Config file

9. Press SW4 to reload the EEPROM
10. Press SW3 to reset FPGA
11. With J35 = 2–3, open up the new “yy.mcs”file to be loaded and check the following setup in the programming. Click the *OK* button when completed.

3.3.3.4 USB I/O Connection

Control of the TSW14J58EVM is through the USB 3.0 connector J1 and USB 2.0 connector J23. This provides the interface between the HSDC Pro GUI running on a PC using the Microsoft® Windows® operating system and the FPGA. For the computer, the drivers needed to access the USB port are included on the HSDC Pro GUI installation software that can be downloaded from the web. The drivers are automatically installed during the installation process. On the TSW14J58EVM, the USB port is used to identify the type and serial number of the EVM under test, load the desired FPGA configuration file, capture data from ADC EVMs, and send test pattern data to the DAC EVMs.

4 Software Start-Up

4.1 Installation Instructions

- Download the latest version of the *HSDC Pro GUI* to a local directory on a host PC. This is found on the TI website by entering “HIGH SPEED DATA CONVERTER PRO GUI INSTALLER”.
- Unzipping the software package generates a folder called “High Speed Data Converter Pro - Installer vx.xx.exe", where x.xx is the version number. Run this program to start the installation.
- Make sure to disconnect all USB cables from any TSW14xxx boards before installing the software.
- Follow the on-screen instructions during installation.
- Click on the “Install” button. A new window opens. Click the *Next* button.
- Accept the License Agreement. Click on the *Next* button to start the installation. After the installer has finished, click the *Next* button one last time.
- The installation is now complete. The GUI executable and associated files will reside in the following directory:
  C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro.
- Power up the TSW14J58 under test. Connect both a USB2.0 and USB3.0 cable between the EVM and a host computer.
- To start the GUI, click on the file called “High Speed Data Converter Pro.exe", located under C:\Program Files\Texas Instruments\High Speed Data Converter Pro.

Note

If an older version of the GUI has already been installed, make sure to uninstall it before loading a newer version. If the GUI detects that a newer version of the GUI is available online (http://www.ti.com/tool/DATACONVERTERPRO-SW), it will assist the user with downloading the latest version from the TI website. The GUI automatically interrogates the product website for the latest version every seven days but the latest version check can also be manually invoked through use of the pull-down menu *Help→Check for updates*.

Note

When new TI high-speed data converter EVMs or JESD204C_B interface modes become available that are not currently supported by the latest release of HSDC Pro GUI, the HSDCProv_xpxx_Patch_setup executable, available on the TI website under the High Speed Data Converter Pro Software product folder (http://www.ti.com/tool/DATACONVERTERPRO-SW), will allow the user to add these to the GUI device list. After the patch has been downloaded, follow the on-screen instructions to run the patch. The software displays the files that will be added. After running the patch, open HSDC Pro and the new parts and modes will appear in the ADC and DAC device drop-down selection box. The patch is always specific to a core GUI version and will not work for a GUI version for which the patch was not explicitly created.

4.2 USB Interface and Drivers

- Connect a USB 3.0 cable between J1 of the TSW14J58EVM and a host PC. LED DS5 should turn on indicating power present to the USB3.0 device.
- Connect a USB 2.0 cable between J23 of the TSW14J58EVM and a host PC
- Connect the provided power cable between J2 of the EVM and a +5.5 VDC source.
- Set SW5 to ON. LEDs DS20 (+5.5 V present), D4 (USB2.0 power present), and several status LEDs should turn on.

Click on the *High-Speed Data Converter Pro* icon that was created on the desktop panel, or go to C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro and double click on the executable called “High Speed Data Converter Pro.exe” to start the GUI.

The GUI first attempts to connect to the EVM USB interface. If the GUI identifies a valid board serial number, a pop-up opens displaying this value, as Figure 4-1 shows. The user can connect several TSW14J58 EVMs to one host PC, but the GUI can only connect to one at a time. When multiple boards are connected to the PC, the pop-up displays all of the serial numbers found. The user then selects which board to associate the GUI with.

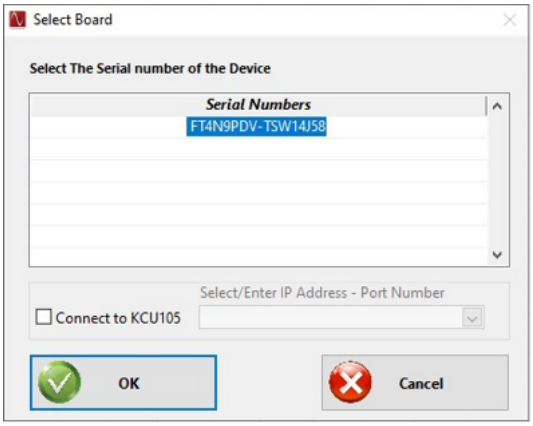

Figure 4-1. TSW14J58EVM Serial Number

Click the *OK* button to connect the GUI to the board. The top-level GUI opens and appears as shown in Figure 4-2.

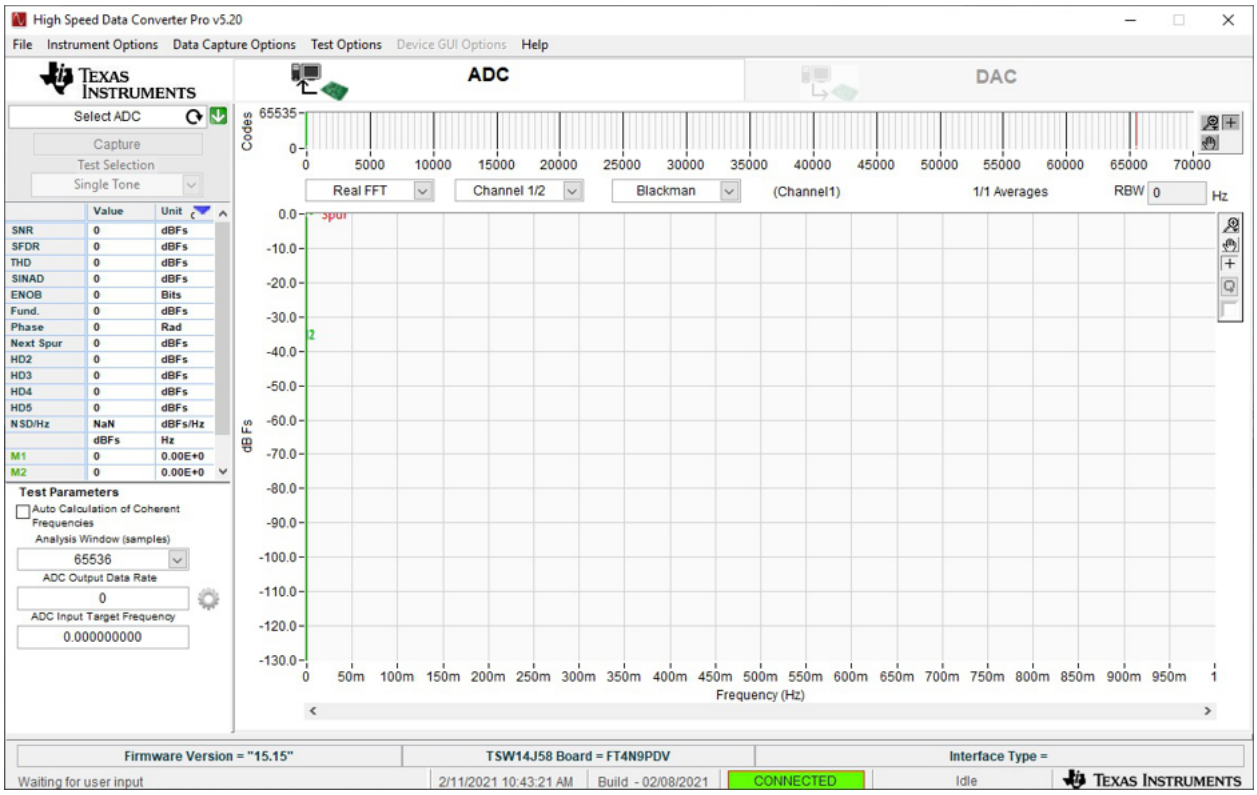

Figure 4-2. High-Speed Data Converter Pro GUI Top Level

If the message “No Board Connected” opens, double check the USB cable connections and that power switch SW5 is in the on position. Remove the USB3.0 cable from the board then re-install. Click on the *Instrument Option* tab at the top left of the GUI and selecting “Connect to the Board”. If this still does not correct this issue, check the status of the host USB port.

When the software is installed and the USB cables are connected to the TSW14J58EVM and the PC, the TSW14J58 USB 3.0 converter should be located in the Hardware Device Manager under the universal serial bus controllers as shown in Figure 4-3, labeled as FTDI FT601 USB 3.0 Bridge Device. When the USB 3.0 cable is removed, this driver will no longer be visible in the device manager. The USB 2.0 device will be listed as USB Serial Converter A, B, C and D. If the drivers are present in the device manager window and the software still does not connect, remove the USB cables from the board then reconnect them. Attempt to connect to the board using the GUI. If the problem still exists, cycle power to the board and repeat the prior steps.

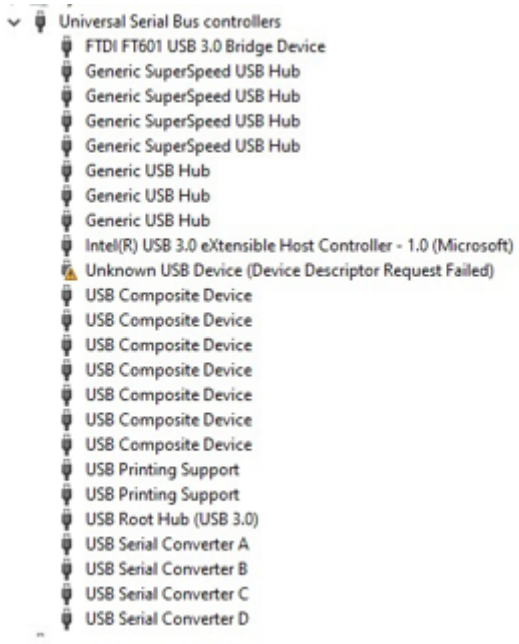

Figure 4-3. Hardware Device Manager

5 Downloading Firmware

The TSW14J58EVM has an Xilinx® Kintex® UltraScale® XCKU5P device that requires firmware to be downloaded every time power is cycled to operate. The firmware files needed are special .bin formatted files that are provided with the software package. The files used by the GUI currently reside in the directory called C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J58 Details\Firmware.

To load a firmware, after the GUI has established connection, click the drop-down arrow on the right side of the *Select ADC* window in the top left of the GUI and select the device to evaluate, for example, ADC12DJ3200_JMODE0_2G_3G, as shown in Figure 5-1.

The GUI prompts the user to update the firmware for the ADC. Click "Yes". The GUI will display the message "Downloading Firmware, Please Wait". The software now loads the firmware from the PC to the FPGA, a process that takes about 6 seconds. Once completed, the GUI reports an Interface Type in the lower right corner and LEDs D16, D17, DDR Calib and PLL lock should all turn white.

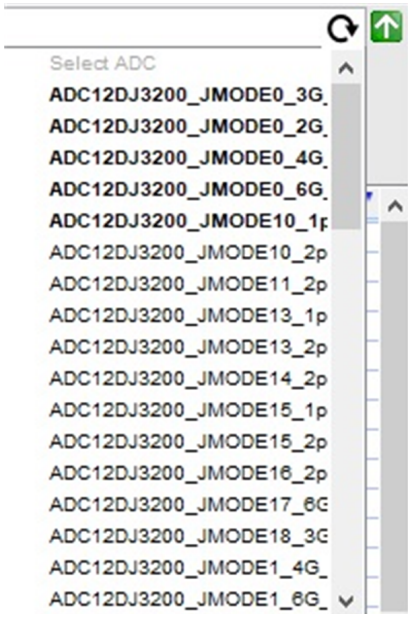

Figure 5-1. Select ADC Firmware to be Loaded

For information regarding the use of the TSW14J58EVM with a TI ADC or DAC JESD204C_B serial interface EVM, consult the *High-Speed Data Converter Pro GUI User's Guide* and the individual EVM User's Guide, available on www.ti.com.

If the message appears as shown in Figure 5-2, verify that all jumpers are in the default position and the power and USB status LEDs are illuminated. If the 5.5-V power status LED is off, there may be a problem with the external power supply. Make sure this supply can source at least 5 A of current. If the available current is too low, this can prevent the firmware from downloading. Unplug and re-install the USB connectors and try to connect to the board. If this fails, cycle the power switch to re-initialize the power-up sequencer to try to correct this problem.

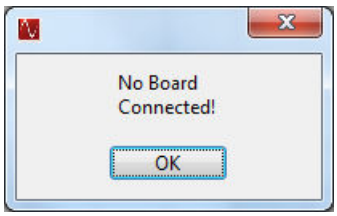

Figure 5-2. Download Firmware Error Message

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