Matching the noise performance of the operational amplifier to the ADC

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Proper selection of the operational amplifier that drives an analog-to-digital converter (ADC) in a mixed-signal application is critical. The designer must compare issues such as amplifier noise, bandwidth, settling time, and slew rate to the ADC's signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), input impedance, and sampling time. This article specifically addresses the matching of the noise specifications and performance of an op amp and a successive approximation register (SAR) ADC in a single-supply environment.

The noise that the amplifier generates originates from the input differential stage. The input stage of every amplifier generates transistor-device noise, which spot-noise graphs describe as referred-to-input (RTI) noise. With this graphical information we can determine how much noise reaches the input terminal of the ADC by calculating the referred-to-output (RTO) amplifier noise.

This discussion begins with a description of the amplifier's device noise. The amplifier noise sources are then tied together into one figure of merit, and the units are converted from volts to an SNR in decibels. Finally, the impact of the op amp in this mixed-signal circuit (Figure 1) is determined by calculating the combination of the op amp SNR value with the ADC's SNR performance.

Characteristics of the amplifier noise

It is important to understand the noise that the operational amplifier generates in this application. The typical performance of the amplifier given in its product datasheet shows that the op amp noise behavior over frequency has a signature that is unmistakable (see Figure 2). In this article, since we will consider the effects of using a single-supply CMOS amplifier, the input current noise is low enough that we can ignore it. Here we will consider only the effects of the amplifier's voltage noise.

The amplifier noise specification in the typical amplifier datasheet is an RTI specification. We can model the amplifier noise as a voltage source at the non-inverting input of the amplifier. The electrical characteristics table of an operational amplifier gives the input voltage noise

Figure 1. Typical driver circuit for SAR ADC

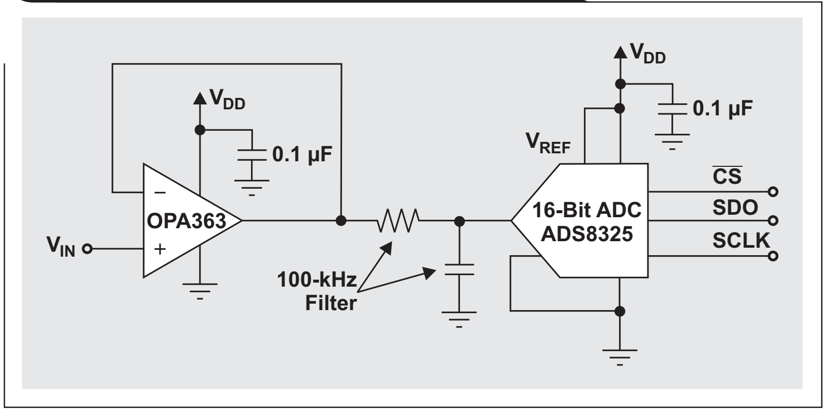
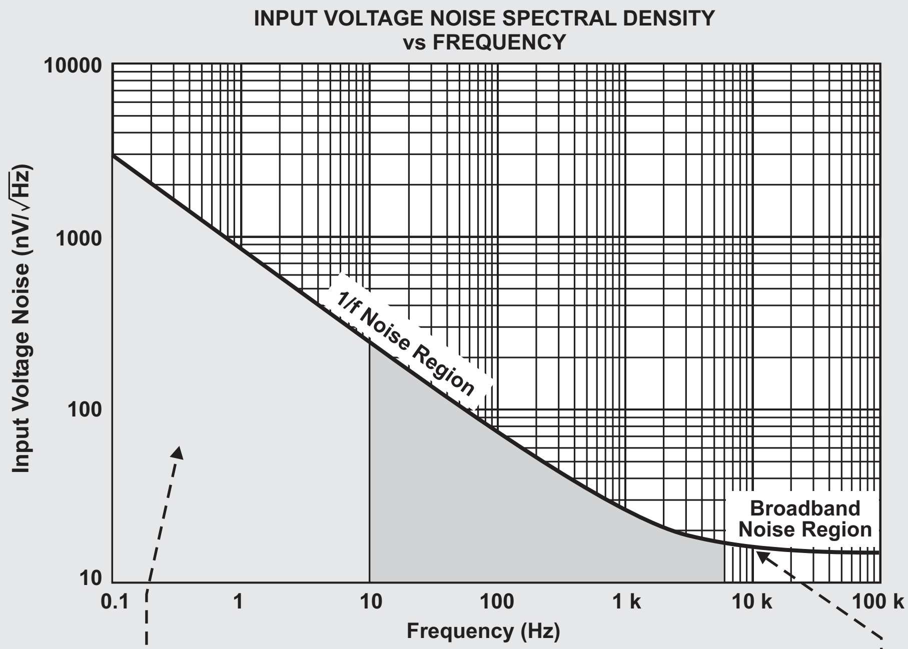


Figure 2. OPA363 amplifier noise parameters



Electrical Characteristics for OPA363

Parameter		Typical	Units
NOISE			
Input Voltage Noise, f = 0.1 to 10 Hz	e_n	10	μV_{PP}
Input Voltage Noise Density, f = 10 kHz	e_{nd}	17	nV/√Hz

and input voltage noise density specifications (see Figure 2). The input voltage noise specification (10 μV_{PP}) describes the low-frequency noise of the amplifier in terms of a bandwidth. This bandwidth is part of the 1/f noise region of the amplifier. The transistors in the input stage of the amplifier, along with the input-stage active load, generate this noise.

Input voltage noise density calls out a noise figure that refers to one frequency. For instance, the electrical characteristics table in Figure 2 shows that the input voltage noise density (e_{nd}) at 10 kHz is equal to 17 nV/√Hz. Usually this specification appears in the broadband-noise portion of the frequency plot (Figure 2). Theoretically, this broadband noise is flat. Assuming that it is flat is a good estimate of the amplifier's behavior. The resistors inside the operational amplifier primarily generate the broadband noise whether they are diffused resistors or the source and drain of the transistors.

The amplifier datasheet contains a typical specification graph that shows the input voltage noise density versus frequency. Figure 2 is an example of this type of graph. In this example, the input voltage noise specification is equal to the area beneath the input-voltage, noise-density curve between the specified frequencies of 0.1 and 10 Hz. Note that the units for this specification are peak-to-peak. To convert this to an rms value, simply divide the peak-to-peak value by 6.6 (industry-standard crest factor [CF] = 3.3).

Table 1 contains typical CF values used to convert rms to peak-to-peak values (and vice versa). To estimate the peak-to-peak operational amplifier output noise voltage, multiply the rms output voltage by 2 × CF. To estimate the ADC peak-to-peak output bit performance, subtract the bit crest factor (BCF) from the rms specification.

Table 1. Crest factor and bit crest factor values used for conversions from rms to peak-to-peak

CREST FACTOR (CF) (V)	BIT CREST FACTOR (BCF) (Bits)	ADC CONVERSIONS WITHIN THE PEAK-TO-PEAK LEVELS (%)
2.6	2.38	99
3.3*	2.72	99.9
3.9	2.96	99.99
4.4	3.14	99.999
4.9	3.29	99.9999

*Industry standard

We can easily calculate the noise underneath the curve in Figure 2 for different input voltage noise bandwidths in the 1/f region. The first order of business in this calculation is to determine the input noise density at 1 Hz. Once we find that value, the following simple formula will provide the rms noise under the curve.

$$V_{(1/f):\ f1\text{-}f2} = C\sqrt{\ln\left(\frac{f_2}{f_1}\right)},$$

where C is equal to the input noise density at 1 Hz.

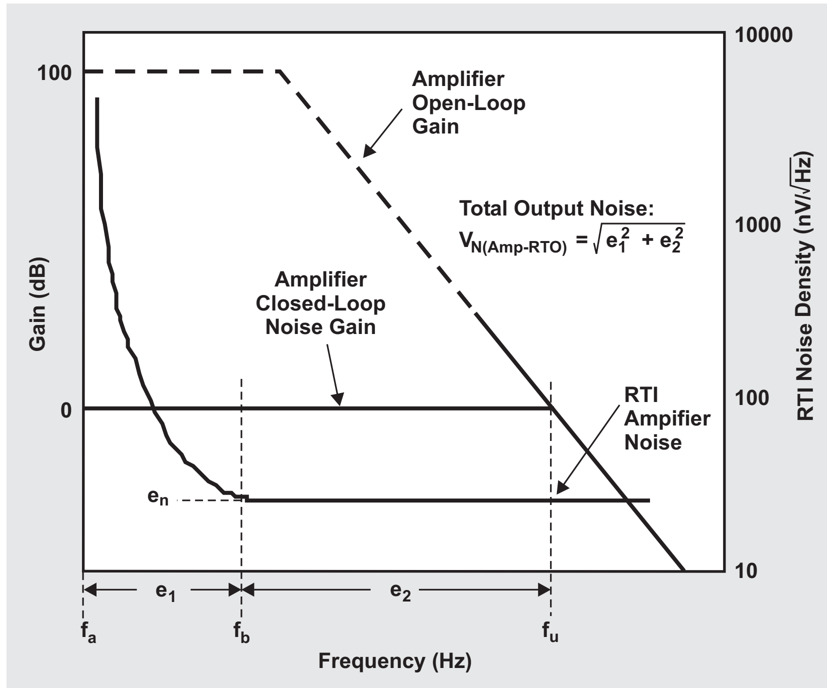
As an example, the amount of rms noise produced by the amplifier shown in Figure 2 from 0.1 Hz to 6000 Hz is:

$$V_{(1/f):\ f1\text{-}f2} = C\sqrt{\ln\left(\frac{f_2}{f_1}\right)},$$

$$V_{(1/f):\ f1\text{-}f2} = 700\ \text{nV}\sqrt{\ln\left(\frac{6000}{0.1}\right)},\ \text{and}$$

$$V_{(1/f):\ f1\text{-}f2} = 2.32\ \mu\text{Vrms}.$$

Figure 3. Typical RTI noise evaluation



With this calculation, and with the amplifier noise gain G = 1, the SNR at the output of the amplifier for the 1/f noise is:

$$SNR_{OPA} = 20\log_{10}\left(\frac{V_{OUT\text{-}rms}}{G \times V_{(1/f):\ f1\text{-}f2}}\right),$$

$$SNR_{OPA} = 20\log_{10}\left(\frac{\frac{5\ \text{V}}{2\sqrt{2}}}{2.32\ \mu\text{V}}\right),\ \text{and}$$

$$SNR_{OPA} = 117.6\ \text{dB}.$$

When we think about noise at these low frequencies, we may jump to the conclusion that we should take this formula down to a very low frequency, such as 0.0001 Hz (0.0001 Hz = 1 cycle per 2.8 hours). However, at frequencies lower than 0.1 Hz, which is one cycle every 10 seconds, it is very possible that other things such as temperature, aging, or component life are changing in the circuit. Realistically, low-frequency noise from the amplifier will probably not appear at this sample speed; but changes in the circuit, such as temperature or power supply voltage, may.

The amplifier table of specifications (Figure 2) also gives the input noise density value. This specification is always at a higher frequency, in the area where the input voltage noise is relatively constant. For this region of the curve, multiplying the square root of the bandwidth and the noise density derives the noise across this bandwidth. For example, if the noise of the amplifier is 17 nV/√Hz at 10 kHz, the noise from the amplifier across the bandwidth of 6 kHz to 100 kHz is:

$$V_{1\text{-}100\ \text{kHz}} = (\text{Noise Density at 10 kHz})\sqrt{\text{BW}},$$

$$V_{1\text{-}100\ \text{kHz}} = e_{nd}\sqrt{\text{BW}},$$

$$V_{1\text{-}100\ \text{kHz}} = \left(17\ \text{nV}/\sqrt{\text{Hz}}\right)\left(\sqrt{100{,}000 - 1{,}000}\right),\ \text{and}$$

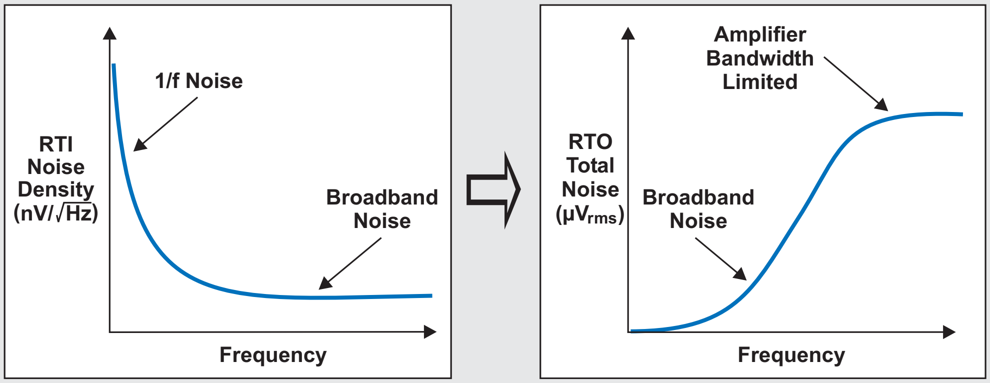
$$V_{1\text{-}100\ \text{kHz}} = 5.21\ \mu\text{Vrms},$$

where BW is equal to the bandwidth of interest.

So how do we get from the manufacturer's graph to an RTO noise value? We calculate the area beneath the noise curve and multiply that times the noise gain of the amplifier. In this example, the noise gain of our circuit is +1 V/V. We determine the noise that the amplifier contributes in both regions and then add the two values together using the square root of the sum of the squares. Figure 3 shows the formula for this calculation and illustrates the two regions.

Figure 3 separates the noise into two parts. In region e_1, we gain the 1/f noise of the amplifier by the dc gain of the amplifier circuit, which is +1 V/V. The specifications for amplifier noise are in nanovolts per square root of hertz. So the analysis is complete when we multiply the average noise over the region by the square root of the bandwidth of that region. For CMOS amplifiers, the 1/f region is usually from 0.1 Hz to 100 Hz up to 1000 Hz. Since this noise value is multiplied by the square root of the bandwidth, its

Figure 4. Graphical representation of RTI noise density and RTO noise



(a) Simulated Noise Response (b) Cumulative Noise

Note: The area under the RTI plot of a frequency region is multiplied by the square root of that bandwidth and closed-loop gain to calculate the RTO plot.

contribution is low. In region e_2, the broadband noise of the amplifier is multiplied by the amplifier circuit gain, which is again +1 V/V, and the square root of the bandwidth.

Each region contributes to the overall circuit noise:

$$e_1 = C\sqrt{\ln\left(\frac{f_b}{f_a}\right)} = 2.32\ \mu\text{Vrms}$$

$$e_2 = e_n\sqrt{f_2 - f_1} = 5.21\ \mu\text{Vrms}$$

The total noise at the output of the amplifier is:

$$V_{N(\text{Amp-RTO})} = \sqrt{e_1^2 + e_2^2}$$

$$= 5.70\ \mu\text{Vrms}.$$

With this calculation, the SNR at the output of the amplifier for the 1/f noise is:

$$\text{SNR}_{\text{OPA}} = 20\log_{10}\left(\frac{V_{\text{OUT-rms}}}{V_{N(\text{Amp-RTO})}}\right),$$

$$\text{SNR}_{\text{OPA}} = 20\log_{10}\left(\frac{\frac{5\text{ V}}{2\sqrt{2}}}{5.70\ \mu\text{V}}\right), \text{ and}$$

$$\text{SNR}_{\text{OPA}} = 109.8\text{ dB}.$$

We can validate this noise calculation using the Texas Instruments (TI) SPICE simulation tool, TINA-TI™. This tool can be found at amplifier.ti.com under “Engineering Resources.”

The two graphs in Figure 4 demonstrate how TINA-TI can help us understand the noise in our circuit. Figure 4(a) shows the simulated noise response of an amplifier. Figure 4(b) provides the cumulative noise as frequency increases. Notice that the noise is very low at the lower frequencies in Figure 4(b). This is because the lower bandwidths are multiplied by the square root of a small number, the bandwidth. As frequency increases, the cumulative noise also increases. One would think that at higher frequencies the increases in noise would be less because of the characteristics of Figure 4(a). As we can see, this is not true, because the bandwidth multiplier (square root of the bandwidth) is larger at higher frequencies.

Combining the op amp and ADC noise figures

Once we examine the amplifier for possible noise sources, it is easy to evaluate the total noise of the system in Figure 1. This system uses the 16-bit ADC, ADS8325, whose maximum sample rate is 100 ksps. The typical SNR of this device is 91 dB.

As we found before, the OPA363 RTO noise is 109.8 dB. Now we can determine the total noise of the system by using the op amp SNR and ADC SNR, and applying the theorem of taking the square root of the sum of the squares.

$$\text{SNR}_{\text{Total}} = -20\log_{10}\sqrt{10^{-\text{SNR Op Amp}/10} + 10^{-\text{SNR ADC}/10}}$$

$$\text{SNR}_{\text{Total}} = 90.94\text{ dB}$$

From this calculation we can see that the amplifier noise has very little impact on the resolution of the system.

With the devices in the circuit, the SNR performance will always be equal to or less than the lowest value. Given this interaction between the amplifier and ADC, picking a higher-noise amplifier will give the worst results. For instance, if we use an amplifier in a gain of 10 V/V that has a typical voltage noise specification of $e_{nd} = 45\ nV/\sqrt{Hz}$ at 10 kHz, then SNR_{Total} is 82.2 dB. If we use the 16-bit ADS8325, then SNR_{Total} is 81.6 dB. In this example, the amplifier is dominating the noise of the circuit.

There are more factors that have an effect on the amplifier selection process, but amplifier noise can have a significant effect on the digital code outcome. If the amplifier is too noisy, the ADC will reliably convert the noise from the amplifier circuit to the digital output. On the other hand, it is possible to have an ADC that is noisier than the amplifier circuit. If we choose an extremely low-noise amplifier without evaluating the system, we will probably spend too much money on one component or the other. Determining the potential noise in a circuit is always a daunting challenge, but there are some general rules of thumb that can be applied to overcome these problems. We can use the circuit's frequency range to our advantage in the calculations; and, when we combine noise sources, we can use the equation for the square root of the sum of the squares. By using these tricks we can quickly determine the compatibility of our amplifier/ADC combination.

In this circuit an amplifier isolates impedances in the signal chain. Other features, like gain or filtering, can be added; but regardless of the features we put around the amplifier, we should always ensure that the amplifier circuit preserves the integrity of the ADC.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "1.8V, 7MHz, 90dB CMRR, Single-Supply, Rail-to-Rail I/O Operational Amplifier," OPA363/2363, OPA364/2364, OPA4364 Datasheet	sbos259
2. Bonnie Baker, *A Baker's Dozen: Real Analog Solutions for Digital Designers* (Newnes-Elsevier, 2005).	—
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Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/ADS8325
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